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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	960
Number of Logic Elements/Cells	7680
Total RAM Bits	131072
Number of I/O	150
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	196-VFBGA, CSPBGA
Supplier Device Package	196-CSPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l08f-tcb196c

Table 8 lists the I/O standards that can co-exist in I/O Bank 3, depending on the VCCIO_3 voltage.

***Table 8:* Compatible I/O Standards in I/O Bank 3 of iCE65L04 and iCE65L08**

VCCIO_3 Voltage	3.3V	2.5V	1.8V	1.5V
Compatible I/O Standards	SB_LVCMOS33_8	Any SB_LVCMOS25 SB_SSTL2_Class_2 SB_SSTL2_Class_1 SB_LVDS_INPUT	Any SB_LVCMOS18 SB_SSTL18_FULL SB_SSTL18_HALF SB_MDDR10 SB_MDDR8 SB_MDDR4 SB_MDDR2 SB_LVDS_INPUT	Any SB_LVCMOS15

Programmable Output Drive Strength

Each PIO in I/O Bank 3 offers programmable output drive strength, as listed in Table 8. For the LVCMOS and MDDR I/O standards, the output driver has settings for static drive currents ranging from 2 mA to 16 mA output drive current, depending on the I/O standard and supply voltage.

The SSTL18 and SSTL2 I/O standards offer full- and half-strength drive current options

Differential Inputs and Outputs

All PIO pins support "single-ended" I/O standards, such as LVCMOS. However, iCE65 FPGAs also support differential I/O standards where a single data value is represented by two complementary signals transmitted or received using a pair of PIO pins. The PIO pins in I/O Bank 3 of iCE65L04 and iCE65L08L08 support Low-Voltage Differential Swing (LVDS) and SubLVDS inputs as shown in Figure 8. Differential outputs are available in all four I/O banks.

Differential Inputs Only on I/O Bank 3 of iCE65L04 and iCE65L08

Differential receivers are required for popular applications such as LVDS and LVPECL clock inputs, camera interfaces, and for various telecommunications standards.

Specific pairs of PIO pins in I/O Bank 3 form a differential input. Each pair consists of a DPxxA and DPxxB pin, where "xx" represents the pair number. The DPxxB receives the true version of the signal while the DPxxA receives the complement of the signal. Typically, the resulting signal pair is routed on the printed circuit board (PCB) with matched 50Ω signal impedance. The differential signaling, the low voltage swing, and the matched signal routing are ideal for communicating very-high frequency signals. Differential signals are generally also more tolerant of system noise and generate little EMI themselves.

The LVDS input circuitry requires 2.5V on the VCCIO_3 voltage supply. Similarly, the SubLVDS input circuitry requires 1.8V on the VCCIO_3 voltage supply. For electrical specifications, see "Differential Inputs" on page 100.

Each differential input pair requires an external 100 Ω termination resistor, as shown in Figure 8.

The PIO pins that make up a differential input pair are indicated with a blue bounding box in the footprint diagrams and in the pinout tables.

For best possible performance, the global buffer inputs (GBIN[7:0]) connect directly to the their associated global buffers (GBUF[7:0]), bypassing the PIO logic and iCEgate circuitry as shown in Figure 7. Consequently, the direct GBIN-to-GBUF connection cannot be blocked by the iCEgate circuitry. However, it is possible to use iCEgate to block PIO-to-GBUF clock connections.

For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power

Input Pull-Up Resistors on I/O Banks 0, 1, and 2

The PIO pins in I/O Banks 0, 1, and 2 have an optional input pull-up resistor. Pull-up resistors are not provided in iCE65L04 and iCE65L08 I/O Bank 3. During the iCE65 configuration process, the input pull-up resistor is unconditionally enabled and pulls the input to within a diode drop of the associated I/O bank supply voltage (VCCIO_#). This prevents any signals from floating on the circuit board during configuration.

After iCE65 configuration is complete, the input pull-up resistor is optional, defined by a configuration bit. The pull-up resistor is also useful to tie off unused PIO pins. The Lattice iCEcube development software defines all unused PIO pins in I/O Banks 0, 1 and 2 as inputs with the pull-up resistor turned on. The pull-up resistor value depends on the VCCIO voltage applied to the bank, as shown in Table 49.

Note: JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, else VCCIO_1 draws current.

No Input Pull-up Resistors on I/O Bank 3 of iCE65L04 and iCE65L08

The PIO pins in I/O Bank 3 do not have an internal pull-up resistor. To minimize power consumption, tie unused PIO pins in Bank 3 to a known logic level or drive them as a disabled high-impedance output.

Input Hysteresis

Inputs typically have about 50 mV of hysteresis, as indicated in Table 49.

Output and Output Enable Signal Path

As shown in Figure 7, a signal from programmable interconnect feeds the OUT signal on a Programmable I/O pad. This output connects either directly to the associated package pin or is held in an optional output flip-flop. Because all flip-flops are automatically reset after configuration, the output from the output flip-flop can be optionally inverted so that an active-Low output signal is held in the disabled (High) state immediately after configuration.

Similarly, each Programmable I/O pin has an output enable or three-state control called OE. When OE = High, the OUT output signal drives the associated pad, as described in Table 10. When OE = Low, the output driver is in the high-impedance (Hi-Z) state. The OE output enable control signal itself connects either directly to the output buffer or is held in an optional register. The output buffer is optionally permanently enabled or permanently disabled, either to unconditionally drive output signals, or to allow input-only signals.

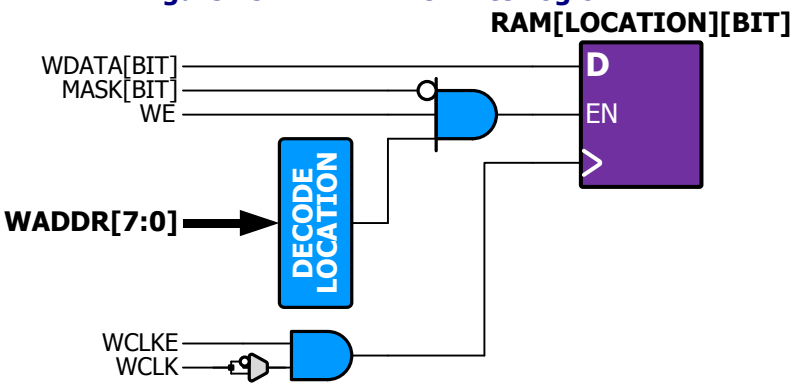
Table 10: **PIO Output Operations (non-registered operation, no inversions)**

Operation	OUT Data Output	OE Enable	PAD
Three-State	X	0	Hi-Z
Drive Output Data	OUT	1*	OUT

X = don't care, 1* = High or unused, Hi-Z = high-impedance, three-stated, floating.

See Input and Output Register Control per PIO Pair for information about the registered input path.

Figure 18: RAM4K Bit Write Logic



When the WCLKE signal is Low, the clock to the RAM4K block is disabled, keeping the RAM in its lowest power mode.

Table 18: RAM4K Write Operations

Operation	WDATA[15:0] Data	MASK[15:0] Mask Bit	WADDR[7:0] Address	WE Write Enable	WCLKE Clock Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	X	0	No change
Disabled					0	X	No change
Disabled	X	X	X	0	X	X	No change
Write Data	WDATA[i]	MASK[i] = 0	WADDR	1	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i] = 1	WADDR	1	1	↑	RAM[WADDR][i] = No change

To write data into the RAM4K block, perform the following operations.

- Supply a valid address on the WADDR[7:0] address input port
- Supply valid data on the WDATA[15:0] data input port
- To write or mask selected data bits, set the associated MASK input port accordingly. For example, write operations on data bit D[i] are controlled by the associated MASK[i] input.
  - MASK[i] = 0: Write operations are enabled for data line WDATA[i]
  - MASK[i] = 1: Mask write operations are disabled for data line WDATA[i]
- Enable the RAM4K write port (WE = 1)
- Enable the RAM4K write clock (WCLKE = 1)
- Apply a rising clock edge on WCLK (assuming that the clock is not inverted)

Read Operations

Figure 19 shows the logic involved in reading a location from RAM. Table 19 describes various read operations for a RAM4K block. By default, all RAM4K read operations are synchronized to the rising edge of RCLK although the clock is invertible as shown in Figure 19.

Device Configuration

As described in Table 20, iCE65 components are configured for a specific application by loading a binary configuration bitstream image, generated by the Lattice development system. For high-volume applications, the bitstream image is usually permanently programmed in the on-chip NVCM, However, the bitstream image can also be stored external in a standard, low-cost commodity SPI serial Flash PROM. The iCE65 component can automatically load the image using the SPI Master Configuration Interface. Similarly, the iCE65 configuration data can be downloaded from an external processor, microcontroller, or DSP processor using an SPI-like serial interface or an IEEE 1149 JTAG interface.

Table 20: **iCE65 Device Configuration Modes**

Mode	Analogy	Configuration Data Source
NVCM	ASIC	Internal, lowest-cost, secure, one-time programmable Nonvolatile Configuration Memory (NVCM)
SPI Flash	Microprocessor	External, low-cost, commodity, SPI serial Flash PROM
SPI Peripheral	Processor Peripheral	Configured by external device, such as a processor, microcontroller, or DSP using practically any data source, such as system Flash, a disk image, or over a network connection.
JTAG	JTAG	JTAG configuration requires sending a special command sequence on the SPI interface to enable JTAG configuration. Configuration is controlled by and external device.

Configuration Mode Selection

The iCE65 configuration mode is selected according to the following priority described below and illustrated in Figure 20.

- After exiting the Power-On Reset (POR) state or when CRESET_B returns High after being held Low for 250 ns or more, the iCE65 FPGA samples the logical value on its SPI_SS_B pin. Like other programmable I/O pins, the SPI_SS_B pin has an internal pull-up resistor (see Input Pull-Up Resistors on I/O Banks 0, 1, and 2).
- If the SPI_SS_B pin is sampled as a logic '1' (High), then …
  - Check if the iCE65 is enabled to configure from the Nonvolatile Configuration Memory (NVCM). If the iCE65 device has NVCM memory ('**F**' ordering code) but the NVCM is yet unprogrammed, then the iCE65 device is not enabled to configure from NVCM. Conversely, if the NVCM is programmed, the iCE65 device will configure from NVCM.
    - If enabled to configure from NVCM, the iCE65 device configures itself using NVCM.
    - If not enabled to configure from NVCM, then the iCE65 FPGA configures using the SPI Master Configuration Interface.
- If the SPI_SS_B pin is sampled as a logic '0' (Low), then the iCE65 device waits to be configured from an external controller or from another iCE65 device in SPI Master Configuration Mode using an SPI-like interface.

Figure 21: iCE65 Configuration Control Pins

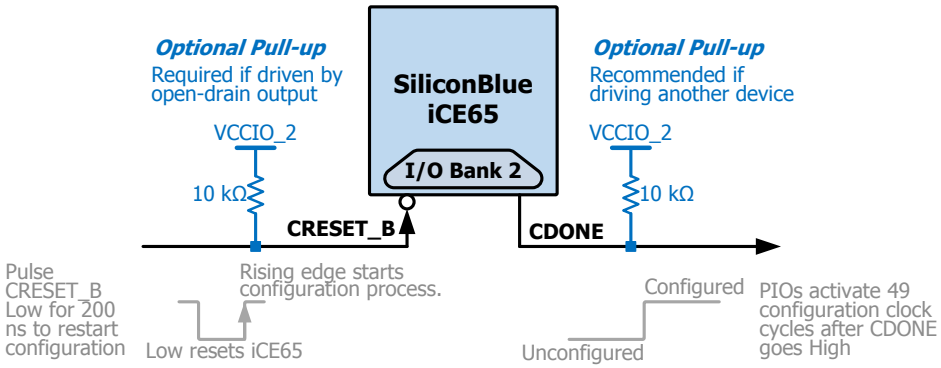


Figure 21 shows the two iCE65 configuration control pins, CRESET_B and CDONE. Table 23 lists the ball/pin numbers for the configuration control pins by package. When driven Low for at least 200 ns, the dedicated Configuration Reset input, CRESET_B, resets the iCE65 device. When CRESET_B returns High, the iCE65 FPGA restarts the configuration process from its power-on conditions (Cold Boot). The CRESET_B pin is a pure input with no internal pull-up resistor. If driven by open-drain driver or un-driven, then connect the CRESET_B pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

***Table 23:* Configuration Control Ball/Pin Numbers by Package**

Configuration Control Pins	CB81	QN84	VQ100	CB132	CB196	CB284
CRESET_B	J6	A21	44	L10	L10	R14
CDONE	H6	B16	43	M10	M10	T14

The iCE65 device signals the end of the configuration process by actively turning off the internal pull-down transistor on the Configuration Done output pin, CDONE. The pin has a permanent, weak internal pull-up resistor to the VCCIO_2 rail. If the iCE65 device drives other devices, then optionally connect the CDONE pin to a 10 kΩ pull-up resistor connected to the VCCIO_2 supply.

The PIO pins activate according to their configured function after 49 configuration clock cycles. The internal oscillator is the configuration clock source for the SPI Master Configuration Interface and when configuring from

* Note: only 14 of the 16 RAM4K Memory Blocks may be pre-initialized in the iCE65L01.

Nonvolatile Configuration Memory (NVCM). When using the SPI Peripheral Configuration Interface, the configuration clock source is the SPI_SCK clock input pin.

Internal Oscillator

During SPI Master or NVCM configuration mode, the controlling clock signal is generated from an internal oscillator. The oscillator starts operating at the Default frequency. During the configuration process, however, bit settings within the configuration bitstream can specify a higher-frequency mode in order to maximize SPI bandwidth and reduce overall configuration time. See Table 57: Internal Oscillator Frequency on page 105 for the specified oscillator frequency range.

Using the SPI Master Configuration Interface, internal oscillator controls all the interface timing and clocks the SPI serial Flash PROM via the SPI_SCK clock output pin.

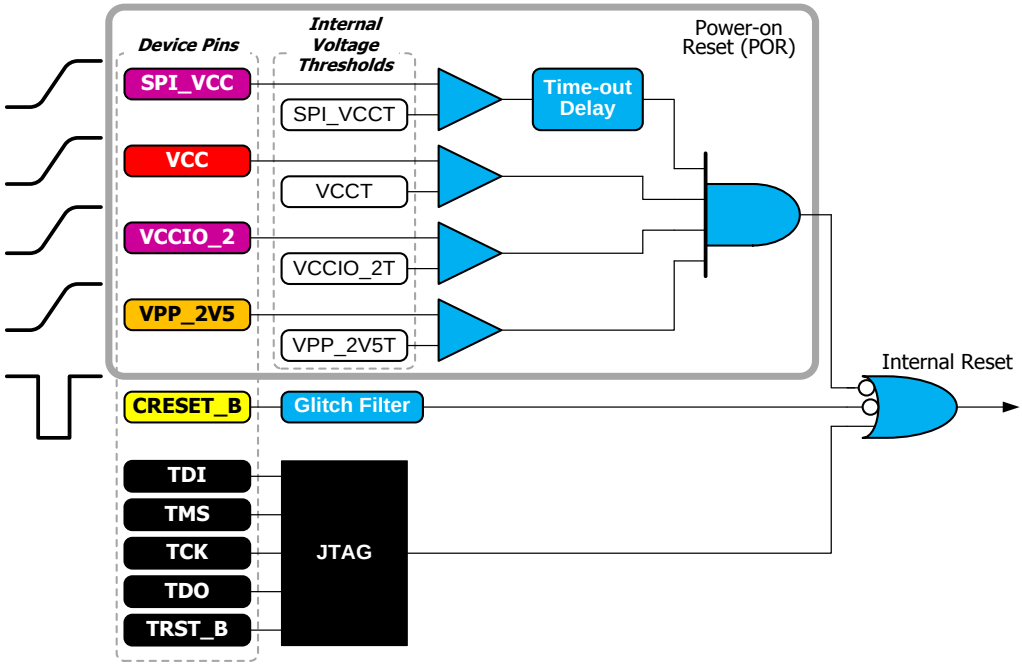
The oscillator output, which also supplies the SPI SCK clock output during the SPI Flash configuration process, has a 50% duty cycle.

Internal Device Reset

Figure 22 presents the various signals that internally reset the iCE65 internal logic.

- Power-On Reset (POR)
- CRESET_B Pin
- JTAG Interface

Figure 22: iCE65 Internal Reset Circuitry



Power-On Reset (POR)

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

Supply Rail	iCE65 Production Devices
VCC	Yes
SPI_VCC	Yes
VCCIO_1	No
VCCIO_2	Yes
VPP_2V5	Yes

CRESET_B Pin

The CRESET_B pin resets the iCE65 internal logic when Low.

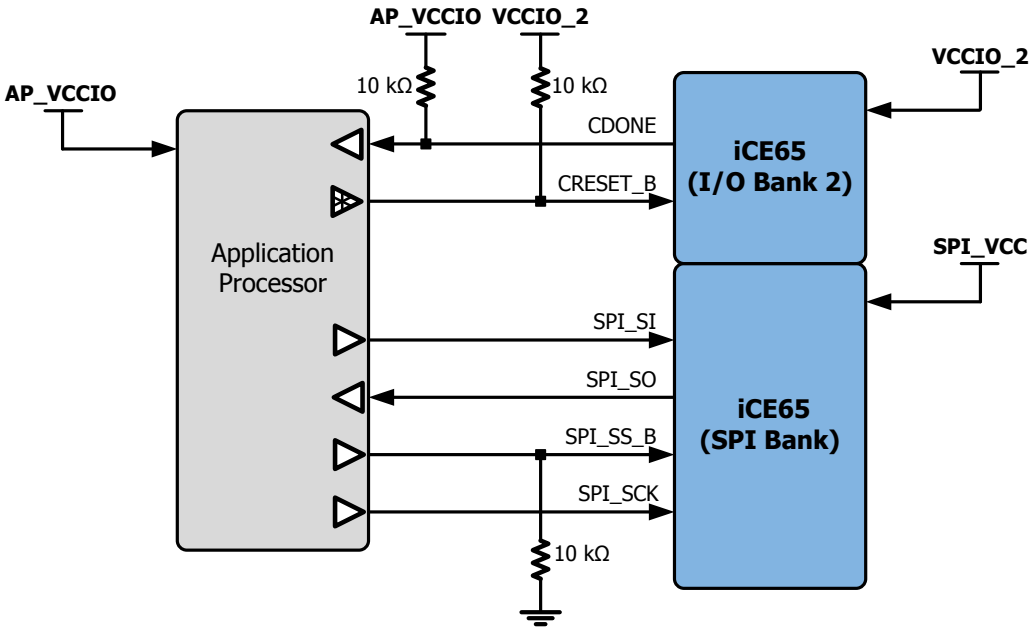
JTAG Interface

Specific command sequences also reset the iCE65 internal logic.

SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 28: **iCE65 SPI Peripheral Configuration Interface**



The SPI control signals are defined in Table 25.

Table 29: **SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)**

Signal Name	Direction	iCE65 I/O Supply	Description
CDONE	AP ← iCE65	VCCIO_2	Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC.
CRESET_B	AP → iCE65		Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2.
SPI_VCC	Supply	SPI_VCC	SPI Flash PROM voltage supply input.
SPI_SI	AP → iCE65		SPI Serial Input to the iCE65 FPGA, driven by the application processor.
SPI_SO	AP ← iCE65		SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM.
SPI_SS_B	AP → iCE65		SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground.
SPI_SCK	AP → iCE65		SPI Slave Clock output from the application processor.

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

SPI Peripheral Configuration Process

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

After driving CRESET_B High or allowing it to float High, the AP must wait a minimum of t_{CR_SCK} µs, (see Table 60) allowing the iCE65 FPGA to clear its internal configuration memory.

After waiting for the configuration memory to clear, the AP sends the configuration image generated by the iCEcube development system. An SPI peripheral mode configuration image must not use the ColdBoot or WarmBoot options. Send the entire configuration image, without interruption, serially to the iCE65's SPI_SI input on the falling edge of the SPI_SCK clock input. Once the AP sends the 0x7EAA997E synchronization pattern, the generated SPI_SCK clock frequency must be within the specified 1 MHz to 25 MHz range (40 ns to 1 µs clock period) while sending the configuration image. Send each byte of the configuration image with most-significant bit (msb) first. The AP sends data to the iCE65 FPGA on the falling edge of the SPI_SCK clock. The iCE65 FPGA internally captures each incoming SPI_SI data bit on the rising edge of the SPI_SCK clock. The iCE65's SPI_SO output pin is not used during SPI peripheral mode but must connect to the AP if the AP also programs the iCE65's Nonvolatile Configuration Memory (NVCM).

Prior to sending the iCE65 configuration image , an SPI NVCM shut-off sequence must be sent. See AN014 for details.
The iCE65 configuration image must be sent as one contiguous stream without interruption.
The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

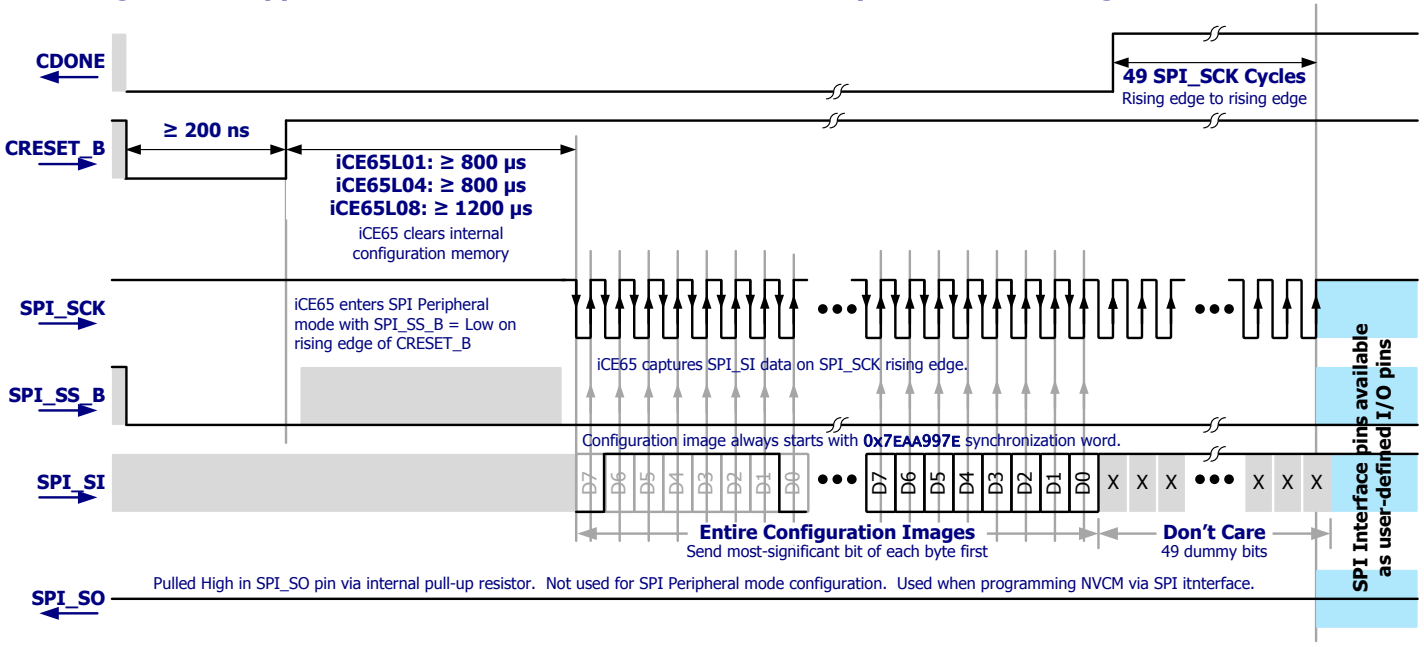
After sending the entire image, the iCE65 FPGA releases the CDONE output allowing it to float High via the 10 kΩ pull-up resistor to AP_VCC. If the CDONE pin remains Low, then an error occurred during configuration and the AP should handle the error accordingly for the application.

After the CDONE output pin goes High, send at least 49 additional dummy bits, effectively 49 additional SPI_SCK clock cycles measured from rising-edge to rising-edge.

After the additional SPI_CLK cycles, the SPI interface pins then become available to the user application loaded in FPGA.

To reconfigure the iCE65 FPGA or to load a different configuration image, merely restart the configuration process by pulsing CRESET_B Low or power-cycling the FPGA.

Figure 29: **Application Processor Waveforms for SPI Peripheral Mode Configuration Process**



The iCE65 configuration image must be sent as one contiguous stream without interruption.

The SPI_SCK clock period must be between 40 ns to 1 µs (1 MHz to 25 MHz).

Supported JTAG Commands

The JTAG interface supports the IEEE 1149.1 mandatory instructions, including EXTEST, SAMPLE/PRELOAD, and BYPASS.

Package and Pinout Information

Maximum User I/O Pins by Package and by I/O Bank

Table 34 lists the maximum number of user-programmable I/O pins by package, with additional detail showing user I/O pins by I/O bank. In some cases, a smaller iCE65 device is packaged in a larger package with unconnected (N.C.) pins or balls, resulting in fewer overall I/O pins. See Table 35 for device-specific I/O counts by package.

Table 34: **User I/O by Package, by I/O Bank**

	CB81	QN84	VQ100	CB132	CB196	CB284
Package Leads	81	84	100	132	196	284
Package Body (mm)	5 x 5	7 x 7	14 x 14	8 x 8	8 x 8	12 x 12
Ball Array (balls)	9 x 9	N/A	N/A	14 x 14	14 x 14	22 x 22
Ball/Lead Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5
Maximum user I/O, all I/O banks	63	67	72	95	150	222
PIO Pins in Bank 0	17	17	19	26	37	60
PIO Pins in Bank 1	16	17	19	21	38	55
PIO Pins in Bank 2	12	11	12	20	35	53
PIO Pins in Bank 3	18	18	18	24	36	50
PIO Pins in SPI Interface	4	4	4	4	4	4

Printed Circuit Board Layout Information

For information on how to use the iCE65 packages on a printed circuit board (PCB) design, consult the following application note.

- AN010: iCE65 Printed Circuit Board (PCB Layout) Guidelines

Maximum User I/O by Device and Package

Table 35 lists the maximum available user I/O by device and by and package type. Not all devices are available in all packages. Similarly, smaller iCE65 devices may have unconnected balls in some packages. Devices sharing a common package have similar footprints.

Table 35: **Maximum User I/O by Device and Package**

Package	Device		
	iCE65L01	**iCE65L04**	**iCE65L08**
CB81	63	—	—
QN84	67	—	—
VQ100	72	72	
CB132	93	95	—
CB196	—	150	150
CB284	—	176	222

iCE65 Pin Descriptions

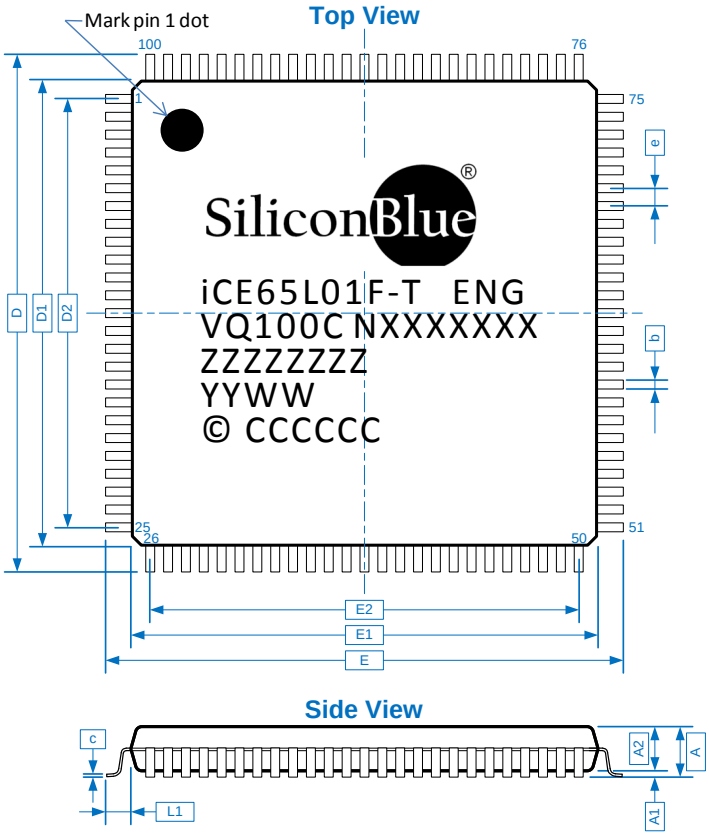
Table 36 lists the various iCE65 pins, alphabetically by name. The table indicates the directionality of the signal and the associated I/O bank. The table also indicates if the signal has an internal pull-up resistor enabled during configuration. Finally, the table describes the function of the pin.

Table 36: iCE65 Pin Description

Signal Name	Direction	I/O Bank	Pull-up during Config	Description
CDONE	Output	2	Yes	Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2.. If driving external devices with CDONE output, connect a 10 kΩ pull-up resistor to VCCIO_2.
CRESET_B	Input	2	No	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to VCCIO_2.
GBIN0/PIO0 GBIN1/PIO0	Input/IO	0	Yes	Global buffer input from I/O Bank 0. Optionally, a full-featured PIO pin.
GBIN2/PIO1 GBIN3/PIO1	Input/IO	1	Yes	Global buffer input from I/O Bank 1. Optionally, a full-featured PIO pin.
GBIN4/PIO2 GBIN5/PIO2	Input/IO	2	Yes	Global buffer input from I/O Bank 2. Optionally, a full-featured PIO pin.
GBIN6/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin.
GBIN7/PIO3	Input/IO	3	No	Global buffer input from I/O Bank 3. Optionally, a full-featured PIO pin. Optionally, a differential clock input using the associated differential input pin.
GND	Supply	All	N/A	Ground. All must be connected.
PIOx_yy	I/O	0,1,2	Yes	Programmable I/O pin defined by the iCE65 configuration bitstream. The 'x' number specifies the I/O bank number in which the I/O pin resides. The "yy' number specifies the I/O number in that bank.
PIO2/CBSEL0	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO2/CBSEL1	Input/IO	2	Yes	Optional ColdBoot configuration SELect input, if ColdBoot mode is enabled. A full-featured PIO pin after configuration.
PIO3_yy/ DPwwz	I/O	3	No	Programmable I/O pin that is also half of a differential I/O pair. Only available in I/O Bank 3. The "yy" number specifies the I/O number in that bank. The "ww" number indicates the differential I/O pair. The 'z' indicates the polarity of the pin in the differential pair. 'A'=negative input. 'B'=positive input.
PIOS/SPI_SO	I/O	SPI	Yes	SPI Serial Output. A full-featured PIO pin after configuration.
PIOS /SPI_SI	I/O	SPI	Yes	SPI Serial Input. A full-featured PIO pin after configuration.
PIOS / SPI_SS_B	I/O	SPI	Yes	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to SPI_VCC during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE65 device, as shown in Figure 20. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
PIOS/ SPI_SCK	I/O	SPI	Yes	SPI Slave Clock. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. A full-featured PIO pin after configuration.
TDI	Input	1	No	JTAG Test Data Input. If using the JTAG interface, use a 10kΩ pull-up resistor to VCCIO_1. Tie off to GND when unused.

Pin Function	Pin Number	Type	Bank
PIO2	28	PIO	2
PIO2	29	PIO	2
PIO2	30	PIO	2
PIO2	iCE65L01: 34 iCE65L04: 36	PIO	2
PIO2	37	PIO	2
PIO2	40	PIO	2
PIO2/CBSEL0	41	PIO	2
PIO2/CBSEL1	42	PIO	2
VCCIO_2	31	VCCIO	2
VCCIO_2	38	VCCIO	2
PIO3/DP00A	1	PIO/DPIO	3
PIO3/DP00B	2	PIO/DPIO	3
PIO3/DP01A	3	PIO/DPIO	3
PIO3/DP01B	4	PIO/DPIO	3
PIO3/DP02A	7	PIO/DPIO	3
PIO3/DP02B	8	PIO/DPIO	3
PIO3/DP03A	9	PIO/DPIO	3
PIO3/DP03B	10	PIO/DPIO	3
PIO3/DP04A	12	PIO/DPIO	3
GBIN7/PIO3/DP04B	13	GBIN/DPIO	3
GBIN6/PIO3/DP05A	15	GBIN/DPIO	3
PIO3/DP05B	16	PIO/DPIO	3
PIO3/DP06A	18	PIO/DPIO	3
PIO3/DP06B	19	PIO/DPIO	3
PIO3/DP07A	20	PIO/DPIO	3
PIO3/DP07B	21	PIO/DPIO	3
PIO3/DP08A	24	PIO/DPIO	3
PIO3/DP08B	25	PIO/DPIO	3
VCCIO_3	6	VCCIO	3
VCCIO_3	14	VCCIO	3
VCCIO_3	22	VCCIO	3
PIOS/SPI_SO	45	SPI	SPI
PIOS/SPI_SI	46	SPI	SPI
PIOS/SPI_SCK	48	SPI	SPI
PIOS/SPI_SS_B	49	SPI	SPI
SPI_VCC	50	SPI	SPI
GND	5	GND	GND
GND	17	GND	GND
GND	23	GND	GND
GND	32	GND	GND
GND	39	GND	GND
GND	47	GND	GND
GND	55	GND	GND
GND	70	GND	GND
GND	84	GND	GND
GND	98	GND	GND
VCC	11	VCC	VCC
VCC	35	VCC	VCC

Figure 38: VQ100 Package Mechanical Drawing: NVCM Programmed Device Marking



Description		Symbol	Min.	Nominal	Max.	Units
Leads per Edge	X			25		Leads
	Y			25		
Number of Signal Leads		n		100		
Maximum Size (lead tip to lead tip)	X	E	—	16.0	—	mm
	Y	D	—	16.0	—	
Body Size	X	E1	—	14.0	—	
	Y	D1	—	14.0	—	
Edge Pin Center to Center	X	E2	—	12.0	—	
	Y	D2	—	12.0	—	
Lead Pitch		e	—	0.50	—	
Lead Width		b	0.17	0.20	0.27	
Total Package Height		A	—	1.20	—	
Stand Off		A1	0.05	—	0.15	
Body Thickness		A2	0.95	1.00	1.05	
Lead Length		L1	—	1.00	—	
Lead Thickness		c	0.09	—	0.20	
Coplanarity			—	0.08	—	

Top Marking Format

Line	Content	Description
1	Logo	Logo
2	iCE65L01F	Part number
	-T	Power/Speed
	ENG	Engineering
3	VQ100C NXXXXXXX	Package type and Lot number
4	ZZZZZZZZ	NVCM Program. code
5	YYWW	Date Code
6	© CCCCCC	Country

Thermal Resistance

Junction-to-Ambient θ_{JA} (°C/W)	
0 LFM	200 LFM
38	32

Ball Function	Ball Number	Pin Type	Bank
PIO1	F14	PIO	1
PIO1	G10	PIO	1
PIO1	G11	PIO	1
PIO1	G13	PIO	1
PIO1	G14	PIO	1
PIO1	H10	PIO	1
PIO1	H11	PIO	1
PIO1	H12	PIO	1
PIO1	H13	PIO	1
PIO1	J10	PIO	1
PIO1	J11	PIO	1
PIO1	J12	PIO	1
PIO1	J13	PIO	1
PIO1	K11	PIO	1
PIO1	K12	PIO	1
PIO1	K14	PIO	1
PIO1	L13	PIO	1
PIO1	L14	PIO	1
PIO1	M13	PIO	1
TCK	L12	JTAG	1
TDI	M12	JTAG	1
TDO	N14	JTAG	1
TMS	P14	JTAG	1
TRST_B	M14	JTAG	1
VCCIO_1	F9	VCCIO	1
VCCIO_1	H14	VCCIO	1
CDONE	M10	CONFIG	2
CRESET_B	L10	CONFIG	2
GBIN4/PIO2 (◆)	***iCE65L04:*** L7 ***iCE65L08:*** N8	GBIN	2
GBIN5/PIO2 (◆)	***iCE65L04:*** P5 ***iCE65L08:*** M7	GBIN	2
PIO2	K5	PIO	2
PIO2	K6	PIO	2
PIO2	K7	PIO	2
PIO2	K8	PIO	2
PIO2	K9	PIO	2
PIO2	L4	PIO	2
PIO2	L5	PIO	2
PIO2	L6	PIO	2
PIO2	L8	PIO	2
PIO2	M3	PIO	2
PIO2	M4	PIO	2
PIO2	M6	PIO	2
PIO2 (◆)	***iCE65L04:*** M7 ***iCE65L08:*** P5	PIO	2
PIO2	M8	PIO	2
PIO2	M9	PIO	2
PIO2	N3	PIO	2
PIO2	N4	PIO	2
PIO2	N5	PIO	2
PIO2	N6	PIO	2

Ball Function	Ball Number	Pin Type	Bank
PIO3/DP13A	H5	DPIO	3
PIO3/DP13B	G5	DPIO	3
PIO3/DP14A	L1	DPIO	3
PIO3/DP14B	L2	DPIO	3
PIO3/DP15A	M1	DPIO	3
PIO3/DP15B	M2	DPIO	3
PIO3/DP16A (◆)	***iCE65L04:*** K3 ***iCE65L08:*** K4	DPIO	3
PIO3/DP16B (◆)	***iCE65L08:*** K4 ***iCE65L08:*** K3	DPIO	3
PIO3/DP17A	N1	DPIO	3
PIO3/DP17B	N2	DPIO	3
VCCIO_3	E3	VCCIO	3
VCCIO_3	J6	VCCIO	3
VCCIO_3	K1	VCCIO	3
PIOS/SPI_SO	M11	SPI	SPI
PIOS/SPI_SI	P11	SPI	SPI
PIOS/SPI_SCK	P12	SPI	SPI
PIOS/SPI_SS_B	P13	SPI	SPI
SPI_VCC	L11	SPI	SPI
GND	A9	GND	GND
GND	B12	GND	GND
GND	C2	GND	GND
GND	F1	GND	GND
GND	F7	GND	GND
GND	G7	GND	GND
GND	G8	GND	GND
GND	G9	GND	GND
GND	H6	GND	GND
GND	H7	GND	GND
GND	H8	GND	GND
GND	J5	GND	GND
GND	J8	GND	GND
GND	J14	GND	GND
GND	K10	GND	GND
GND	L3	GND	GND
GND	P6	GND	GND
VCC	B7	VCC	VCC
VCC	F2	VCC	VCC
VCC	F8	VCC	VCC
VCC	G6	VCC	VCC
VCC	H9	VCC	VCC
VCC	J4	VCC	VCC
VCC	J7	VCC	VCC
VCC	K13	VCC	VCC
VCC	N7	VCC	VCC
VPP_2V5	A14	VPP	VPP
VPP_FAST	A13	VPP	VPP

Ball Function	Ball Number iCE65L04 iCE65L08	Pin Type by Device iCE65L04	Pin Type by Device iCE65L08	Bank	CB132 Ball Equivalent
PIO0	E15	PIO	PIO	0	A11
PIO0	E16	PIO	PIO	0	A12
PIO0	G8	PIO	PIO	0	C4
PIO0	G9	PIO	PIO	0	C5
PIO0	G10	PIO	PIO	0	C6
PIO0	G11	PIO	PIO	0	C7
PIO0	G12	PIO	PIO	0	C8
PIO0	G13	PIO	PIO	0	C9
PIO0	G14	PIO	PIO	0	C10
PIO0	G15	PIO	PIO	0	C11
PIO0	G16	PIO	PIO	0	C12
PIO0	H9	PIO	PIO	0	D5
PIO0	H10	PIO	PIO	0	D6
PIO0	H11	PIO	PIO	0	D7
PIO0	H12	PIO	PIO	0	D8
PIO0	H13	PIO	PIO	0	D9
PIO0	H14	PIO	PIO	0	D10
PIO0	H15	PIO	PIO	0	D11
VCCIO_0	A8	VCCIO	VCCIO	0	—
VCCIO_0	A21	VCCIO	VCCIO	0	—
VCCIO_0	E12	VCCIO	VCCIO	0	A8
VCCIO_0	K10	VCCIO	VCCIO	0	F6
GBIN2/PIO1	L18	GBIN	GBIN	1	G14
GBIN3/PIO1	K18	GBIN	GBIN	1	F14
PIO1 (●)	A22	N.C.	PIO	1	—
PIO1 (●)	AA22	N.C.	PIO	1	—
PIO1 (●)	B22	N.C.	PIO	1	—
PIO1	C20	PIO	PIO	1	—
PIO1 (●)	C22	N.C.	PIO	1	—
PIO1	D20	PIO	PIO	1	—
PIO1 (●)	D22	N.C.	PIO	1	—
PIO1	E20	PIO	PIO	1	—
PIO1 (●)	E22	N.C.	PIO	1	—
PIO1	F18	PIO	PIO	1	B14
PIO1	F20	PIO	PIO	1	—
PIO1 (●)	F22	N.C.	PIO	1	—
PIO1	G18	PIO	PIO	1	C14
PIO1	G20	PIO	PIO	1	—
PIO1	G22	PIO	PIO	1	—
PIO1	H16	PIO	PIO	1	D12
PIO1	H18	PIO	PIO	1	D14
PIO1	H20	PIO	PIO	1	—
PIO1	J15	PIO	PIO	1	E11
PIO1	J16	PIO	PIO	1	E12
PIO1	J18	PIO	PIO	1	E14
PIO1 (●)	J22	N.C.	PIO	1	—
PIO1	K15	PIO	PIO	1	F11
PIO1	K16	PIO	PIO	1	F12
PIO1	K20	PIO	PIO	1	—
PIO1 (●)	K22	N.C.	PIO	1	—

Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 47: Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VCC	Core supply Voltage	–0.5	1.42	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply			V
VPP_FAST	Optional fast NVCM programming supply			V
VCCIO_0 **VCCIO_1** **VCCIO_2** **SPI_VCC**	I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface)	–0.5	4.00	V
VCCIO_3	I/O Bank 3 supply voltage	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
VIN_0 **VIN_1** **VIN_2** **VIN_SPI**	Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface)	–1.0	5.5	V
VIN_3 **VIN_VREF**	Voltage applied to PIO pin within I/O Bank 3	–0.5	iCE65L01: 4.00 iCE65L04/08: 3.6	V
IOUT	DC output current per pin	—	20	mA
T_J	Junction temperature	–55	125	°C
T_{STG}	Storage temperature, no bias	–65	150	°C

Recommended Operating Conditions

Table 48: **Recommended Operating Conditions**

Symbol	Description		Minimum	Nominal	Maximum	Units
VCC	Core supply voltage	–L: Ultra-Low Power mode	0.95	1.00	1.05	V
		–L: Low Power –T: High Performance	1.14	1.20	1.26	V
VPP_2V5	VPP_2V5 NVCM programming and operating supply	Release from Power-on Reset	1.30	—	3.47	V
		Configure from NVCM	2.30	—	3.47	V
		NVCM programming	2.30	—	3.00	V
VPP_FAST	Optional fast NVCM programming supply		Leave unconnected in application			
SPI_VCC	SPI interface supply voltage		1.71	—	3.47	V
VCCIO_0 VCCIO_1 VCCIO_2 VCCIO_3 SPI_VCC	I/O standards, all banks*	**LVCMOS33**	3.14	3.30	3.47	V
		Non-standard voltage: in between 2.5V and 3.3V use LVCMOS25 in iCEcube2	Nominal -5%	2.5< Nominal <3.3	Nominal +5%	V
		LVCMOS25, LVDS	2.38	2.50	2.63	V
		LVCMOS18, SubLVDS	1.71	1.80	1.89	V
		LVCMOS15	1.43	1.50	1.58	V
VCCIO_3	I/O standards only available in iCE65L04/08 I/O Bank 3*	**SSTL2**	2.38	2.50	2.63	V
		SSTL18	1.71	1.80	1.89	V
		MDDR	1.71	1.80	1.89	V
T_A	Ambient temperature	Commercial (C)	0	—	70	°C
		Industrial (I)	–40	—	85	°C
T_{PROG}	NVCM programming temperature		10	25	30	°C

NOTE:

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

I/O Characteristics

Table 49: PIO Pin Electrical Characteristics

Symbol	Description		Conditions	Minimum	Nominal	Maximum	Units
I_I	Input pin leakage current	I/O Bank 0, 1, 2	V_{IN} = $VCCIO_{max}$ to 0 V			±10	µA
		I/O Bank 3	V_{IN} = $VCCIO_{max}$				
I_{OZ}	Three-state I/O pin (Hi-Z) leakage current		V_O = $VCCIO_{max}$ to 0 V			±10	µA
C_{PIO}	PIO pin input capacitance				6		pF
C_{GBIN}	GBIN global buffer pin input capacitance				6		pF
R_{PULLUP}	Internal PIO pull-up resistance during configuration		VCCIO = 3.3V		40		kΩ
			VCCIO = 2.5V		50		kΩ
			VCCIO = 1.8V		90		kΩ
			VCCIO = 1.5V				kΩ
			VCCIO = 1.2V				kΩ
V_{HYST}	Input hysteresis		VCCIO = 1.5V to 3.3V		50		mV

NOTE: All characteristics are characterized and may or may not be tested on each pin on each device.

Single-ended I/O Characteristics

Table 50: I/O Characteristics (I/O Banks 0, 1, 2 and SPI only) (I/O Bank 3 iCE65L01 only)

I/O Standard	Nominal I/O Bank Supply Voltage	Input Voltage (V)		Output Voltage (V)		Output Current at Voltage (mA)	
		V_{IL}	V_{IH}	V_{OL}	V_{OH}	I_{OL}	I_{OH}
LVCMOS33	3.3V	0.80	2.00	0.4	2.40	8	8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	6	6
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	1.40	4	4
LVCMOS15	1.5V	Not supported Use I/O Bank 3		0.4	1.20	2	2

Table 51: I/O Characteristics (I/O Bank 3 and iCE65L04/08 only)

I/O Standard	Supply Voltage	Input Voltage (V)		Output Voltage (V)		I/O Attribute Name	mA at Voltage
		Max. V_{IL}	Min. V_{IH}	Max. V_{OL}	Min. V_{OH}		I_{OL}, I_{OH}
LVCMOS33	3.3V	0.80	2.20	0.4	2.40	SL_LVCMOS33_8	±8
LVCMOS25	2.5V	0.70	1.70	0.4	2.00	SB_LVCMOS25_16	±16
						SB_LVCMOS25_12	±12
						SB_LVCMOS25_8 *	±8
						SB_LVCMOS25_4	±4
LVCMOS18	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_LVCMOS18_10	±10
						SB_LVCMOS18_8	±8
						SB_LVCMOS18_4 *	±4
						SB_LVCMOS18_2	±2
LVCMOS15	1.5V	35% VCCIO	65% VCCIO	25% VCCIO	75% VCCIO	SB_LVCMOS15_4	±4
						SB_LVCMOS15_2 *	±2
MDDR	1.8V	35% VCCIO	65% VCCIO	0.4	VCCIO–0.45	SB_MDDR10	±10
						SB_MDDR8	±8
						SB_MDDR4 *	±4
						SB_MDDR2	±2
SSTL2 (Class 2)	2.5V	VREF–0.180	VREF+0.180	0.35	VTT+0.430	SB_SSTL2_CLASS_2	±16.2
SSTL2 (Class 1)				0.54		SB_SSTL2_CLASS_1	±8.1
SSTL18 (Full)	1.8V	VREF–0.125	VREF+0.125	0.28	VTT+0.280	SB_SSTL18_FULL	±13.4
SSTL18 (Half)				VTT–0.475	VTT+0.475	SB_SSTL18_HALF	±6.7

NOTES:
SSTL2 and SSTL18 I/O standards require the VREF input pin, which is only available on the CB284 package and die-based products.

Programmable Input/Output (PIO) Block

Table 55 provides timing information for the logic in a Programmable Logic Block (PLB), which includes the paths shown in Figure 57 and Figure 58. The timing shown is for the LVCMOS25 I/O standard in all I/O banks. The iCEcube development software reports timing adjustments for other I/O standards.

Figure 57: **Programmable I/O (PIO) Pad-to-Pad Timing Circuit**

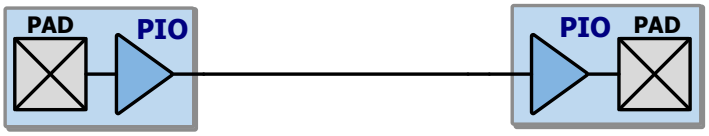


Figure 58: **Programmable I/O (PIO) Sequential Timing Circuit**

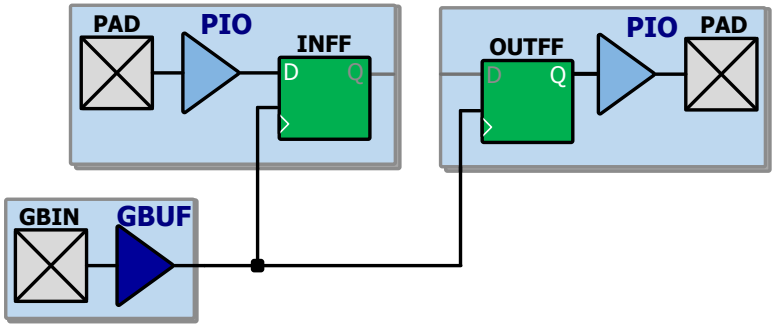


Table 55: **Typical Programmable Input/Output (PIO) Timing (LVCMOS25)**

Symbol	From	To	Device: iCE65	L01	L04, L08			Units
			Power/Speed Grad	–T	–L		–T	
			Nominal VCC	1.2 V	1.0 V	1.2 V	1.2 V	
			Description	Typ.	Typ.	Typ.	Typ.	
		Synchronous Output Paths						
t_{OCKO}	OUTFF clock input	PIO output	Delay from clock input on OUTFF output flip-flop to PIO output pad.	4.7	13.8	7.3	5.6	ns
t_{GBCKIO}	GBIN input	OUTFF clock input	Global Buffer Input (GBIN) delay, though Global Buffer (GBUF) clock network to clock input on the PIO OUTFF output flip-flop.	2.1	7.3	3.8	2.6	ns
		Synchronous Input Paths						
t_{SUPDIN}	PIO input	GBIN input	Setup time on PIO input pin to INFF input flip-flop before active clock edge on GBIN input, including interconnect delay.	0	0	0	0	ns
t_{HDPDIN}	GBIN input	PIO input	Hold time on PIO input to INFF input flip-flop after active clock edge on the GBIN input, including interconnect delay.	2.7	7.1	3.6	2.8	ns
		Pad to Pad						
t_{PADIN}	PIO input	Inter-connect	Asynchronous delay from PIO input pad to adjacent interconnect.	2.5	9.5	5.0	3.2	ns
t_{PADO}	Inter-connect	PIO output	Asynchronous delay from adjacent interconnect to PIO output pad including interconnect delay.	4.5	14.6	7.7	6.2	ns

Revision History

Version	Date	Description
2.42	30-MAR-2012	Changed company name. Updated Table 1
2.41	1-AUG-2011	Added VQ100 marking for NVCM programming.
2.4	13-MAY-2011	Added L01 CB121 package Figure 39. Added note "else VCCIO_1 draws current" to JTAG inputs TCK, TDI and TMS do not have the input pull-up resistor and must be tied off to GND when unused, Table 32. Input pin leakage current Table 49 split by bank. QN84 package drawing, Figure 35, added note "underside metal is at ground potential", increased thermal resistance. Added Marking Format and Thermal resistance to CB81 Packag Mechanical Drawing Figure 33. Added coplanarity specification to VQ100 Package Mechanical Drawing Figure 37
2.3	18-OCT-2010	Added L01 CB81 and L08 CB132 packages.
2.2.3	12-OCT-2010	Changed Figure 29: Application Processor Waveforms for SPI Peripheral Mode Configuration Process and Table 60 from 300 µs CRESET_B to 800 µs for iCE65L01/04 and 1200 µs for iCE65L08.
2.2.2	8-OCT-2010	Added iCE65L04 marking specification to Figure 47 CB196 Package Mechanical Drawing.
2.2.1	5-OCT-2010	Changed FSPI_SCK from 0.125 MHz to 1 MHz in SPI Peripheral Configuration Interface and in Table 60.
2.2	6-AUG-2010	Programmable Interconnect section removed.
2.1.1	26-MAY-2010	Switched labels on Figure 53 LVCMOS Output High, VCCIO = 1.8V with VCCIO = 2.5V.
2.1	15-MAR-2010	Added JTAG unused input tie off guideline. Added marking specification and thermal characteristics to package drawings. Added production datasheet for iCE65L01 with timing update, including QN84, VQ100 and CB132. Added NVCM shut-off on SPI configuration. Added non-standard VCCIO operating conditions. Increased the minimum voltage supply specification for LVCMOS33 to 3.14V in Table 48.
2.0.1	12-NOV-2009	Recommended Operation Conditions, Table 47, replaced junction with ambient.
2.0	14-SEPT-2009	Finalized production data sheet for iCE65L04 and iCE65L08. Improved SubLVDS input specification V_{ICM} in Table 52. CS63 and CC72 packages removed and placed in iCE DiCE KGD, Known Good Die datasheet. Added "IBIS Models for I/O Banks 0, 1, 2 and the SPI Bank". Added "Printed Circuit Board Layout Information".
1.5.1	13-JUL-2009	Updated the text in "SPI PROM Requirements" section. Minor label change in Figure 48.
1.5	20-JUN-2009	Updated timing information and added –T high-speed device option (affected Figure 2, Table 48, Table 54, Table 55, Table 56, and Table 61). Added support for 3.3V LVCMOS I/Os in I/O Bank 3 (affected Figure 7, Table 5, Table 7, Table 8, Table 47, Table 48, and Table 51). Added a section about the SPI Peripheral Configuration Interface and timing in Table 60. Added a warning that a Warm Boot operation can only jump to another configuration image that has Warm Boot disabled. Updated configuration image size and configuration time for the iCE65L02 in Table 27 and Table 58. Reduced the minimum voltage supply specification for LVCMOS33 to 2.7V in Table 48. Added information about which power rails can be disconnected without effecting the Power-On Reset (POR) circuit and clarified description of VPP_2V5 pin in Table 36. Added I/O characterization curves (Figure 52, Figure 53, and Figure 54). Minor changes to Figure 20 and Figure 21. Changed timing per Figures 54-58 and Tables 55-57.
1.4.4	25-MAR-2009	Clarified the voltage requirements for the VPP_2V5 pin in Table 36 and notes under Table 48.
1.4.3	9-MAR-2009	Removed volatile-only (-V) product offering from Figure 2. Corrected NC on ball V22, removed it for ball T22 on CB284 package (Figure 48).
1.4.2	27-FEB-2009	Updated Table 14, Table 23, Table 26, Table 30, Table 33, Table 35, and Table 46. Updated I/O Bank 3 information in Table 7 and Table 48.
1.4.1	24-FEB-2009	Based on characterization data, reduced 32KHz operating current by 40% in Table 1, Table 61, and Figure 1. Corrected that SSTL18 standards require VREF pin in Table 7. Correct ball numbers for GBIN4/GBIN5 for CS110 package.
1.4	9-FEB-2009	Added footprint and pinout information for the VQ100 Very-thin Quad Flat Package. Added footprint for iCE65L08 in CB196 (Figure 46) and added Table 43 showing the differences between the 'L04 and 'L08 in the CB196 package. Unified the package footprint nomenclature in the Package and Pinout Information section. Added note to Global Buffer Inputs that the differential clock direct input is not available on the CB132 package. Added tables showing the ball/pin number for various control functions, by package (Table 14, Table 23, Table 26, Table 30, and Table 33). Corrected the GBIN/GBUF designations. GBIN4 and GBIN5 were swapped as were GBIN6 and GBIN7. This change affected all pinout tables and footprint diagrams. Updated and corrected "Differential Global Buffer Input." Tested and corrected the clock-enable and reset connections between global buffers and various resources (Table 11, Table 12, and Table 13). Added "Automatic Global Buffer Insertion, Manual Insertion." Added "Die Cross Reference" section. Improved industrial temperature range by lowering

Lattice Semiconductor Corporation
5555 N.E. Moore Court
Hillsboro, Oregon 97124-6421
United States of America

Tel: +1 503 268 8000
Fax: +1 503 268 8347