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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 960 |
| Number of Logic Elements/Cells | 7680 |
| Total RAM Bits | 131072 |
| Number of I/O | 92 |
| Number of Gates | - |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | - |
| Supplier Device Package | 110-WLCSP |
| Purchase URL | https://www.e-xfl.com/product-detail/lattice-semiconductor/ice65l08f-tcs110i |

## Programmable Logic Block (PLB)

Generally, a logic design for an iCE65 component is created using a high-level hardware description language such as Verilog or VHDL. The Lattice Semiconductor development software then synthesizes the high-level description into equivalent functions built using the programmable logic resources within each iCE65 device. Both sequential and combinational functions are constructed from an array of Programmable Logic Blocks (PLBs). Each PLB contains eight Logic Cells (LCs), as pictured in Figure 4, and share common control inputs, such as clocks, reset, and enable controls.

PLBs are connected to one another and other logic functions using the rich Programmable Interconnect resources.

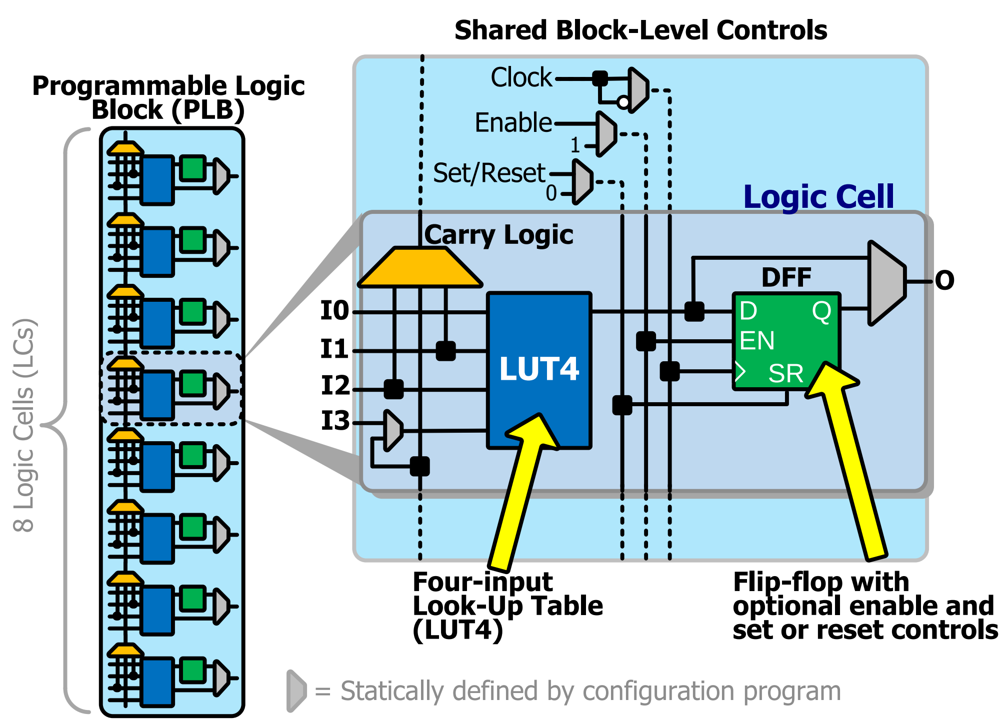
### Logic Cell (LC)

Each iCE65 device contains thousands of Logic Cells (LCs), as listed in Table 1. Each Logic Cell includes three primary logic elements, shown in Figure 4.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, of up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

The output from a Logic Cell is available to all inputs to all eight Logic Cells within the Programmable Logic Block. Similarly, the Logic Cell output feeds into fabric to connect to other features on the iCE65 device.

***Figure 4:* Programmable Logic Block and Logic Cell**



Each flip-flop has an additional control that defines its set or reset behavior. As defined in the configuration image, the control defines whether the set or reset operation is synchronized to the active CLK clock edge or whether it is completely asynchronous.

- The SB_DFFR and SB_DFFS primitives are asynchronously controlled, solely by the SR input. If the SR input is High, then an SB_DFFR primitive is asynchronously reset and an SB_DFFS primitive is asynchronously set.
- The SB_DFFSR and SB_DFFRSS primitives are synchronously controlled by both the SR input and the clock input. If the SR input is High at a rising edge of the clock input, then an SB_DFFSR primitive is synchronously reset and an SB_DFFSS primitive is synchronously set.

The LUT4 output or the flip-flop output then connects to the programmable interconnect.

Because of the shared control signals, the design software can pack flip-flops with common control inputs into a single PLB block, as described by Table 4. There are eight total packing options.

**Table 4: Flip-flop Packing/Sharing within a PLB**

| Group | Active Clock Edge | Clock Enable | Set or Reset Control (Sync. or Async) |
|---|---|---|---|
| **1** | ↑ | None (always enabled) | None |
| **2** | ↓ | | |
| **3** | ↑ | | PLB set/reset control |
| **4** | ↓ | | |
| **5** | ↑ | Selective (controlled by PLB clock enable) | None |
| **6** | ↓ | | |
| **7** | ↑ | | PLB set/reset control |
| **8** | ↓ | | |

For detailed flip-flop internal timing, see Table 54.

## Carry Logic

The dedicated Carry Logic within each Logic Cell primarily accelerates and improves the efficiency of arithmetic logic such as adders, accumulators, subtracters, incrementers, decrementers, counters, ALUs, and comparators. The Carry Logic also supports wide combinational logic functions.

$$COUT = I1 \bullet I2 + CIN \bullet I1 + CIN \bullet I2 \qquad \text{[Equation 1]}$$

Equation 1 and Figure 5 describe the Carry Logic structure within a Logic Cell. The Carry Logic shares inputs with the associated Look-Up Table (LUT4). The LUT4's I1 and I2 inputs directly feed the Carry Logic; inputs I0 and I3 do not. A signal cascades between Logic Cells within the Programmable Logic Block. The carry input from the previous adjacent Logic Cell optionally provides an alternate input to the LUT4 function, supplanting the I3 input.

### *Low-Power Disable*

To save power and prevent unnecessary signal switching, the Carry Logic function within a Logic Cell is disabled if not used. The output of a Logic Cell's Carry Logic is forced High.

### *PLB Carry Input and Carry Output Connections*

As shown in Figure 5, each Programmable Logic Block has a carry input signal that can be initialized High, Low, or come from the carry output signal from PLB immediately below.

Similarly, the Carry Logic output from the Programmable Logic Block connects to the PLB immediately above, which allows the Carry Logic to span across multiple PLBs in a column. As shown in Figure 6, the Carry Logic chain can be tapped mid-way through a chain or a PLB by feeding the value through a LUT4 function.

### *Adder Example*

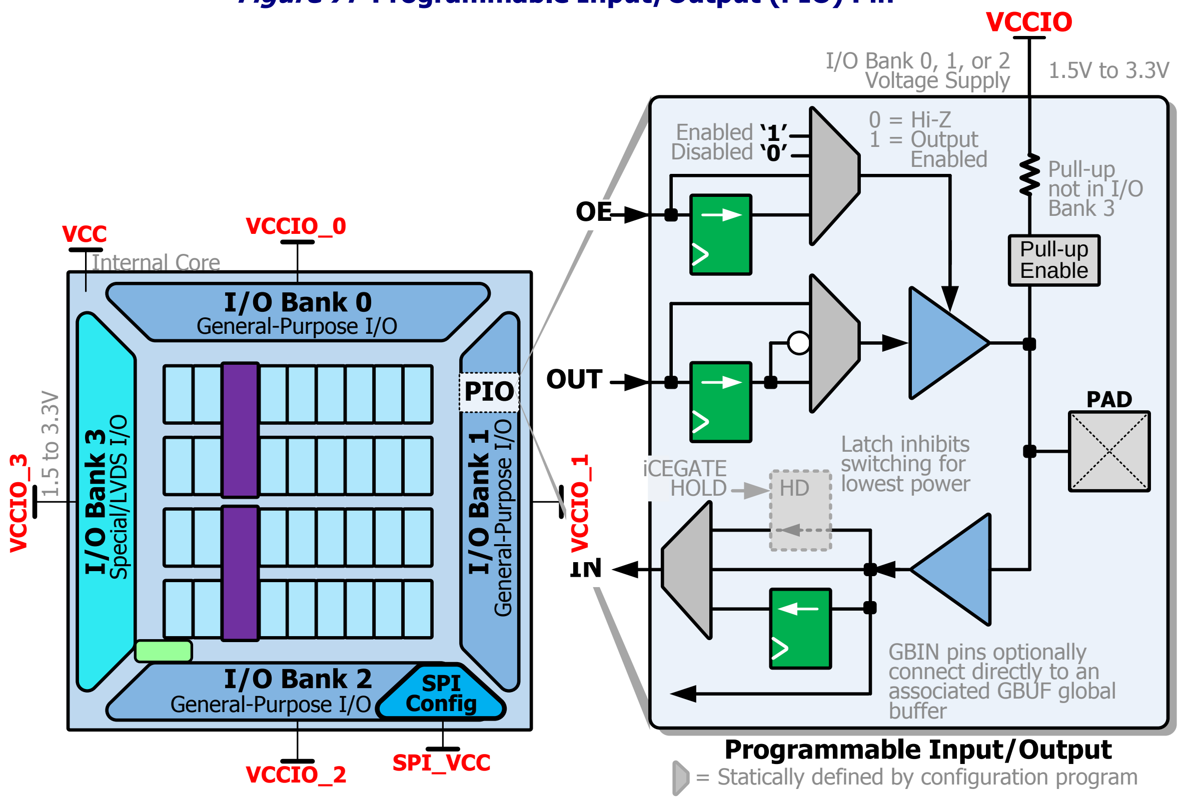
Figure 6 shows an example design that uses the Carry Logic. The example is a 2-bit adder, which can be expanded into an adder of arbitrary size. The LUT4 function within a Logic Cell is programmed to calculate the sum of the two input values and the carry input, `A[i] + B[i] + CARRY_IN[i-1] = SUM[i]`.

## Programmable Input/Output Block (PIO)

Programmable Input/Output (PIO) blocks surround the periphery of the device and connect external components to the Programmable Logic Blocks (PLBs) and RAM4K blocks via programmable interconnect. Individual PIO pins are grouped into one of four I/O banks, as shown in Figure 7. I/O Bank 3 has additional capabilities, including LVDS differential I/O and the ability to interface to Mobile DDR memories.

Figure 7 also shows the logic within a PIO pin. When used in an application, a PIO pin becomes a signal input, an output, or a bidirectional I/O pin with a separate direction control input.

***Figure 7:* Programmable Input/Output (PIO) Pin**




### I/O Banks

PIO blocks are organized into four separate I/O banks, each with its own voltage supply input, as shown in Table 5. The voltage applied to the VCCIO pin on a bank defines the I/O standard used within the bank. Table 50 and Table 51 describe the I/O drive capabilities and switching thresholds by I/O standard. On iCE65L04 and iCE65L08 devices, I/O Bank 3, along the left edge of the die, is different than the others and supports specialized I/O standards.

#### *I/O Bank Voltage Supply Inputs Support Different I/O Standards*

Because each I/O bank has its own voltage supply, iCE65 components become the ideal bridging device between different interface standards. For example, the iCE65 device allows a 1.8V-only processor to interface cleanly with a 3.3V bus interface. The iCE65 device replaces external voltage translators.

**Table 5: Supported Voltages by I/O Bank**

| Bank | Device Edge | Supply Input | 3.3V | 2.5V | 1.8V | 1.5V |
|---|---|---|---|---|---|---|
| **0** | Top | VCCIO_0 | Yes | Yes | Yes | Outputs only |
| **1** | Right | VCCIO_1 | Yes | Yes | Yes | Outputs only |
| **2** | Bottom | VCCIO_2 | Yes | Yes | Yes | Outputs only |
| **3** | Left | VCCIO_3 | Yes | Yes | Yes | iCE65L01: Outputs only<br>iCE65L04/08: Yes |
| **SPI** | Bottom Right | SPI_VCC | Yes | Yes | Yes | No |

## Global Routing Resources

### *Global Buffers*

Each iCE65 component has eight global buffer routing connections, illustrated in Figure 14. There are eight high-drive buffers, connected to the eight low-skew, global lines. These lines are designed primarily for clock distribution but are also useful for other high-fanout signals such as set/reset and enable signals. The global buffers originate either from the Global Buffer Inputs (GBINx) or from programmable interconnect. The associated GBINx pin represents the best pin to drive a global buffer from an external source. However, the application with an iCE65 FPGA can also drive a global buffer via any other PIO pin or from internal logic using the programmable interconnect.

If not used in an application, individual global buffers are turned off to save power.

**Figure 14: High-drive, Low-skew, High-fanout Global Buffer Routing Resources**

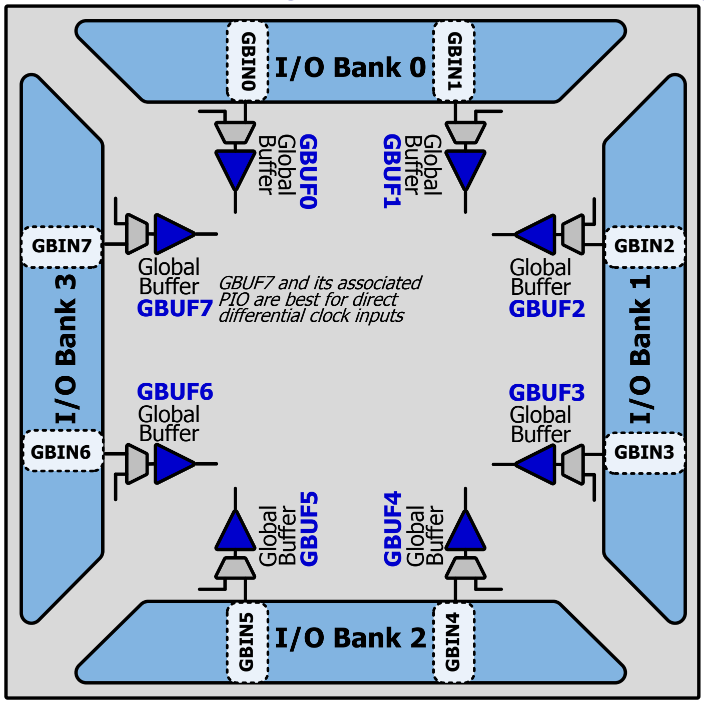



Table 11 lists the connections between a specific global buffer and the inputs on a Programmable Logic Block (PLB). All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

**Table 11: Global Buffer (GBUF) Connections to Programmable Logic Block (PLB)**

| Global Buffer | LUT Inputs | Clock | Clock Enable | Reset |
|---|---|---|---|---|
| **GBUF0** | Yes, any 4 of 8 GBUF buffers | Yes | Yes | No |
| **GBUF1** | | Yes | No | Yes |
| **GBUF2** | | Yes | Yes | No |
| **GBUF3** | | Yes | No | Yes |
| **GBUF4** | | Yes | Yes | No |
| **GBUF5** | | Yes | No | Yes |
| **GBUF6** | | Yes | Yes | No |
| **GBUF7** | | Yes | No | Yes |

Table 12 and Table 13 list the connections between a specific global buffer and the inputs on a Programmable I/O (PIO) pair. Although there is no direct connection between a global buffer and a PIO output, such a connection is possible by first connecting through a PLB LUT4 function. Again, all global buffers optionally drive all clock inputs. However, even-numbered global buffers optionally drive the clock-enable input on a PIO pair.

The PIO clock enable connect is different between the iCE65L01/iCE65L04 and iCE65L08.

**Table 12: iCE65L01 & iCE65L04: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

| Global Buffer | Output Connections | Input Clock | Output Clock | Clock Enable |
|---|---|---|---|---|
| **GBUF0** | No (connect through PLB LUT) | Yes | Yes | No |
| **GBUF1** | | Yes | Yes | Yes |
| **GBUF2** | | Yes | Yes | No |
| **GBUF3** | | Yes | Yes | Yes |
| **GBUF4** | | Yes | Yes | No |
| **GBUF5** | | Yes | Yes | Yes |
| **GBUF6** | | Yes | Yes | No |
| **GBUF7** | | Yes | Yes | Yes |

**Table 13: iCE64L08: Global Buffer (GBUF) Connections to Programmable I/O (PIO) Pair**

| Global Buffer | Output Connections | Input Clock | Output Clock | Clock Enable |
|---|---|---|---|---|
| **GBUF0** | No (connect through PLB LUT) | Yes | Yes | Yes |
| **GBUF1** | | Yes | Yes | No |
| **GBUF2** | | Yes | Yes | Yes |
| **GBUF3** | | Yes | Yes | No |
| **GBUF4** | | Yes | Yes | Yes |
| **GBUF5** | | Yes | Yes | No |
| **GBUF6** | | Yes | Yes | Yes |
| **GBUF7** | | Yes | Yes | No |

### *Global Buffer Inputs*

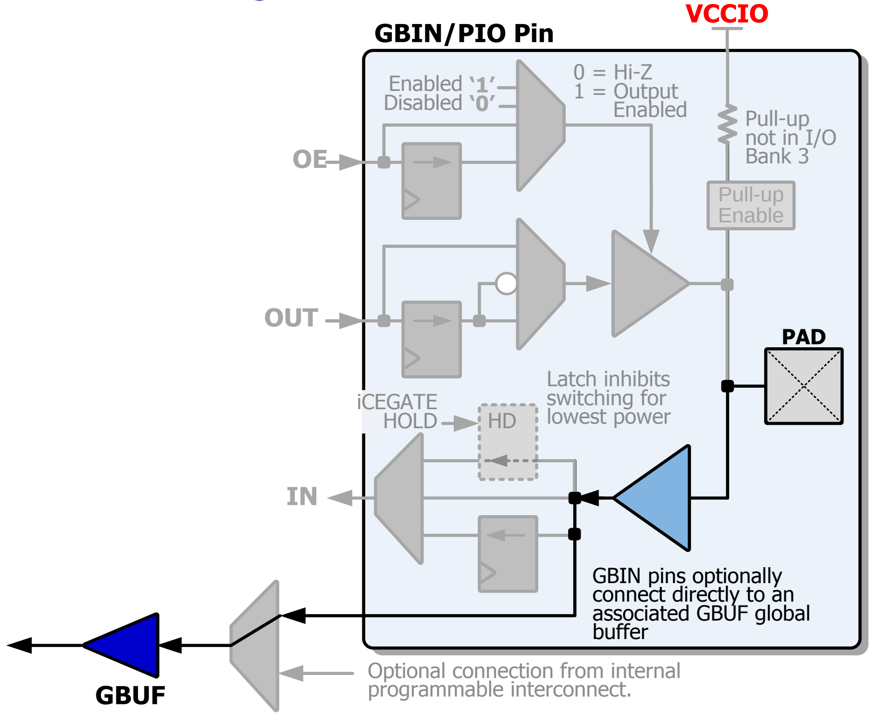
The iCE65 component has eight specialized GBIN/PIO pins that are optionally direct inputs to the global buffers, offering the best overall clock characteristics. As shown in Figure 15, each GBIN/PIO pin is a full-featured I/O pin but also provides a direct connection to its associated global buffer. The direct connection to the global buffer bypasses the iCEgate input-blocking latch and other PIO input logic. These special PIO pins are allocated two to an I/O Bank, a total of eight. These pins are labeled GBIN0 through GBIN7, as shown in Figure 14 and the pin locations for each GBIN input appear in Table 14.

**Table 14: Global Buffer Input Ball/Pin Number by Package**

| Global Buffer Input (GBIN) | I/O Bank | VQ100 | CB132 | 'L04 CB196 | 'L08 CB196 | CB284 |
|---|---|---|---|---|---|---|
| **GBIN0** | 0 | 90 | A6 | A7 | A7 | E10 |
| **GBIN1** | | 89 | A7 | E7 | E7 | E11 |
| **GBIN2** | 1 | 63 | G14 | F10 | F10 | L18 |
| **GBIN3** | | 62 | F14 | G12 | G12 | K18 |
| **GBIN4** | 2 | 34 | P8 | L7 | N8 | V12 |
| **GBIN5** | | 33 | P7 | P5 | M7 | V11 |
| **GBIN6** | 3 | 15 | H1 | H1 | H1 | M5 |
| **GBIN7** | | 13 | G1 | G1 | H3 | L5 |

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

**Figure 15: GBIN/PIO Pin**




### *Differential Global Buffer Input*

All eight global buffer inputs support single-ended I/O standards such as LVCMOS. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct SubLVDS, LVDS, or LVPECL differential clock input, as shown in Figure 16. The GBIN7 and its associated differential I/O pad accept a differential clock signal. A 100 Ω termination resistor is required across the two pads. Optionally, swap the outputs from the LVDS or LVPECL clock driver to invert the clock as it enters the iCE65 device.

**Figure 16: LVDS or LVPECL Clock Input**

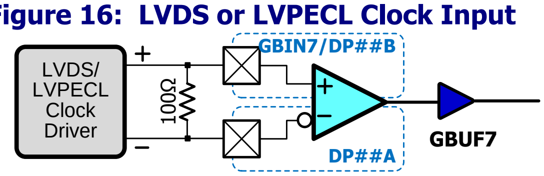



Table 15 lists the pin or ball numbers for the differential global buffer input by package style. Although this differential input is the only one that connects directly to a global buffer, other differential inputs can connect to a global buffer using general-purpose interconnect, with slightly more signal delay.

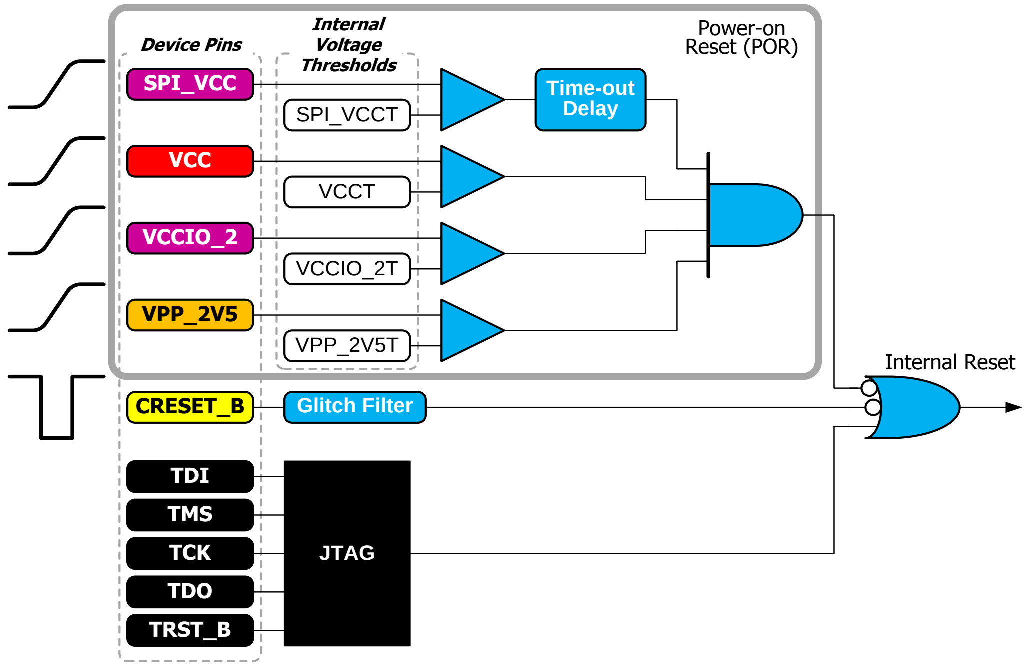
***Table 15:* Differential Global Buffer Input Ball/Pin Number by Package**

| Differential Global Buffer Input (GBIN) | I/O Bank | VQ100 | CB132 | 'L04 CB196 | 'L08 CB196 | CB284 |
|---|---|---|---|---|---|---|
| **GBIN7/DPxxB** | 3 | 13 | N/A | G1 | H3 | L5 |
| **DPxxA** | | 12 | N/A | G2 | H4 | L3 |

The differential global buffer input is not available for iCE65 devices in the CB132 package. This restriction is an artifact of the pin compatibility between the CB132 and CB284 package.

Note the clock differences between the iCE65L04 and iCE65L08 in the CB196 package.

**Figure 22: iCE65 Internal Reset Circuitry**




### *Power-On Reset (POR)*

The Power-on Reset (POR) circuit monitors specific voltage supply inputs and holds the device in reset until all the relevant supplies exceed the internal voltage thresholds. The SPI_VCC supply also has an additional time-out delay to allow an attached SPI serial PROM to power up properly. Table 24 shows the POR supply inputs. The Nonvolatile Configuration Memory (NVCM) requires that the VPP_2V5 supply be connected, even if the application does not use the NVCM.

***Table 24:* Power-on Reset (POR) Voltage Resources**

| Supply Rail | iCE65 Production Devices |
|---|---|
| **VCC** | Yes |
| **SPI_VCC** | Yes |
| **VCCIO_1** | No |
| **VCCIO_2** | Yes |
| **VPP_2V5** | Yes |

### *CRESET_B Pin*

The CRESET_B pin resets the iCE65 internal logic when Low.

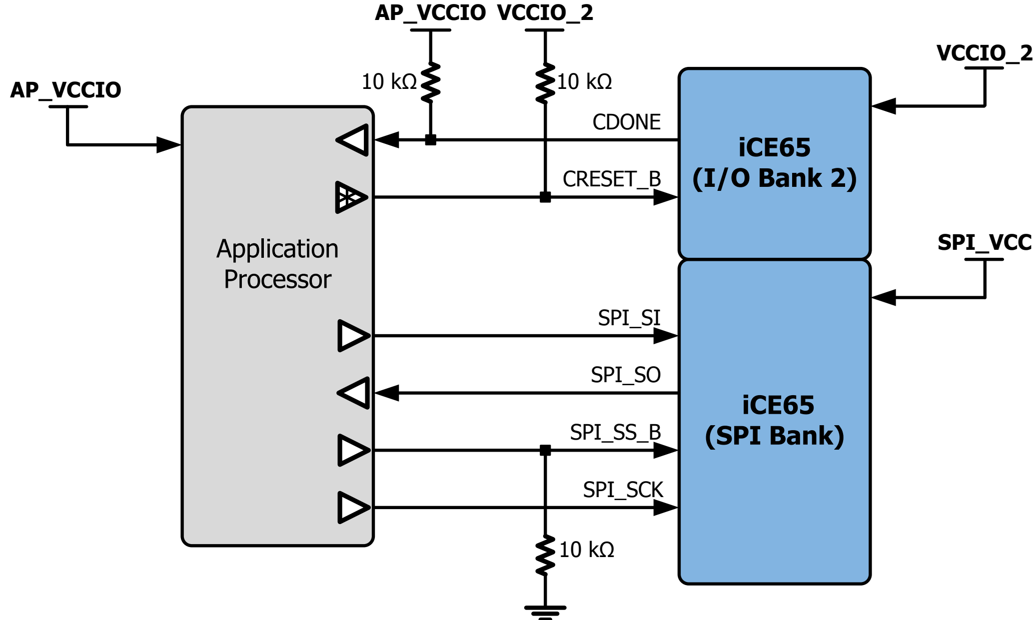
### *JTAG Interface*

Specific command sequences also reset the iCE65 internal logic.

## SPI Master Configuration Interface

All iCE65 devices, including those with NVCM, can be configured from an external, commodity SPI serial Flash PROM, as shown in Figure 23. The SPI configuration interface is essentially its own independent I/O bank, powered by the VCC_SPI supply input. Presently, most commercially-available SPI serial Flash PROMs require a 3.3V supply.

Figure 28: iCE65 SPI Peripheral Configuration Interface




The SPI control signals are defined in Table 25.

Table 29: SPI Peripheral Configuration Interface Pins (SPI_SS_B Low when CRESET_B Released)

| Signal Name | Direction | iCE65 I/O Supply | Description |
|---|---|---|---|
| CDONE | AP ← iCE65 | VCCIO_2 | Configuration Done output from iCE65. Connect to a 10kΩ pull-up resistor to the application processor I/O voltage, AP_VCC. |
| CRESET_B | AP → iCE65 | | Configuration Reset input on iCE65. Typically driven by AP using an open-drain driver, which also requires a 10kΩ pull-up resistor to VCCIO_2. |
| SPI_VCC | Supply | SPI_VCC | SPI Flash PROM voltage supply input. |
| SPI_SI | AP → iCE65 | | SPI Serial Input to the iCE65 FPGA, driven by the application processor. |
| SPI_SO | AP ← iCE65 | | SPI Serial Output from CE65 device to the application processor. Not actually used during SPI peripheral mode configuration but required if the SPI interface is also used to program the NVCM. |
| SPI_SS_B | AP → iCE65 | | SPI Slave Select output from the application processor. Active Low. Optionally hold Low prior to configuration using a 10kΩ pull-down resistor to ground. |
| SPI_SCK | AP → iCE65 | | SPI Slave Clock output from the application processor. |

After configuration, the SPI port pins are available to the user-application as additional PIO pins, supplied by the SPI_VCC input voltage, essentially providing a fifth "mini" I/O bank.

### Enabling SPI Configuration Interface

The optional 10 kΩ pull-down resistor on the SPI_SS_B signal ensures that the iCE65 FPGA powers up in the SPI peripheral mode. Optionally, the application processor drives the SPI_SS_B pin Low when CRESET_B is released, forcing the iCE65 FPGA into SPI peripheral mode.

### SPI Peripheral Configuration Process

Figure 29 illustrates the interface timing for the SPI peripheral mode and Figure 30 outlines the resulting configuration process. The actual timing specifications appear in Table 60. The application processor (AP) begins by driving the iCE65 CRESET_B pin Low, resetting the iCE65 FPGA. Similarly, the AP holds the iCE65's SPI_SS_B pin Low. The AP must hold the CRESET_B pin Low for at least 200 ns. Ultimately, the AP either releases the CRESET_B pin and allows it to float High via the 10 kΩ pull-up resistor to VCCIO_2 or drives CRESET_B High. The iCE65 FPGA enters SPI peripheral mode when the CRESET_B pin returns High while the SPI_SS_B pin is Low.

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| **PIO2** | B14 | PIO | 2 |
| **PIO2/CBSEL0** | B15 | PIO | 2 |
| **PIO2/CBSEL1** | A20 | PIO | 2 |
| **VCCIO_2** | A17 | PIO | 2 |
| **GBIN6/PIO3** | A9 | GBIN | 3 |
| **GBIN7/PIO3** | A8 | GBIN | 3 |
| **PIO3** | A1 | PIO | 3 |
| **PIO3** | A2 | PIO | 3 |
| **PIO3** | A3 | PIO | 3 |
| **PIO3** | A4 | PIO | 3 |
| **PIO3** | A5 | PIO | 3 |
| **PIO3** | A10 | PIO | 3 |
| **PIO3** | A11 | PIO | 3 |
| **PIO3** | A12 | PIO | 3 |
| **PIO3** | B1 | PIO | 3 |
| **PIO3** | B2 | PIO | 3 |
| **PIO3** | B3 | PIO | 3 |
| **PIO3** | B4 | PIO | 3 |
| **PIO3** | B5 | PIO | 3 |
| **PIO3** | B7 | PIO | 3 |
| **PIO3** | B8 | PIO | 3 |
| **PIO3** | B9 | PIO | 3 |
| **VCCIO_3** | B6 | VCCIO | 3 |
| **PIOS/SPI_SO** | B17 | SPI | SPI |
| **PIOS/SPI_SI** | A22 | SPI | SPI |
| **PIOS/SPI_SCK** | A23 | SPI | SPI |
| **PIOS/SPI_SS_B** | B18 | SPI | SPI |
| **SPI_VCC** | A24 | SPI | SPI |
| **GND** | A6 | GND | GND |
| **GND** | A18 | GND | GND |
| **GND** | A30 | GND | GND |
| **GND** | B33 | GND | GND |
| **VCC** | A7 | VCC | VCC |
| **VCC** | A15 | VCC | VCC |
| **VCC** | A28 | VCC | VCC |
| **VCC** | B28 | VCC | VCC |
| **VPP_2V5** | A36 | VPP | VPP |
| **VPP_FAST** | A37 | VPP | VPP |

## CB121 Chip-Scale Ball-Grid Array

The CB121 package is a chip-scale, fully-populated, ball-grid array with 0.5 mm ball pitch.

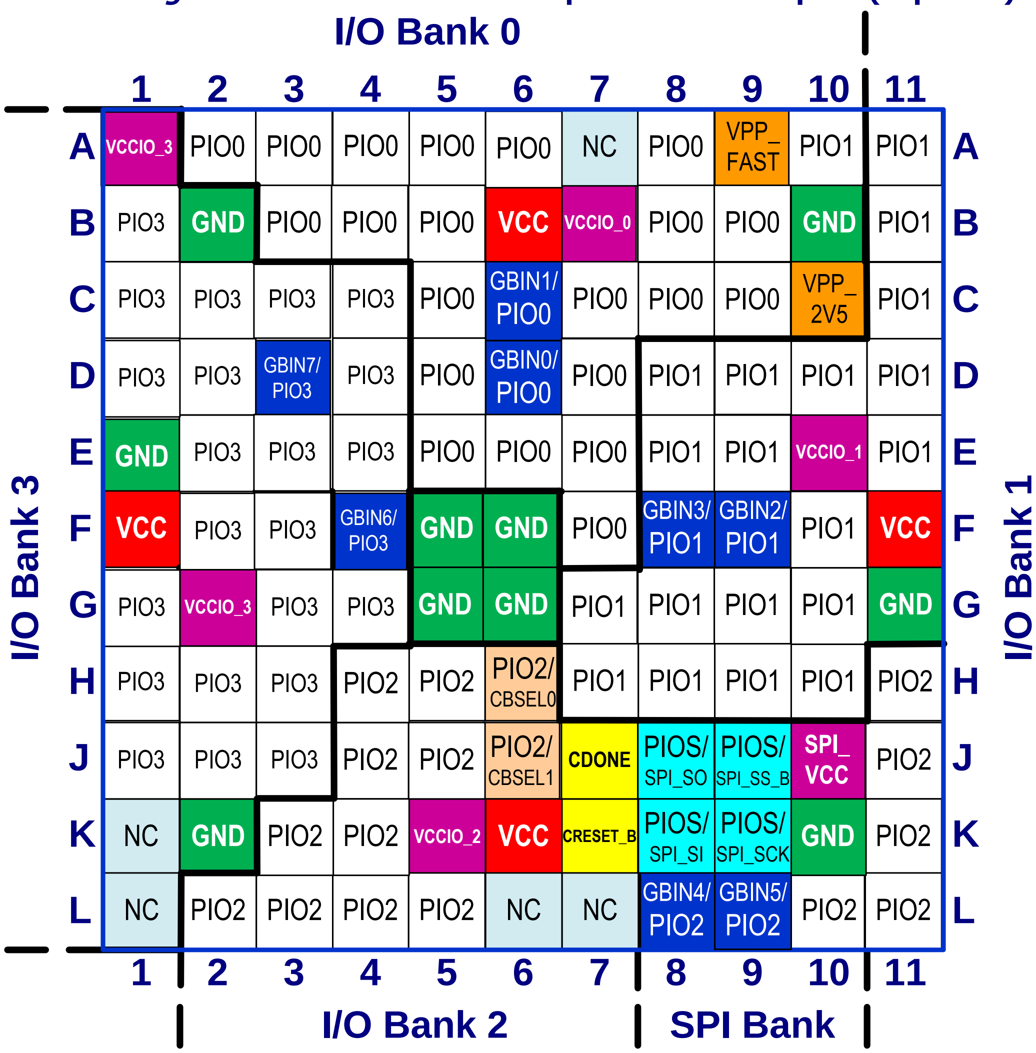
### *Footprint Diagram*

Figure 39 shows the iCE65L01 chip-scale BGA footprint for the 6 x 6 mm CB121 package.

Also see Table 40 for a complete, detailed pinout for the 121-ball chip-scale BGA packages.

The signal pins are also grouped into the four I/O Banks and the SPI interface.

***Figure 39:* iCE65L01 CB121 Chip-Scale BGA Footprint (Top View)**




### *Pinout Table*

Table 40 provides a detailed pinout table for the iCE65L01 in the CB121 chip-scale BGA package. Pins are generally arranged by I/O bank, then by ball function.

***Table 40:* iCE65L01 CB121 Chip-scale BGA Pinout Table**

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| GBIN0/PIO0 | D6 | GBIN | 0 |
| GBIN1/PIO0 | C6 | GBIN | 0 |
| PIO0 | A2 | PIO | 0 |
| PIO0 | A3 | PIO | 0 |
| PIO0 | A4 | PIO | 0 |

***Figure 43:*** **iCE65L08 CB132 Chip-Scale BGA Footprint (Top View)**

I/O Bank 0

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | GBIN0/ PIO0 | GBIN1/ PIO0 | VCCIO_0 | GND | PIO0 | PIO0 | PIO0 | VPP_ FAST | VPP_ 2V5 | A |
| B | PIO3/ DP00A | | | | | | | | | | | | | PIO1 | B |
| C | PIO3/ DP00B | | PIO3/ DP01A | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | | PIO1 | C |
| D | PIO3/ DP03A | | PIO3/ DP01B | PIO3/ DP02A | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO0 | PIO1 | | PIO1 | D |
| E | PIO3/ DP03B | | VCCIO_3 | PIO3/ DP02B | | | | | | | PIO1 | PIO1 | | PIO1 | E |
| F | GND | | PIO3/ DP04B | PIO3/ DP04A | | VCCIO_0 | GND | VCC | VCCIO_1 | | PIO1 | PIO1 | | GBIN3/ PIO1 | F |
| G | GBIN7/ DP05B | | PIO3/ DP05A | PIO3/ DP11B | | VCC | GND | GND | GND | | PIO1 | PIO1 | | GBIN2/ PIO1 | G |
| H | GBIN6/ DP06A | | PIO3/ DP06B | PIO3/ DP11A | | GND | GND | GND | VCC | | PIO1 | PIO1 | | VCCIO_1 | H |
| J | PIO3/ DP07B | | PIO3/ DP07A | VCC | | VCCIO_3 | VCC | GND | VCCIO_2 | | PIO1 | PIO1 | | GND | J |
| K | VCCIO_3 | | PIO3/ DP08A | PIO3/ DP08B | | | | | | | PIO1 | PIO1 | | PIO1 | K |
| L | PIO3/ DP09A | | GND | PIO2 | PIO2 | PIO2 | PIO2 | PIO2 | PIO2/ CBSEL0 | CRESET_B | SPI_ VCC | TCK | | PIO1 | L |
| M | PIO3/ DP09B | | PIO2 | PIO2 | VCCIO_2 | PIO2 | PIO2 | PIO2 | PIO2 | CDONE | PIOS/ SPI_SO | TDI | | TRST_B | M |
| N | PIO3/ DP10A | | | | | | | | | | | | | TDO | N |
| P | PIO3/ DP10B | PIO2 | PIO2 | PIO2 | PIO2 | GND | GBIN5/ PIO2 | GBIN4/ PIO2 | PIO2 | PIO2/ CBSEL1 | PIOS/ SPI_SI | PIOS/ SPI_SCK | PIOS/ SPI_SS_B | TMS | P |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

I/O Bank 3

I/O Bank 1

SPI Bank

I/O Bank 2

### Pinout Table

Table 41 provides a detailed pinout table for the CB132 package. Pins are generally arranged by I/O bank, then by ball function. The table also highlights the differential I/O pairs in I/O Bank 3.

**Table 41: iCE65 CB132 Chip-scale BGA Pinout Table**

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| **GBIN0/PIO0** | iCE65L01: A7<br>iCE65L04/L08: A6 | GBIN | 0 |
| **GBIN1/PIO0** | iCE65L01: A6<br>iCE65L04/08: A7 | GBIN | 0 |
| **PIO0** | A1 | PIO | 0 |
| **PIO0** | A2 | PIO | 0 |
| **iCE65L01: (NC)<br>iCE65L04/L08: PIO0** | A3 | iCE65L01: (NC)<br>iCE65L04: PIO0 | 0 |
| **PIO0** | A4 | PIO | 0 |
| **PIO0** | A5 | PIO | 0 |
| **PIO0** | A10 | PIO | 0 |
| **iCE65L01: (NC)<br>iCE65L04/L08: PIO0** | A11 | iCE65L01: (NC)<br>iCE65L04: PIO0 | 0 |
| **PIO0** | A12 | PIO | 0 |
| **PIO0** | C10 | PIO | 0 |
| **PIO0** | C11 | PIO | 0 |
| **PIO0** | C12 | PIO | 0 |
| **PIO0** | C4 | PIO | 0 |
| **PIO0** | C5 | PIO | 0 |
| **PIO0** | C6 | PIO | 0 |
| **PIO0** | C7 | PIO | 0 |
| **PIO0** | C8 | PIO | 0 |
| **PIO0** | C9 | PIO | 0 |
| **PIO0** | D5 | PIO | 0 |
| **PIO0** | D6 | PIO | 0 |
| **PIO0** | D7 | PIO | 0 |
| **PIO0** | D8 | PIO | 0 |
| **PIO0** | D9 | PIO | 0 |
| **PIO0** | D10 | PIO | 0 |
| **PIO0** | D11 | PIO | 0 |
| **VCCIO_0** | A8 | VCCIO | 0 |
| **VCCIO_0** | F6 | VCCIO | 0 |
| **GBIN2/PIO1** | G14 | GBIN | 1 |
| **GBIN3/PIO1** | F14 | GBIN | 1 |
| **PIO1** | B14 | PIO | 1 |
| **PIO1** | C14 | PIO | 1 |
| **PIO1** | D12 | PIO | 1 |
| **PIO1** | D14 | PIO | 1 |
| **PIO1** | E11 | PIO | 1 |
| **PIO1** | E12 | PIO | 1 |
| **PIO1** | E14 | PIO | 1 |
| **PIO1** | F11 | PIO | 1 |
| **PIO1** | F12 | PIO | 1 |
| **PIO1** | G11 | PIO | 1 |
| **PIO1** | G12 | PIO | 1 |
| **PIO1** | H11 | PIO | 1 |

| Ball Function | Ball Number | Pin Type | Bank |
|---|---|---|---|
| **PIO2 (◆)** | ***iCE65L04:*** N8<br>***iCE65L08:*** L7 | PIO | 2 |
| **PIO2** | N9 | PIO | 2 |
| **PIO2** | N11 | PIO | 2 |
| **PIO2** | N12 | PIO | 2 |
| **PIO2** | N13 | PIO | 2 |
| **PIO2** | P1 | PIO | 2 |
| **PIO2** | P2 | PIO | 2 |
| **PIO2** | P3 | PIO | 2 |
| **PIO2** | P4 | PIO | 2 |
| **PIO2** | P7 | PIO | 2 |
| **PIO2** | P8 | PIO | 2 |
| **PIO2** | P9 | PIO | 2 |
| **PIO2/CBSEL0** | L9 | PIO | 2 |
| **PIO2/CBSEL1** | P10 | PIO | 2 |
| **VCCIO_2** | J9 | VCCIO | 2 |
| **VCCIO_2** | M5 | VCCIO | 2 |
| **VCCIO_2** | N10 | VCCIO | 2 |
| **PIO3/DP00A** | C1 | DPIO | 3 |
| **PIO3/DP00B** | B1 | DPIO | 3 |
| **PIO3/DP01A** | D3 | DPIO | 3 |
| **PIO3/DP01B** | C3 | DPIO | 3 |
| **PIO3/DP02A** | D1 | DPIO | 3 |
| **PIO3/DP02B** | D2 | DPIO | 3 |
| **PIO3/DP03A (◆)** | ***iCE65L04:*** E1<br>***iCE65L08:*** E2 | DPIO | 3 |
| **PIO3/DP03B (◆)** | ***iCE65L04:*** E2<br>***iCE65L04:*** E1 | DPIO | 3 |
| **PIO3/DP04A** | D4 | DPIO | 3 |
| **PIO3/DP04B** | E4 | DPIO | 3 |
| **PIO3/DP05A (◆)** | ***iCE65L04:*** F3<br>***iCE65L08:*** F4 | DPIO | 3 |
| **PIO3/DP05B (◆)** | ***iCE65L04:*** F4<br>***iCE65L08:*** F3 | DPIO | 3 |
| **PIO3/DP06A** | F5 | DPIO | 3 |
| **PIO3/DP06B** | E5 | DPIO | 3 |
| **PIO3/DP07A (◆)** | ***iCE65L04:*** G2<br>***iCE65L08:*** H4 | DPIO | 3 |
| **GBIN7/PIO3/DP07B (◆)** | ***iCE65L04:*** G1<br>***iCE65L08:*** H3 | GBIN | 3 |
| **GBIN6/PIO3/DP08A** | H1 | GBIN | 3 |
| **PIO3/DP08B** | H2 | DPIO | 3 |
| **PIO3/DP09A** | G3 | DPIO | 3 |
| **PIO3/DP09B** | G4 | DPIO | 3 |
| **PIO3/DP10A** | J1 | DPIO | 3 |
| **PIO3/DP10B** | J2 | DPIO | 3 |
| **PIO3/DP11A (◆)** | ***iCE65L04:*** H4<br>***iCE65L08:*** G1 | DPIO | 3 |
| **PIO3/DP11B (◆)** | ***iCE65L04:*** H3<br>***iCE65L08:*** G2 | DPIO | 3 |
| **PIO3/DP12A** | K2 | DPIO | 3 |
| **PIO3/DP12B** | J3 | DPIO | 3 |

| Ball Function | Ball Number | Pin Type by Device | | Bank | CB132 Ball Equivalent |
|---|---|---|---|---|---|
| | iCE65L04 iCE65L08 | iCE65L04 | iCE65L08 | | |
| VCCIO_3 | J7 | VCCIO | VCCIO | 3 | E3 |
| VCCIO_3 | K3 | VCCIO | VCCIO | 3 | — |
| VCCIO_3 | N10 | VCCIO | VCCIO | 3 | J6 |
| VCCIO_3 | P5 | VCCIO | VCCIO | 3 | K1 |
| VCCIO_3 | R3 | VCCIO | VCCIO | 3 | — |
| VREF | M1 | VREF | VREF | 3 | — |
| PIOS/SPI_SO | T15 | SPI | SPI | SPI | M11 |
| PIOS/SPI_SI | V15 | SPI | SPI | SPI | P11 |
| PIOS/SPI_SCK | V16 | SPI | SPI | SPI | P12 |
| PIOS/SPI_SS_B | V17 | SPI | SPI | SPI | P13 |
| SPI_VCC | R15 | SPI | SPI | SPI | L11 |
| GND | C12 | GND | GND | GND | — |
| GND | E13 | GND | GND | GND | A9 |
| GND | J3 | GND | GND | GND | — |
| GND | K5 | GND | GND | GND | F1 |
| GND | K11 | GND | GND | GND | F7 |
| GND | L11 | GND | GND | GND | G7 |
| GND | L12 | GND | GND | GND | G8 |
| GND | L13 | GND | GND | GND | G9 |
| GND | M10 | GND | GND | GND | H6 |
| GND | M11 | GND | GND | GND | H7 |
| GND | M12 | GND | GND | GND | H8 |
| GND | N1 | GND | GND | GND | — |
| GND | N12 | GND | GND | GND | J8 |
| GND | N18 | GND | GND | GND | J14 |
| GND | N20 | GND | GND | GND | — |
| GND | R7 | GND | GND | GND | L3 |
| GND | T3 | GND | GND | GND | — |
| GND | V1 | GND | GND | GND | — |
| GND | V10 | GND | GND | GND | P6 |
| GND | Y12 | GND | GND | GND | — |
| GND | Y16 | GND | GND | GND | — |
| GND | AB5 | GND | GND | GND | — |
| GND | G1 | GND | GND | GND | — |
| GND | R1 | GND | GND | GND | — |
| VCC | C8 | VCC | VCC | VCC | — |
| VCC | D3 | VCC | VCC | VCC | — |
| VCC | K12 | VCC | VCC | VCC | F8 |
| VCC | L10 | VCC | VCC | VCC | G6 |
| VCC | L20 | VCC | VCC | VCC | — |
| VCC | M13 | VCC | VCC | VCC | H9 |
| VCC | N8 | VCC | VCC | VCC | J4 |
| VCC | N11 | VCC | VCC | VCC | J7 |
| VCC | Y8 | VCC | VCC | VCC | — |
| VPP_2V5 | E18 | VPP | VPP | VPP | A14 |
| VPP_FAST | E17 | VPP | VPP | VPP | A13 |

| iCE65L04 Pad Name | DiePlus | | | | | | |
|---|---|---|---|---|---|---|---|
| | VQ100 | CB132 | CB196 | CB284 | Pad | X (µm) | Y (µm) |
| **PIO2_08** | — | L6 | P3 | R10 | 74 | 965.00 | 37.20 |
| **VCCIO_2** | 31 | M5 | M5 | T9 | 75 | 1,000.00 | 139.20 |
| **PIO2_09** | — | P5 | K5 | V9 | 76 | 1,035.00 | 37.20 |
| **PIO2_10** | — | M6 | N4 | T10 | 77 | 1,070.00 | 139.20 |
| **GND** | 32 | P6 | H7 | V10 | 78 | 1,105.00 | 37.20 |
| **PIO2_11** | — | — | P4 | Y4 | 79 | 1,140.00 | 139.20 |
| **PIO2_12** | — | — | L6 | Y5 | 80 | 1,175.00 | 37.20 |
| **PIO2_13** | — | — | — | AB6 | 81 | 1,210.00 | 139.20 |
| **PIO2_14** | — | — | — | AB7 | 82 | 1,245.00 | 37.20 |
| **PIO2_15** | — | — | — | AB8 | 83 | 1,280.00 | 139.20 |
| **PIO2_16** | — | — | — | AB9 | 84 | 1,315.00 | 37.20 |
| **PIO2_17** | — | — | — | AB10 | 85 | 1,350.00 | 139.20 |
| **PIO2_18** | — | — | — | AB11 | 86 | 1,385.00 | 37.20 |
| **GND** | — | J8 | H8 | N12 | 87 | 1,420.00 | 139.20 |
| **PIO2_19** | — | — | K6 | Y6 | 88 | 1,455.00 | 37.20 |
| **PIO2_20** | — | — | N5 | Y7 | 89 | 1,490.00 | 139.20 |
| **VCC** | — | — | J4 | Y8 | 90 | 1,525.00 | 37.20 |
| **PIO2_21** | — | — | M6 | Y9 | 91 | 1,560.00 | 139.20 |
| **PIO2_22** | — | — | N6 | Y10 | 92 | 1,595.00 | 37.20 |
| **GBIN5/PIO2_23** | 33 | P7 | P5 | V11 | 93 | 1,630.00 | 139.20 |
| **GBIN4/PIO2_24** | 34 | P8 | L7 | V12 | 94 | 1,665.00 | 37.20 |
| **PIO2_25** | — | — | — | AB12 | 95 | 1,700.00 | 139.20 |
| **VCCIO_2** | — | — | J9 | Y11 | 96 | 1,735.00 | 37.20 |
| **PIO2_26** | — | — | — | AB13 | 97 | 1,770.00 | 139.20 |
| **PIO2_27** | — | — | K7 | AB14 | 98 | 1,805.00 | 37.20 |
| **GND** | — | — | J5 | Y12 | 99 | 1,840.00 | 139.20 |
| **PIO2_28** | — | — | K9 | AB15 | 100 | 1,875.00 | 37.20 |
| **PIO2_29** | — | — | M7 | Y13 | 101 | 1,910.00 | 139.20 |
| **PIO2_30** | — | — | K8 | Y14 | 102 | 1,945.00 | 37.20 |
| **PIO2_31** | — | — | P7 | Y15 | 103 | 1,980.00 | 139.20 |
| **PIO2_32** | — | — | L8 | Y17 | 104 | 2,015.00 | 37.20 |
| **PIO2_33** | — | — | P8 | Y18 | 105 | 2,050.00 | 139.20 |
| **PIO2_34** | — | — | N8 | Y19 | 106 | 2,085.00 | 37.20 |
| **PIO2_35** | — | — | M8 | Y20 | 107 | 2,120.00 | 139.20 |
| **VCC** | 35 | J7 | J7 | N11 | 108 | 2,155.00 | 37.20 |
| **VCC** | — | — | — | — | 109 | 2,190.00 | 139.20 |
| **PIO2_36** | 36 | P9 | P9 | V13 | 110 | 2,225.00 | 37.20 |
| **PIO2_37** | 37 | M7 | N9 | T11 | 111 | 2,260.00 | 139.20 |
| **VCCIO_2** | 38 | J9 | N10 | N13 | 112 | 2,295.00 | 37.20 |
| **PIO2_38** | — | L7 | M9 | R11 | 113 | 2,330.00 | 139.20 |
| **GND** | 39 | H8 | J8 | M12 | 114 | 2,365.00 | 37.20 |
| **PIO2_39** | — | M8 | N12 | T12 | 115 | 2,400.00 | 139.20 |
| **PIO2_40** | — | L8 | N11 | R12 | 116 | 2,435.00 | 37.20 |
| **PIO2_41** | 40 | M9 | N13 | T13 | 117 | 2,470.00 | 139.20 |
| **PIO2_42/CBSEL0** | 41 | L9 | L9 | R13 | 118 | 2,505.00 | 37.20 |
| **PIO2_43/CBSEL1** | 42 | P10 | P10 | V14 | 119 | 2,540.00 | 139.20 |
| **CDONE** | 43 | M10 | M10 | T14 | 120 | 2,575.00 | 37.20 |

| iCE65L04 Pad Name | DiePlus VQ100 | CB132 | CB196 | CB284 | Pad | X (µm) | Y (µm) |
|---|---|---|---|---|---|---|---|
| CRESET_B | 44 | L10 | L10 | R14 | 121 | 2,625.00 | 139.20 |
| PIOS_00/SPI_SO | 45 | M11 | M11 | T15 | 122 | 2,690.00 | 37.20 |
| PIOS_01/SPI_SI | 46 | P11 | P11 | V15 | 123 | 2,740.00 | 139.20 |
| GND | 47 | — | P6 | Y16 | 124 | 2,790.00 | 37.20 |
| PIOS_02/SPI_SCK | 48 | P12 | P12 | V16 | 125 | 2,840.00 | 139.20 |
| PIOS_03/SPI_SS_B | 49 | P13 | P13 | V17 | 126 | 2,890.00 | 37.20 |
| SPI_VCC | 50 | L11 | L11 | R15 | 127 | 2,990.00 | 37.20 |
| TDI | N/A | M12 | M12 | T16 | 128 | 3,610.80 | 342.00 |
| TMS | N/A | P14 | P14 | V18 | 129 | 3,712.80 | 392.00 |
| TCK | N/A | L12 | L12 | R16 | 130 | 3,610.80 | 442.00 |
| TDO | N/A | N14 | N14 | U18 | 131 | 3,712.80 | 492.00 |
| TRST_B | N/A | M14 | M14 | T18 | 132 | 3,610.80 | 542.00 |
| PIO1_00 | 51 | L14 | K11 | R18 | 133 | 3,712.80 | 592.00 |
| PIO1_01 | 52 | K12 | L13 | P16 | 134 | 3,610.80 | 642.00 |
| PIO1_02 | 53 | K11 | K12 | P15 | 135 | 3,712.80 | 692.00 |
| PIO1_03 | 54 | K14 | M13 | P18 | 136 | 3,610.80 | 727.00 |
| GND | 55 | J14 | J14 | N18 | 137 | 3,712.80 | 762.00 |
| GND | 55 | J14 | J14 | N18 | 138 | 3,610.80 | 797.00 |
| PIO1_04 | 56 | J12 | J10 | N16 | 139 | 3,712.80 | 832.00 |
| PIO1_05 | 57 | J11 | L14 | N15 | 140 | 3,610.80 | 867.00 |
| VCCIO_1 | 58 | H14 | H14 | M18 | 141 | 3,712.80 | 902.00 |
| VCCIO_1 | — | — | — | — | 142 | 3,610.80 | 937.00 |
| PIO1_06 | 59 | H12 | J11 | M16 | 143 | 3,712.80 | 972.00 |
| PIO1_07 | 60 | H11 | K14 | M15 | 144 | 3,610.80 | 1,007.00 |
| PIO1_08 | — | — | H10 | W20 | 145 | 3,712.80 | 1,042.00 |
| PIO1_09 | — | — | J13 | V20 | 146 | 3,610.80 | 1,077.00 |
| PIO1_10 | — | — | J12 | U20 | 147 | 3,712.80 | 1,112.00 |
| VCC | 61 | H9 | N7 | M13 | 148 | 3,610.80 | 1,147.00 |
| VCC | — | — | — | — | 149 | 3,712.80 | 1,182.00 |
| PIO1_11 | — | — | H13 | T22 | 150 | 3,610.80 | 1,217.00 |
| PIO1_12 | — | — | H12 | R22 | 151 | 3,712.80 | 1,252.00 |
| PIO1_13 | — | — | — | P22 | 152 | 3,610.80 | 1,287.00 |
| PIO1_14 | — | — | — | N22 | 153 | 3,712.80 | 1,322.00 |
| PIO1_15 | | — | G13 | T20 | 154 | 3,610.80 | 1,357.00 |
| PIO1_16 | — | — | H11 | R20 | 155 | 3,712.80 | 1,392.00 |
| PIO1_17 | — | — | G14 | P20 | 156 | 3,610.80 | 1,427.00 |
| GND | — | — | K10 | N20 | 157 | 3,712.80 | 1,462.00 |
| GND | — | — | — | — | 158 | 3,610.80 | 1,497.00 |
| PIO1_18 | — | — | G10 | M20 | 159 | 3,712.80 | 1,532.00 |
| GBIN3/PIO1_19 | 62 | F14 | G12 | K18 | 160 | 3,610.80 | 1,567.00 |
| GBIN2/PIO1_20 | 63 | G14 | F10 | L18 | 161 | 3,712.80 | 1,602.00 |
| PIO1_21 | — | — | F14 | K20 | 162 | 3,610.80 | 1,637.00 |
| VCCIO_1 | — | — | H14 | J20 | 163 | 3,712.80 | 1,672.00 |
| VCCIO_1 | — | — | — | — | 164 | 3,610.80 | 1,707.00 |
| PIO1_22 | — | — | F13 | H20 | 165 | 3,712.80 | 1,742.00 |
| PIO1_23 | — | — | D13 | G20 | 166 | 3,610.80 | 1,777.00 |

| iCE65L08 Pad Name | Available Packages | | DiePlus | | |
|---|---|---|---|---|---|
| | CB196 | CB284 | Pad | X (µm) | Y (µm) |
| PIO2_28 | — | Y13 | 132 | 2,062.5 | 139.5 |
| GBIN5/PIO2_29 | M7 | V11 | 133 | 2,097.5 | 37.5 |
| GBIN4/PIO2_30 | N8 | V12 | 134 | 2,132.5 | 139.5 |
| GND | J8 | Y12 | 135 | 2,167.5 | 37.5 |
| GND | — | — | 136 | 2,202.5 | 139.5 |
| PIO2_31 | P8 | Y14 | 137 | 2,237.5 | 37.5 |
| PIO2_32 | — | AB15 | 138 | 2,272.5 | 139.5 |
| PIO2_33 | M8 | V13 | 139 | 2,307.5 | 37.5 |
| PIO2_34 | — | AB16 | 140 | 2,342.5 | 139.5 |
| PIO2_35 | L8 | Y15 | 141 | 2,377.5 | 37.5 |
| PIO2_36 | — | AB17 | 142 | 2,412.5 | 139.5 |
| PIO2_37 | N9 | AB18 | 143 | 2,447.5 | 37.5 |
| PIO2_38 | — | AB19 | 144 | 2,482.5 | 139.5 |
| PIO2_39 | — | AB20 | 145 | 2,517.5 | 37.5 |
| PIO2_40 | — | AB21 | 146 | 2,552.5 | 139.5 |
| PIO2_41 | — | Y17 | 147 | 2,587.5 | 37.5 |
| PIO2_42 | — | AB22 | 148 | 2,622.5 | 139.5 |
| PIO2_43 | — | Y18 | 149 | 2,657.5 | 37.5 |
| PIO2_44 | P9 | Y19 | 150 | 2,692.5 | 139.5 |
| VCC | N7 | N11 | 151 | 2,727.5 | 37.5 |
| VCC | — | — | 152 | 2,762.5 | 139.5 |
| PIO2_45 | M9 | Y20 | 153 | 2,797.5 | 37.5 |
| PIO2_46 | K8 | T11 | 154 | 2,832.5 | 139.5 |
| VCCIO_2 | J9 | N13 | 155 | 2,867.5 | 37.5 |
| VCCIO_2 | — | — | 156 | 2,902.5 | 139.5 |
| PIO2_47 | N11 | R11 | 157 | 2,937.5 | 37.5 |
| GND | J8 | M12 | 158 | 2,972.5 | 139.5 |
| GND | — | — | 159 | 3,007.5 | 37.5 |
| PIO2_48 | N12 | T12 | 160 | 3,042.5 | 139.5 |
| PIO2_49 | K9 | R12 | 161 | 3,077.5 | 37.5 |
| PIO2_50 | N13 | T13 | 162 | 3,112.5 | 139.5 |
| PIO2_51/CBSEL0 | L9 | R13 | 163 | 3,147.5 | 37.5 |
| PIO2_52/CBSEL1 | P10 | V14 | 164 | 3,182.5 | 139.5 |
| CDONE | M10 | T14 | 165 | 3,217.5 | 37.5 |
| CRESET_B | L10 | R14 | 166 | 3,260.0 | 139.5 |
| PIOS_00/SPI_SO | M11 | T15 | 167 | 3,320.0 | 37.5 |
| PIOS_01/SPI_SI | P11 | V15 | 168 | 3,370.0 | 139.5 |
| GND | J8 | Y16 | 169 | 3,420.0 | 37.5 |
| GND | — | — | 170 | 3,470.0 | 139.5 |
| PIOS_02/SPI_SCK | P12 | V16 | 171 | 3,520.0 | 37.5 |
| PIOS_03/SPI_SS_B | P13 | V17 | 172 | 3,570.0 | 139.5 |
| VCC | — | — | 173 | 3,620.0 | 37.5 |
| VCC | — | — | 174 | 3,670.0 | 139.5 |
| SPI_VCC | L11 | R15 | 175 | 3,720.0 | 37.5 |
| SPI_VCC | — | — | 176 | 3,770.0 | 139.5 |

## Electrical Characteristics

All parameter limits are specified under worst-case supply voltage, temperature, and processing conditions.

### Absolute Maximum Ratings

Stresses beyond those listed under Table 47 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

**Table 47: Absolute Maximum Ratings**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **VCC** | Core supply Voltage | –0.5 | 1.42 | V |
| **VPP_2V5** | VPP_2V5 NVCM programming and operating supply | | | V |
| **VPP_FAST** | Optional fast NVCM programming supply | | | V |
| **VCCIO_0**<br>**VCCIO_1**<br>**VCCIO_2**<br>**SPI_VCC** | I/O bank supply voltage (I/O Banks 0, 1, and 2 plus SPI interface) | –0.5 | 4.00 | V |
| **VCCIO_3** | I/O Bank 3 supply voltage | –0.5 | iCE65L01: 4.00<br>iCE65L04/08: 3.6 | V |
| **VIN_0**<br>**VIN_1**<br>**VIN_2**<br>**VIN_SPI** | Voltage applied to PIO pin within a specific I/O bank (I/O Banks 0, 1, and 2 plus SPI interface) | –1.0 | 5.5 | V |
| **VIN_3**<br>**VIN_VREF** | Voltage applied to PIO pin within I/O Bank 3 | –0.5 | iCE65L01: 4.00<br>iCE65L04/08: 3.6 | V |
| **IOUT** | DC output current per pin | — | 20 | mA |
| **$T_J$** | Junction temperature | –55 | 125 | °C |
| **$T_{STG}$** | Storage temperature, no bias | –65 | 150 | °C |

### Recommended Operating Conditions

***Table 48:*** **Recommended Operating Conditions**

| Symbol | Description | | Minimum | Nominal | Maximum | Units |
|---|---|---|---|---|---|---|
| VCC | Core supply voltage | –L: Ultra-Low Power mode | 0.95 | 1.00 | 1.05 | V |
| | | –L: Low Power<br>–T: High Performance | 1.14 | 1.20 | 1.26 | V |
| VPP_2V5 | VPP_2V5 NVCM programming and operating supply | Release from Power-on Reset | 1.30 | — | 3.47 | V |
| | | Configure from NVCM | 2.30 | — | 3.47 | V |
| | | NVCM programming | 2.30 | — | 3.00 | V |
| VPP_FAST | Optional fast NVCM programming supply | | Leave unconnected in application | | | |
| SPI_VCC | SPI interface supply voltage | | 1.71 | — | 3.47 | V |
| VCCIO_0<br>VCCIO_1<br>VCCIO_2<br>VCCIO_3<br>SPI_VCC | I/O standards, all banks* | **LVCMOS33** | 3.14 | 3.30 | 3.47 | V |
| | | **Non-standard voltage:**<br>in between 2.5V and 3.3V<br>use LVCMOS25 in iCEcube2 | Nominal -5% | 2.5< Nominal <3.3 | Nominal +5% | V |
| | | **LVCMOS25, LVDS** | 2.38 | 2.50 | 2.63 | V |
| | | **LVCMOS18, SubLVDS** | 1.71 | 1.80 | 1.89 | V |
| | | **LVCMOS15** | 1.43 | 1.50 | 1.58 | V |
| VCCIO_3 | I/O standards only available in iCE65L04/08 I/O Bank 3* | **SSTL2** | 2.38 | 2.50 | 2.63 | V |
| | | **SSTL18** | 1.71 | 1.80 | 1.89 | V |
| | | **MDDR** | 1.71 | 1.80 | 1.89 | V |
| $T_A$ | Ambient temperature | Commercial (C) | 0 | — | 70 | °C |
| | | Industrial (I) | –40 | — | 85 | °C |
| **$T_{PROG}$** | NVCM programming temperature | | 10 | 25 | 30 | °C |

**NOTE:**

VPP_FAST is only used for fast production programming. Leave floating or unconnected in application. When the iCE65 device is active, VPP_2V5 must be connected to a valid voltage.

## Internal Configuration Oscillator Frequency

Table 57 shows the operating frequency for the iCE65's internal configuration oscillator.

**Table 57: Internal Oscillator Frequency**

| Symbol | Oscillator Mode | Frequency (MHz) Min. | Frequency (MHz) Max. | Description |
|---|---|---|---|---|
| $f_{OSCD}$ | **Default** | 4.0 | 6.8 | Default oscillator frequency. Slow enough to safely operate with any SPI serial PROM. |
| $f_{OSCL}$ | **Low Frequency** | 14 | 21 | Supported by most SPI serial Flash PROMs |
| $f_{OSCH}$ | **High Frequency** | 21 | 31 | Supported by some high-speed SPI serial Flash PROMs |
| | **Off** | 0 | 0 | Oscillator turned off by default after configuration to save power. |

## Configuration Timing

Table 58 shows the maximum time to configure an iCE65 device, by oscillator mode. The calculations use the slowest frequency for a given oscillator mode from Table 57 and the maximum configuration bitstream size from Table 1 which includes full RAM4K block initialization. The configuration bitstream selects the desired oscillator mode based on the performance of the configuration data source.

***Table 58:*** **Maximum SPI Master or NVCM Configuration Timing by Oscillator Mode**

| Symbol | Description | Device | Default | Low Freq. | High Freq. | Units |
|---|---|---|---|---|---|---|
| $t_{CONFIGL}$ | Time from when minimum Power-on Reset (POR) threshold is reached until user application starts. | **iCE65L01** | 53 | 25 | 11 | ms |
| | | **iCE65L04** | 115 | 55 | 25 | ms |
| | | **iCE65L08** | 230 | 110 | 50 | ms |

Table 59 provides timing for the CRESET_B and CDONE pins.

**Table 59: General Configuration Timing**

| Symbol | From | To | Description | | All Grades Min. | All Grades Max. | Units |
|---|---|---|---|---|---|---|---|
| $\mathbf{t_{CRESET\_B}}$ | CREST_B | CREST_B | Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge | | 200 | — | ns |
| $\mathbf{t_{DONE\_IO}}$ | CDONE High | PIO pins active | Number of configuration clock cycles after CDONE goes High before the PIO pins are activated. | | — | 49 | Clock cycles |
| | | | SPI Peripheral Mode (Clock = SPI_SCK, cycles measured rising-edge to rising-edge) | | Depends on SPI_SCK frequency | | |
| | | | NVCM or SPI Master Mode by internal oscillator frequency setting (Clock = internal oscillator) | Default | 7.20 | 12.25 | µs |
| | | | | Low | 2.34 | 3.50 | µs |
| | | | | High | 1.59 | 2.33 | µs |