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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	62
Program Memory Size	256KB (128K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8356vfve

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8156 device and are shaded in the following figures.*

The 56F8356/56F8156 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories, the external memory interface and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User Manual** for clarification on the operation of all three of these peripherals.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F8356 and 56F8156 are organized into functional groups, as detailed in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins in Package	
	56F8356	56F8156
Power (V_{DD} or V_{DDA})	9	9
Power Option Control	1	1
Ground (V_{SS} or V_{SSA})	6	6
Supply Capacitors[1] & V_{PP}	6	6
PLL and Clock	4	4
Address Bus	17	17
Data Bus	16	16
Bus Control	6	6
Interrupt and Program Control	6	6
Pulse Width Modulator (PWM) Ports	25	13
Serial Peripheral Interface (SPI) Port 0	4	4
Serial Peripheral Interface (SPI) Port 1	—	4
Quadrature Decoder Port 0[2]	4	4
Quadrature Decoder Port 1[3]	4	—
Serial Communications Interface (SCI) Ports	4	4
CAN Ports	2	—
Analog to Digital Converter (ADC) Ports	21	21
Quad Timer Module Ports	3	1
JTAG/Enhanced On-Chip Emulation (EOnCE)	5	5
Temperature Sense	1	—
Dedicated GPIO	—	5

1. If the on-chip regulator is disabled, the V_{CAP} pins serve as 2.5V V_{DD_CORE} power inputs
2. Alternately, can function as Quad Timer pins or GPIO
3. Pins in this section can function as Quad Timer, SPI #1, or GPIO

Part 3 On-Chip Clock Synthesis (OCCS)

3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design. **Figure 3-1** shows the specific OCCS block diagram to reference from the OCCS chapter of the **56F8300 Peripheral User Manual**.

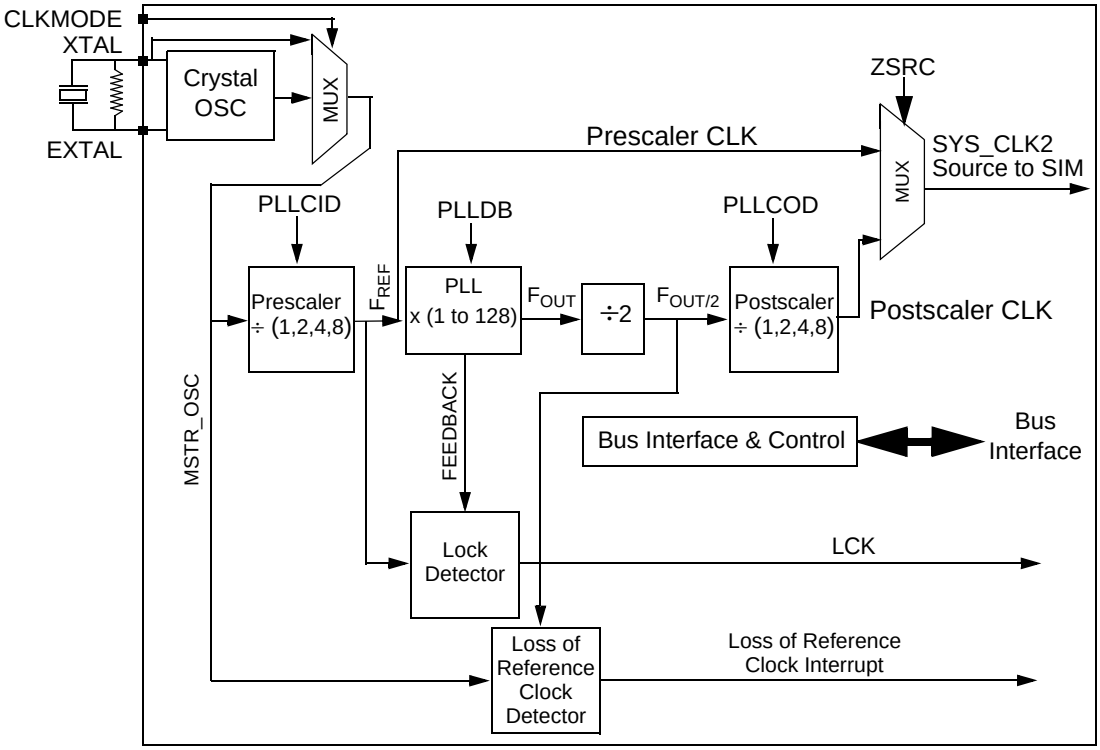


Figure 3-1 OCCS Block Diagram

3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator, or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator must be connected between the EXTAL and XTAL pins.

3.2.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-15**. A recommended crystal oscillator circuit is shown in **Figure 3-2**. Follow the crystal supplier's recommendations when selecting a crystal, since crystal

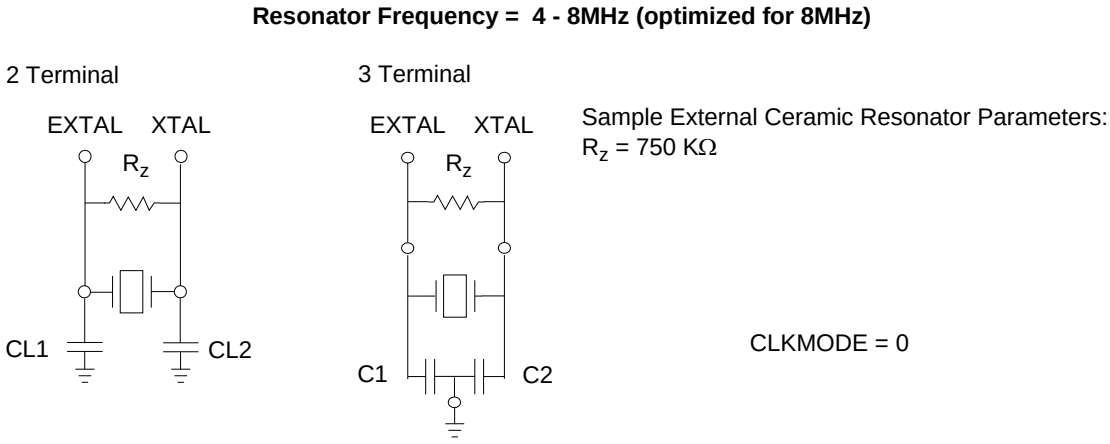


Figure 3-3 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a ceramic resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-4**. The external clock source is connected to XTAL and the EXTAL pin is grounded. Set OCCS_COHL bit high when using an external clock source as well.

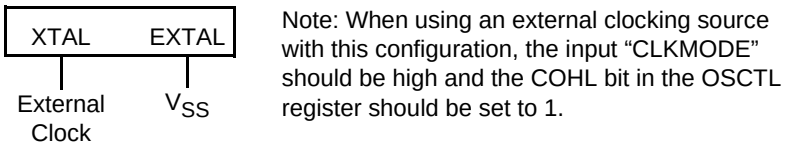


Figure 3-4 Connecting an External Clock Register

3.3 Registers

When referring to the register definitions for the OCCS in the **56F8300 Peripheral User Manual**, use the register definitions **without** the internal Relaxation Oscillator, since the 56F8356/56F8156 devices do NOT contain this oscillator.

Part 4 Memory Map

4.1 Introduction

The 56F8356 and 56F8156 devices are 16-bit motor-control chips based on the 56800E core. These parts use a Harvard-style architecture with two independent memory spaces for Data and Program. On-chip RAM and Flash memories are used in both spaces.

4.7 Peripheral Memory Mapped Registers

On-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary Data memory, except all peripheral registers should be read/written using word accesses only.

Table 4-9 summarizes base addresses for the set of peripherals on the 56F8356 and 56F8156 devices. Peripherals are listed in order of the base address.

The following tables list all of the peripheral registers required to control or access the peripherals.

Note: *Features in italics are NOT available in the 56F8156 device.*

Table 4-9 Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address	Table Number
External Memory Interface	EMI	X:$00 F020	4-10
Timer A	TMRA	X:$00 F040	4-11
Timer B	TMRB	X:$00 F080	4-12
Timer C	TMRC	X:$00 F0C0	4-13
Timer D	TMRD	X:$00 F100	4-14
PWM A	PWMA	X:$00 F140	4-15
PWM B	PWMB	X:$00 F160	4-16
Quadrature Decoder 0	DEC0	X:$00 F180	4-17
Quadrature Decoder 1	DEC1	X:$00 F190	4-18
ITCN	ITCN	X:$00 F1A0	4-19
ADC A	ADCA	X:$00 F200	4-20
ADC B	ADCB	X:$00 F240	4-21
Temperature Sensor	TSENSOR	X:$00 F270	4-22
SCI #0	SCI0	X:$00 F280	4-23
SCI #1	SCI1	X:$00 F290	4-24
SPI #0	SPI0	X:$00 F2A0	4-25
SPI #1	SPI1	X:$00 F2B0	4-26
COP	COP	X:$00 F2C0	4-27
PLL, OSC	CLKGEN	X:$00 F2D0	4-28
GPIO Port A	GPIOA	X:$00 F2E0	4-29
GPIO Port B	GPIOB	X:$00 F300	4-30
GPIO Port C	GPIOC	X:$00 F310	4-31
GPIO Port D	GPIOD	X:$00 F320	4-32

Table 4-21 Analog-to-Digital Converter Registers Address Map (Continued) (ADCB_BASE = $00 F240)

Register Acronym	Address Offset	Register Description
ADCB_LLMT 1	$12	Low Limit Register 1
ADCB_LLMT 2	$13	Low Limit Register 2
ADCB_LLMT 3	$14	Low Limit Register 3
ADCB_LLMT 4	$15	Low Limit Register 4
ADCB_LLMT 5	$16	Low Limit Register 5
ADCB_LLMT 6	$17	Low Limit Register 6
ADCB_LLMT 7	$18	Low Limit Register 7
ADCB_HLMT 0	$19	High Limit Register 0
ADCB_HLMT 1	$1A	High Limit Register 1
ADCB_HLMT 2	$1B	High Limit Register 2
ADCB_HLMT 3	$1C	High Limit Register 3
ADCB_HLMT 4	$1D	High Limit Register 4
ADCB_HLMT 5	$1E	High Limit Register 5
ADCB_HLMT 6	$1F	High Limit Register 6
ADCB_HLMT 7	$20	High Limit Register 7
ADCB_OFS 0	$21	Offset Register 0
ADCB_OFS 1	$22	Offset Register 1
ADCB_OFS 2	$23	Offset Register 2
ADCB_OFS 3	$24	Offset Register 3
ADCB_OFS 4	$25	Offset Register 4
ADCB_OFS 5	$26	Offset Register 5
ADCB_OFS 6	$27	Offset Register 6
ADCB_OFS 7	$28	Offset Register 7
ADCB_POWER	$29	Power Control Register
ADCB_CAL	$2A	ADC Calibration Register

Table 4-22 Temperature Sensor Register Address Map (TSENSOR_BASE = $00 F270)
Temperature Sensor is NOT available in the 56F8156 device

Register Acronym	Address Offset	Register Description
TSENSOR_CNTL	$0	Control Register

Table 4-38 FlexCAN Registers Address Map (Continued)
(FC_BASE = $00 F800)
FlexCAN is NOT available in the 56F8156 device

Register Acronym	Address Offset	Register Description
FCMB6_DATA	$76	Message Buffer 6 Data Register
		Reserved
FCMB7_CONTROL	$78	Message Buffer 7 Control / Status Register
FCMB7_ID_HIGH	$79	Message Buffer 7 ID High Register
FCMB7_ID_LOW	$7A	Message Buffer 7 ID Low Register
FCMB7_DATA	$7B	Message Buffer 7 Data Register
FCMB7_DATA	$7C	Message Buffer 7 Data Register
FCMB7_DATA	$7D	Message Buffer 7 Data Register
FCMB7_DATA	$7E	Message Buffer 7 Data Register
		Reserved
FCMB8_CONTROL	$80	Message Buffer 8 Control / Status Register
FCMB8_ID_HIGH	$81	Message Buffer 8 ID High Register
FCMB8_ID_LOW	$82	Message Buffer 8 ID Low Register
FCMB8_DATA	$83	Message Buffer 8 Data Register
FCMB8_DATA	$84	Message Buffer 8 Data Register
FCMB8_DATA	$85	Message Buffer 8 Data Register
FCMB8_DATA	$86	Message Buffer 8 Data Register
		Reserved
FCMB9_CONTROL	$88	Message Buffer 9 Control / Status Register
FCMB9_ID_HIGH	$89	Message Buffer 9 ID High Register
FCMB9_ID_LOW	$8A	Message Buffer 9 ID Low Register
FCMB9_DATA	$8B	Message Buffer 9 Data Register
FCMB9_DATA	$8C	Message Buffer 9 Data Register
FCMB9_DATA	$8D	Message Buffer 9 Data Register
FCMB9_DATA	$8E	Message Buffer 9 Data Register
		Reserved
FCMB10_CONTROL	$90	Message Buffer 10 Control / Status Register
FCMB10_ID_HIGH	$91	Message Buffer 10 ID High Register
FCMB10_ID_LOW	$92	Message Buffer 10 ID Low Register
FCMB10_DATA	$93	Message Buffer 10 Data Register
FCMB10_DATA	$94	Message Buffer 10 Data Register
FCMB10_DATA	$95	Message Buffer 10 Data Register

5.4 Block Diagram

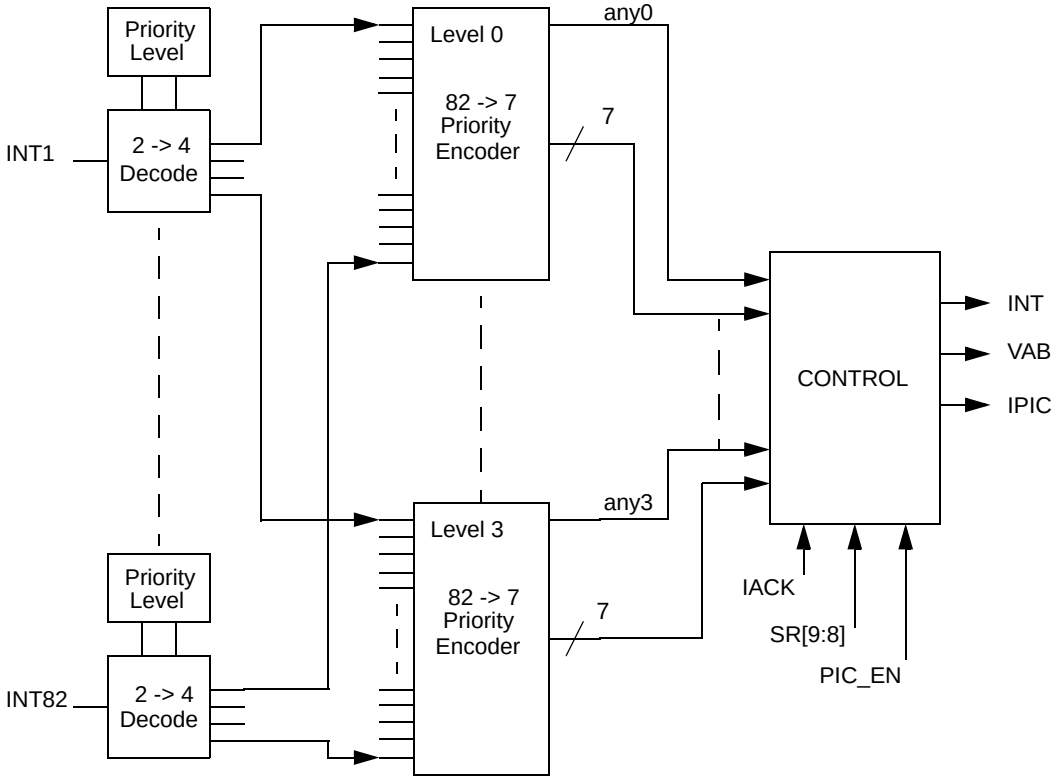


Figure 5-1 Interrupt Controller Block Diagram

5.5 Operating Modes

The ITCN module design contains two major modes of operation:

- **Functional Mode**
  The ITCN is in this mode by default.
- **Wait and Stop Modes**
  During Wait and Stop modes, the system clocks and the 56800E core are turned off. The ITCN will signal a pending IRQ to the System Integration Module (SIM) to restart the clocks and service the IRQ. An IRQ can only wake up the core if the IRQ is enabled prior to entering the Wait or Stop mode. Also, the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ signals automatically become low-level sensitive in these modes even if the control register bits are set to make them falling-edge sensitive. This is because there is no clock available to detect the falling edge.

  A peripheral which requires a clock to generate interrupts will not be able to generate interrupts during Stop mode. The FlexCAN module can wake the device from Stop mode, and a reset will do just that, or $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ can wake it up.

5.6 Register Descriptions

A register address is the sum of a base address and an address offset. The base address is defined at the

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.5 Timer B, Channel 0 Interrupt Priority Level (TMRB0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.6 Timer C, Channel 3 Interrupt Priority Level (TMRC3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.7 Timer C, Channel 2 Interrupt Priority Level (TMRC2 IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8.8 Timer C, Channel 1 Interrupt Priority Level (TMRC1 IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

- 11 = Required nested exception priority level is 3

5.6.30.3 Vector Number - Vector Address Bus (VAB)—Bits 12–6

This *read-only* field shows the vector number (VAB[7:1]) used at the time the last IRQ was taken. This field is only updated when the 56800E core jumps to a new interrupt service routine.

Note: Nested interrupts may cause this field to be updated before the original interrupt service routine can read it.

5.6.30.4 Interrupt Disable (INT_DIS)—Bit 5

This bit allows all interrupts to be disabled.

- 0 = Normal operation (default)
- 1 = All interrupts disabled

5.6.30.5 Reserved—Bit 4

This bit field is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.30.6 $\overline{\text{IRQB}}$ State Pin ($\overline{\text{IRQB}}$ STATE)—Bit 3

This *read-only* bit reflects the state of the external $\overline{\text{IRQB}}$ pin.

5.6.30.7 $\overline{\text{IRQA}}$ State Pin ($\overline{\text{IRQA}}$ STATE)—Bit 2

This *read-only* bit reflects the state of the external $\overline{\text{IRQA}}$ pin.

5.6.30.8 $\overline{\text{IRQB}}$ Edge Pin ($\overline{\text{IRQB}}$ Edg)—Bit 1

This bit controls whether the external $\overline{\text{IRQB}}$ interrupt is edge- or level-sensitive. During Stop and Wait modes, it is automatically level-sensitive.

- 0 = $\overline{\text{IRQB}}$ interrupt is a low-level sensitive (default)
- 1 = $\overline{\text{IRQB}}$ interrupt is falling-edge sensitive

5.6.30.9 $\overline{\text{IRQA}}$ Edge Pin ($\overline{\text{IRQA}}$ Edg)—Bit 0

This bit controls whether the external $\overline{\text{IRQA}}$ interrupt is edge- or level-sensitive. During Stop and Wait modes, it is automatically level-sensitive.

- 0 = $\overline{\text{IRQA}}$ interrupt is a low-level sensitive (default)
- 1 = $\overline{\text{IRQA}}$ interrupt is falling-edge sensitive

6.5.1.2 EMI_MODE (EMI_MODE)—Bit 6

This bit reflects the current (non-clocked) state of the EMI_MODE pin. During reset, this bit, coupled with the EXTBOOT signal, is used to initialize address bits [19:16] either as GPIO or as address. These settings can be explicitly overwritten using the appropriate GPIO peripheral enable register at any time after reset. In addition, this pin can be used as a general purpose input pin after reset.

- 0 = External address bits [19:16] are initially programmed as GPIO
- 1 = When booted with EXTBOOT = 1, A[19:16] are initially programmed as address. If EXTBOOT is 0, they are initialized as GPIO.

6.5.1.3 OnCE Enable (OnCE EBL)—Bit 5

- 0 = OnCE clock to 56800E core enabled when core TAP is enabled
- 1 = OnCE clock to 56800E core is always enabled

6.5.1.4 Software Reset (SW RST)—Bit 4

This bit is always read as 0. Writing a 1 to this bit will cause the part to reset.

6.5.1.5 Stop Disable (STOP_DISABLE)—Bits 3–2

- 00 - Stop mode will be entered when the 56800E core executes a STOP instruction
- 01 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can be reprogrammed in the future
- 10 - The 56800E STOP instruction will not cause entry into Stop mode; STOP_DISABLE can then only be changed by resetting the device
- 11 - Same operation as 10

6.5.1.6 Wait Disable (WAIT_DISABLE)—Bits 1–0

- 00 - Wait mode will be entered when the 56800E core executes a WAIT instruction
- 01 - The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can be reprogrammed in the future
- 10 - The 56800E WAIT instruction will not cause entry into Wait mode; WAIT_DISABLE can then only be changed by resetting the device
- 11 - Same operation as 10

6.5.2 SIM Reset Status Register (SIM_RSTSTS)

Bits in this register are set upon any system reset and are initialized only by a Power-On Reset (POR). A reset (other than POR) will only set bits in the register; bits are not cleared. Only software should clear this register.

Base + $1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0					0	0

Figure 6-4 SIM Reset Status Register (SIM_RSTSTS)

6.5.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.2.2 Software Reset (SWR)—Bit 5

When 1, this bit indicates that the previous reset occurred as a result of a software reset (write to SW RST bit in the SIM_CONTROL register). This bit will be cleared by any hardware reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.3 COP Reset (COPR)—Bit 4

When 1, the COPR bit indicates the Computer Operating Properly (COP) timer-generated reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external RESET pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can be cleared only by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown below. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

6.5.6 SIM Pull-up Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pull-up resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pull-ups disabled by setting the appropriate bit in this register. Disabling pull-ups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See **Table 2-2** to identify which pins can deactivate the internal pull-up resistor.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	PWMA1	CAN	EMI_ MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA0	0	CTRL	0	JTAG	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8 SIM Pull-up Disable Register (SIM_PUDR)

6.5.6.1 Reserved—Bit 15

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.6.2 PWMA1—Bit 14

This bit controls the pull-up resistors on the FAULTA3 pin.

6.5.6.3 CAN—Bit 13

This bit controls the pull-up resistors on the CAN_RX pin.

6.5.6.4 EMI_MODE—Bit 12

This bit controls the pull-up resistors on the EMI_MODE pin.

6.5.6.5 $\overline{\text{RESET}}$—Bit 11

This bit controls the pull-up resistors on the $\overline{\text{RESET}}$ pin.

6.5.6.6 IRQ—Bit 10

This bit controls the pull-up resistors on the $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ pins.

6.5.6.7 XBOOT—Bit 9

This bit controls the pull-up resistors on the EXTBOOT pin.

6.5.6.8 PWMB—Bit 8

This bit controls the pull-up resistors on the FAULTB0, FAULTB1, FAULTB2, and FAULTB3 pins.

6.5.6.9 PWMA0—Bit 7

This bit controls the pull-up resistors on the FAULTA0, FAULTA1, and FAULTA2 pins.

6.5.6.10 Reserved—Bit 6

Table 8-3 GPIO External Signals Map (Continued)
Pins in shaded rows are not available in 56F8356/56F8156
Pins in italics are NOT available in the 56F8156 device

GPIO Port	GPIO Bit	Reset Function	Functional Signal	Package PIn
GPIOF	0	Peripheral	D7	28
	1	Peripheral	D8	29
	2	Peripheral	D9	30
	3	Peripheral	D10	32
	4	Peripheral	D11	133
	5	Peripheral	D12	134
	6	Peripheral	D13	135
	7	Peripheral	D14	136
	8	Peripheral	D15	137
	9	Peripheral	D0	59
	10	Peripheral	D1	60
	11	Peripheral	D2	72
	12	Peripheral	D3	75
	13	Peripheral	D4	76
	14	Peripheral	D5	77
	15	Peripheral	D6	78

1. See **Part 6.5.8** to determine how to select peripherals from this set; DEC1 is the selected peripheral at reset.

Part 9 Joint Test Action Group (JTAG)

9.1 56F8356 Information

Please contact your Freescale marketing representative or authorized distributor for device/package-specific BSDL information.

Part 10 Specifications

10.1 General Characteristics

The 56F8356/56F8156 are fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term “5V-tolerant” refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture

Table 10-18 SPI Timing[1] (Continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-10, 10-11, 10-12, 10-13

1. Parameters listed are guaranteed by design.

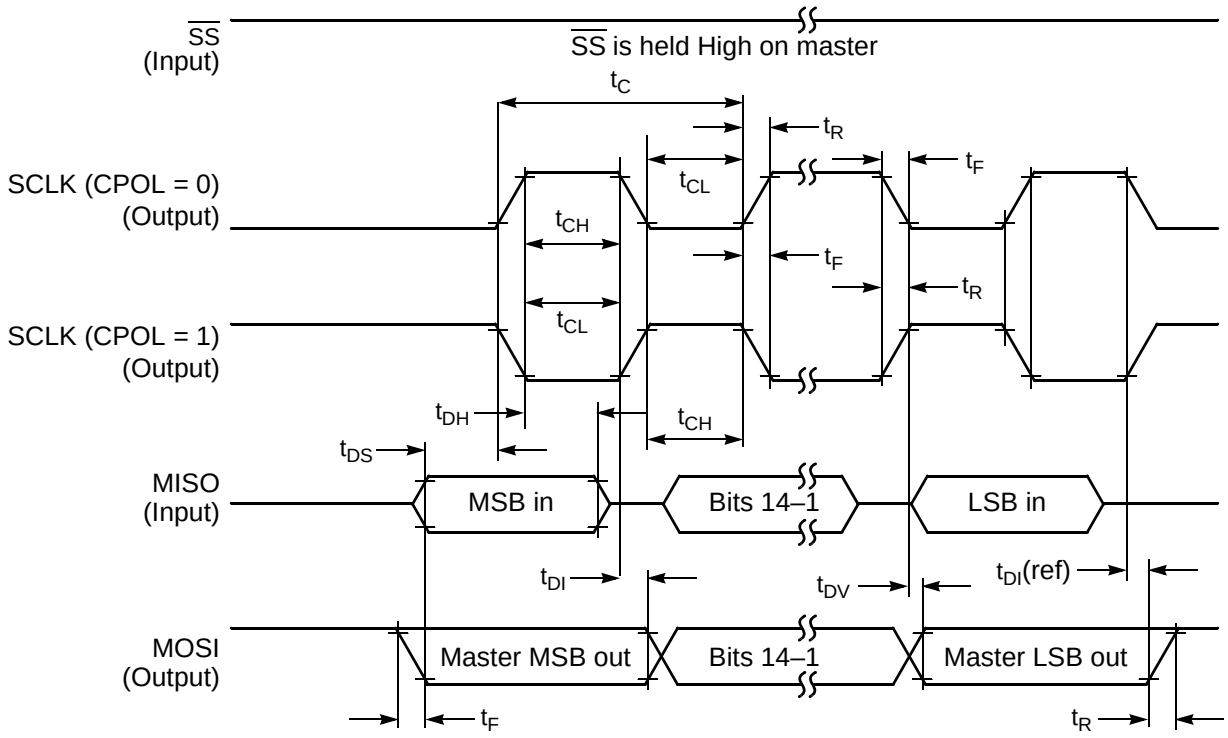
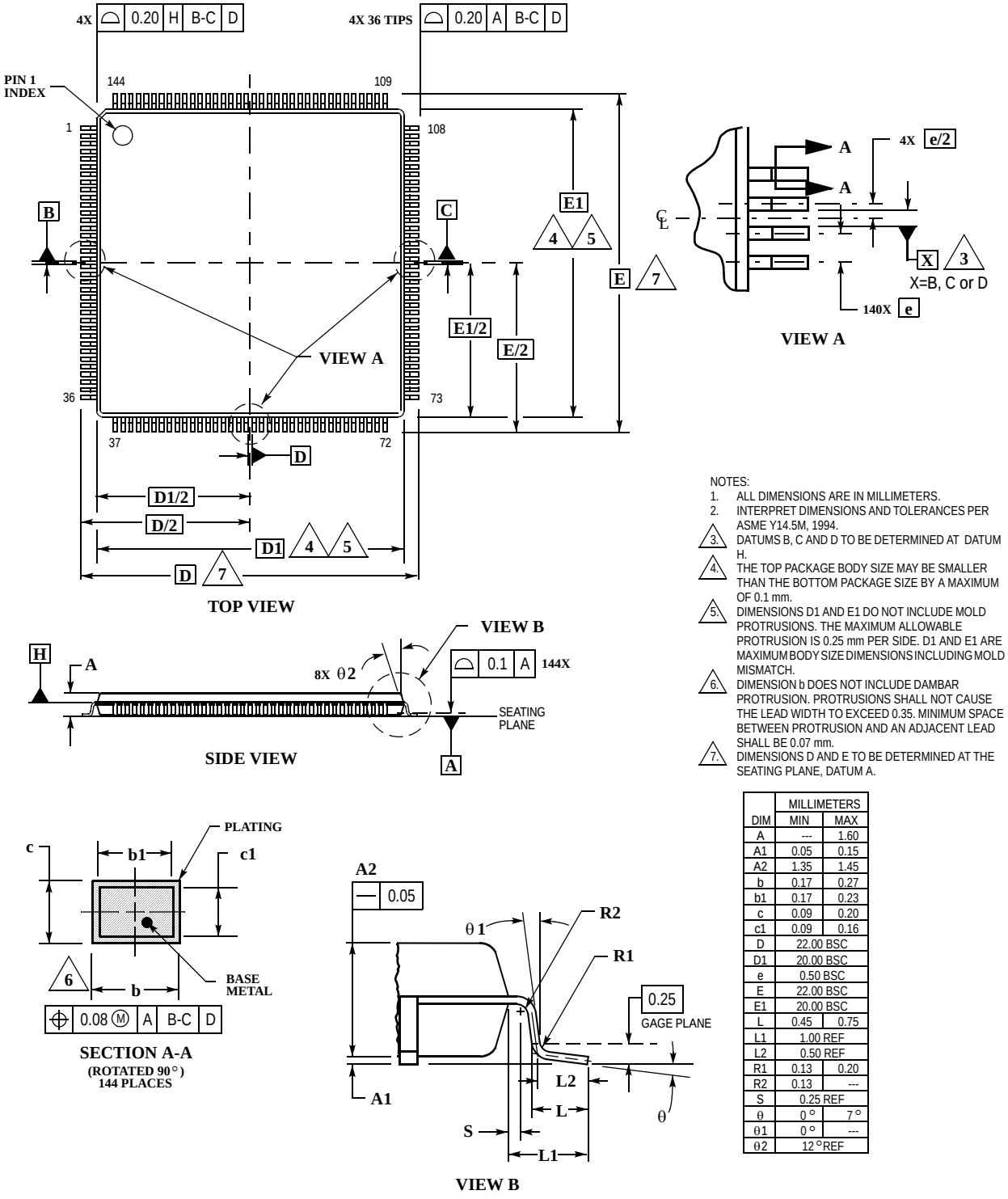


Figure 10-10 SPI Master Timing (CPHA = 0)

Table 11-1 56F8356 144-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{DD_IO}	37	V_{SS}	73	FAULTA1	109	ANB5
2	$V_{PP}2$	38	V_{DD_IO}	74	FAULTA2	110	ANB6
3	CLKO	39	PWMB3	75	D3	111	ANB7
4	TXD0	40	PWMB4	76	D4	112	EXTBOOT
5	RXD0	41	PWMB5	77	D5	113	ISA0
6	PHASEA1	42	TXD1	78	D6	114	ISA1
7	PHASEB1	43	RXD1	79	OCR_DIS	115	ISA2
8	INDEX1	44	$\overline{WR}$	80	$V_{DDA\_OSC\_PLL}$	116	TD0
9	HOME1	45	$\overline{RD}$	81	XTAL	117	TD1
10	A1	46	$\overline{PS}$	82	EXTAL	118	TC0
11	A2	47	$\overline{DS}$	83	$V_{CAP}3$	119	V_{DD_IO}
12	A3	48	GPIOD0	84	V_{DD_IO}	120	$\overline{TRST}$
13	A4	49	GPIOD1	85	$\overline{RSTO}$	121	TCK
14	A5	50	ISB0	86	$\overline{RESET}$	122	TMS
15	$V_{CAP}4$	51	$V_{CAP}1$	87	CLKMODE	123	TDI
16	V_{DD_IO}	52	ISB1	88	ANA0	124	TDO
17	A6	53	ISB2	89	ANA1	125	$V_{PP}1$
18	A7	54	$\overline{IRQA}$	90	ANA2	126	CAN_TX
19	A8	55	$\overline{IRQB}$	91	ANA3	127	CAN_RX
20	A9	56	FAULTB0	92	ANA4	128	$V_{CAP}2$
21	A10	57	FAULTB1	93	ANA5	129	$\overline{SS0}$
22	A11	58	FAULTB2	94	ANA6	130	SCLK0
23	A12	59	D0	95	ANA7	131	MISO0
24	A13	60	D1	96	TEMP_SENSE	132	MOSI0
25	A14	61	FAULTB3	97	V_{REFLO}	133	D11



DIM	MILLIMETERS MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	22.00 BSC	
D1	20.00 BSC	
e	0.50 BSC	
E	22.00 BSC	
E1	20.00 BSC	
L	0.45	0.75
L1	1.00 REF	
L2	0.50 REF	
R1	0.13	0.20
R2	0.13	---
S	0.25 REF	
θ	0°	7°
θ1	0°	---
θ2	12° REF	

Figure 11-3 144-pin LQFP Mechanical Information

where:

T_T = Thermocouple temperature on top of package (^oC)
Ψ_{JT} = Thermal characterization parameter (^oC)/W
P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

12.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct device operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including $V_{DDA}/V_{SSA.}$ Ceramic and tantalum capacitors tend to provide better performance tolerances.

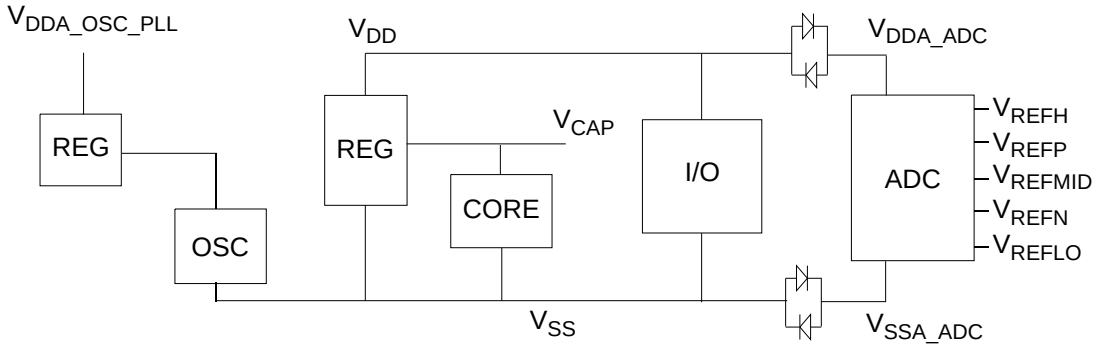


Figure 12-1 Power Management

Part 13 Ordering Information

Table 13-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 13-1 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number
MC56F8356	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	144	60	-40° to + 105° C	MC56F8356VFV60
MC56F8356	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	144	60	-40° to + 125° C	MC56F8356MFV60
MC56F8156	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	144	40	-40° to + 105° C	MC56F8156VFV
MC56F8356	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	144	60	-40° to + 105° C	MC56F8356VFVE*
MC56F8356	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	144	60	-40° to + 125° C	MC56F8356MFVE*
MC56F8156	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	144	40	-40° to + 105° C	MC56F8156VFVE*

*This package is RoHS compliant.