Renesas Electronics America Inc - R5S72620W144FP#U0 Datasheet

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Details	
Product Status	Last Time Buy
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	89
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72620w144fp-u0

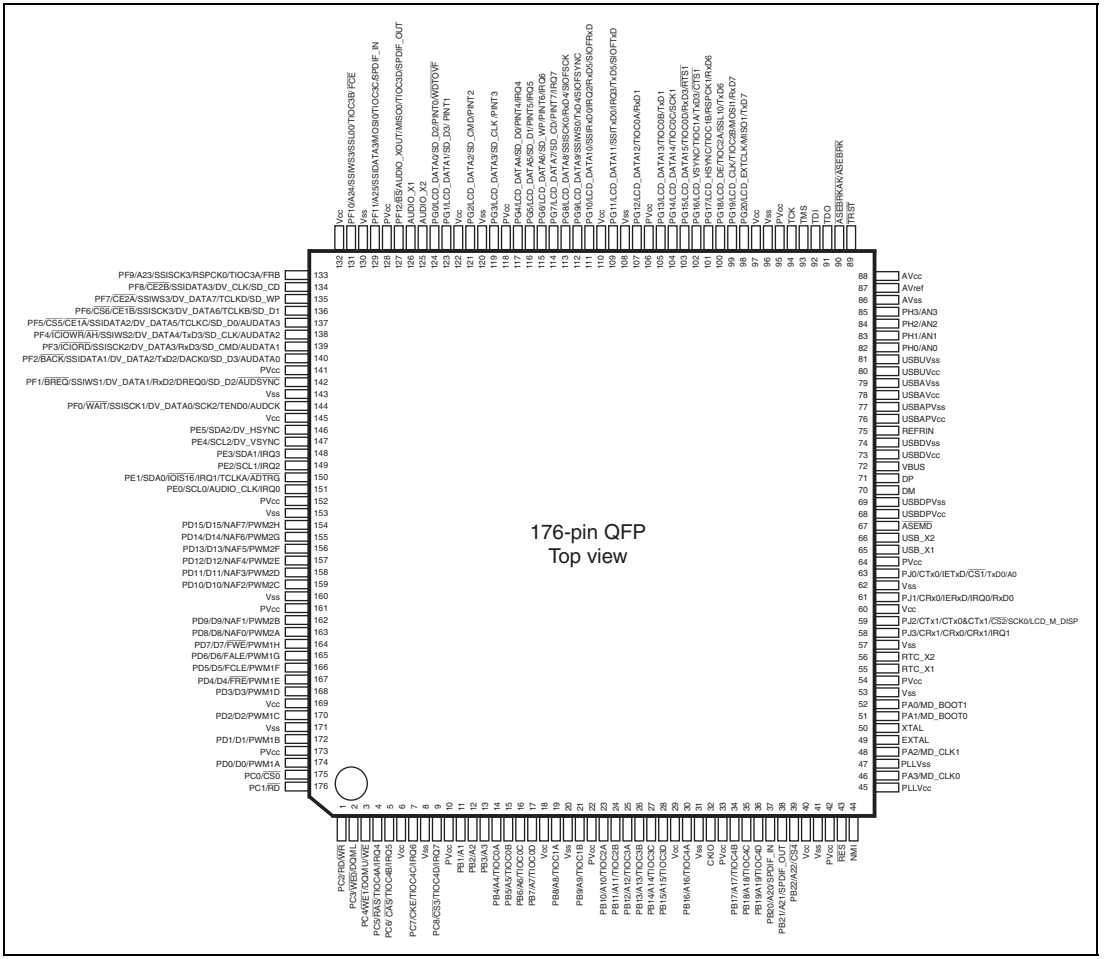

Figure 1.2 (2) Pin Assignment for the SH7262 Group (640-Kbyte Version)

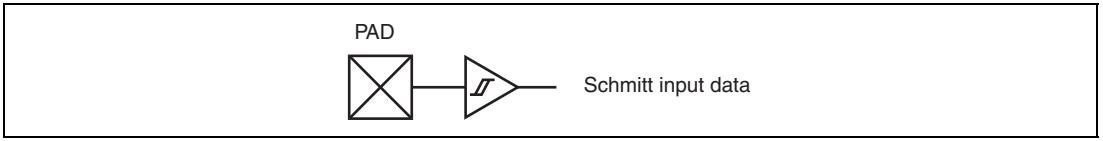

Figure 1.3 (1) Simplified Circuit Diagram (Schmitt Input Buffer)

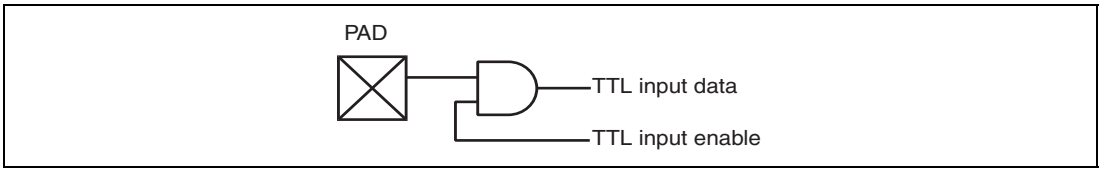

Figure 1.3 (2) Simplified Circuit Diagram (TTL AND Input Buffer)

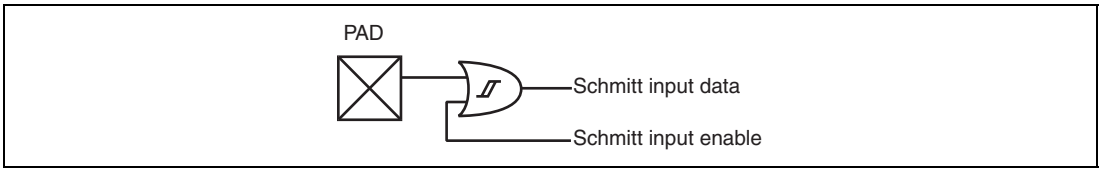

Figure 1.3 (3) Simplified Circuit Diagram (Schmitt OR Input Buffer)

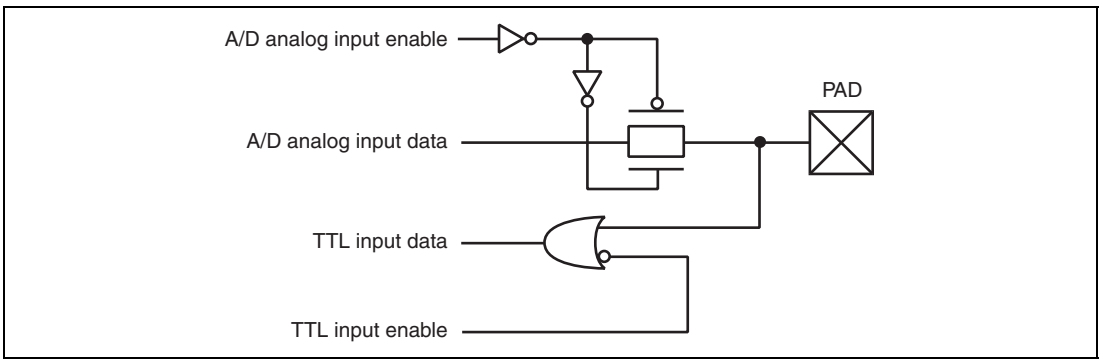

Figure 1.3 (4) Simplified Circuit Diagram (TTL OR Input and A/D Input Buffer)

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Interrupt priority register 18	IPR18	R/W	H'0000	H'FFFE0C18	16, 32
Interrupt priority register 19	IPR19	R/W	H'0000	H'FFFE0C1A	16, 32
Interrupt priority register 20	IPR20	R/W	H'0000	H'FFFE0C1C	16, 32
Interrupt priority register 21	IPR21	R/W	H'0000	H'FFFE0C1E	16, 32
Interrupt priority register 22	IPR22	R/W	H'0000	H'FFFE0C20	16, 32

Notes: 1. For 1-Mbyte version, when the NMI pin is high, becomes H'8000; when low, becomes H'0000. For 640-Kbyte version, when the pin is high, becomes H'8001; when low, becomes H'0001.
2. Only 0 can be written after reading 1, to clear the flag.

8.2 Register Descriptions

Table 8.2 shows the register configuration of the cache.

Table 8.2 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Cache control register 1	CCR1	R/W	H'00000000	H'FFFC1000	32
Cache control register 2	CCR2	R/W	H'00000000	H'FFFC1004	32

8.2.1 Cache Control Register 1 (CCR1)

The instruction cache is enabled or disabled using the ICE bit. The ICF bit controls disabling of all instruction cache entries. The operand cache is enabled or disabled using the OCE bit. The OCF bit controls disabling of all operand cache entries. The WT bit selects either write-through mode or write-back mode for operand cache.

Programs that change the contents of CCR1 should be placed in a cache-disabled space, and a cache-enabled space should be accessed after reading the contents of CCR1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	ICF	-	-	ICE	-	-	-	-	OCF	-	WT	OCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R	R	R/W	R	R	R	R	R/W	R	R/W	R/W

8.4.3 Usage Examples

(1) Invalidating Specific Entries

Specific cache entries can be invalidated by writing 0 to the entry's V bit in the memory mapping cache access. When the A bit is 1, the tag address specified by the write data is compared to the tag address within the cache selected by the entry address, and data is written to the bits V and U specified by the write data when a match is found. If no match is found, there is no operation. When the V bit of an entry in the address array is set to 0, the entry is written back if the entry's U bit is 1.

An example when a write data is specified in R0 and an address is specified in R1 is shown below.

```
; R0=H'0110 0010; tag address(28-11)=B'0 0001 0001 0000 0000 0, U=0, V=0
; R1=H'F080 0088; operand cache address array access, entry=B'000 1000, A=1
;
 MOV.L  R0,@R1
```

(2) Reading the Data of a Specific Entry

The data section of a specific cache entry can be read by the memory mapping cache access. The longword indicated in the data field of the data array in figure 8.4 is read into the register.

An example when an address is specified in R0 and data is read in R1 is shown below.

```
; R0=H'F100 004C; instruction cache data array access, entry=B'000 0100,
; Way=0, longword address=3
;
 MOV.L  @R0,R1
```

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Transfer Source	Transfer Destination	Bus Mode
RS[3:0]	MID	RID					
1000	000010	01	Renesas SPDIF interface	SPDIFTXI (DMA transfer from transmission module)	Any	TDAD	Cycle steal
		10		SPDIFRXI (DMA transfer to reception module)	RDAD	Any	
	000100	01	SD host interface	SD_BUF write	Any	Data register	
		10		SD_BUF read	Data register	Any	
	000110	01	Clock synchronous serial I/O with FIFO	TXI transmit data transfer)	Any	SITDR	
		10		RXI (receive data transfer)	SIRDR	Any	
	001000	01	Serial sound interface Channel 0	SSITXI0 (transmit data empty)	Any	SSIFTDR_0	
		10		SSIRXI0 (receive data full)	SSIFRDR_0	Any	
	001001	11	Serial sound interface Channel 1	SSIRTI1 (transmit data empty)	Any	SSIFTDR_1	
				SSIRTI1 (receive data full)	SSIFRDR_1	Any	
	001010	11	Serial sound interface Channel 2	SSIRTI2 (transmit data empty)	Any	SSIFTDR_2	
				SSIRTI2 (receive data full)	SSIFRDR_2	Any	
	001011	11	Serial sound interface Channel 3	SSIRTI3 (transmit data empty)	Any	SSIFTDR_3	
				SSIRTI3 (receive data full)	SSIFRDR_3	Any	
	001100	11	Motor control PWM timer Channel 1	CMI1 (PWM compare match)	Any	PWBFR1	
	001101	11	Motor control PWM timer Channel 2	CMI2 (PWM compare match)	Any	PWBFR2	
	010000	01	Sampling rate converter Channel 0	IDEI0 (input data empty)	Any	SRCIDR_0	
		10		ODFI0 (output data full)	SRCODR_0	Any	

15.3.8 Bit Rate Register (SCBRR)

SCBRR is an 8-bit register that is used with the CKS1 and CKS0 bits in the serial mode register (SCSMR) and the BGDM and ABCS bits in the serial extension mode register (SCEMR) to determine the serial transmit/receive bit rate.

The CPU can always read and write to SCBRR. SCBRR is initialized to H'FF by a power-on reset. Each channel has independent baud rate generator control, so different values can be set in eight channels.

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The SCBRR setting is calculated as follows:

- Asynchronous mode:

When baud rate generator operates in normal mode (when the BGDM bit of SCEMR is 0):

$$N = \frac{P\phi}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$ (Operation on a base clock with a frequency of 16 times the bit rate)

$$N = \frac{P\phi}{32 \times 2^{2n-1} \times B} \times 10^6 - 1$$ (Operation on a base clock with a frequency of 8 times the bit rate)

When baud rate generator operates in double speed mode (when the BGDM bit of SCEMR is 1):

$$N = \frac{P\phi}{32 \times 2^{2n-1} \times B} \times 10^6 - 1$$ (Operation on a base clock with a frequency of 16 times the bit rate)

$$N = \frac{P\phi}{16 \times 2^{2n-1} \times B} \times 10^6 - 1$$ (Operation on a base clock with a frequency of 8 times the bit rate)

Figure 18.10 uses a system word length of 6 bits and a data word length of 4 bits. These settings are not possible with this module but are used only for clarification of the other configuration bits.

- Inverted Clock

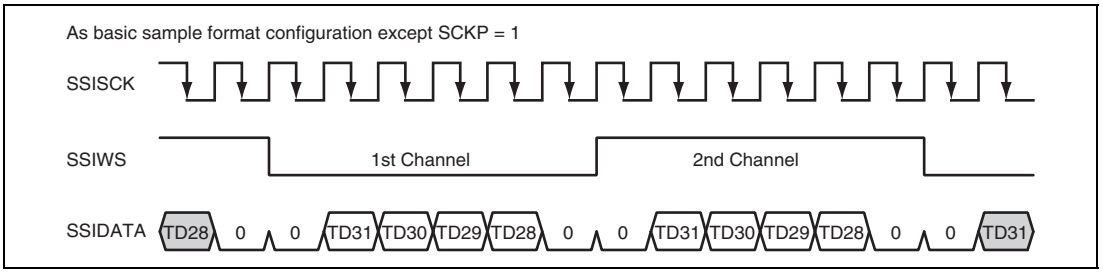

Figure 18.11 Inverted Clock

- Inverted Word Select

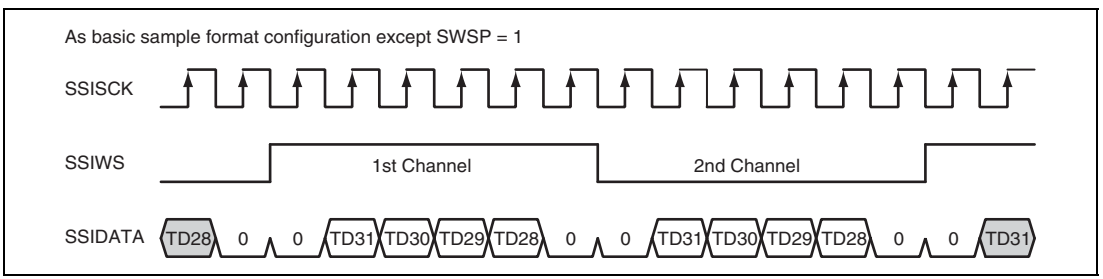

Figure 18.12 Inverted Word Select

- Inverted Padding Polarity

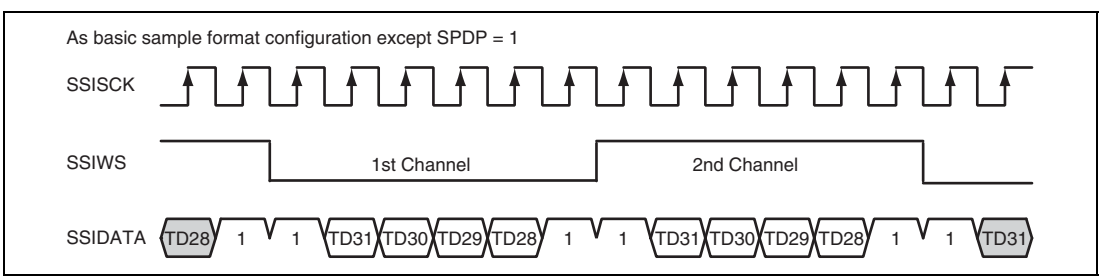

Figure 18.13 Inverted Padding Polarity

23.3.34 Post-ECC Correction Subheader: Channel Number (Byte 17) Data Register (SHEAD21)

The post-ECC correction subheader: channel number (byte 17) data register (SHEAD21) indicates the channel number value in the subheader after ECC correction (byte 17).

Bit:	7	6	5	4	3	2	1	0
	SHEAD21[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SHEAD21 [7:0]	All 0	R	Indicate channel number value in the subheader after ECC correction (byte 17).

23.3.35 Post-ECC Correction Subheader: Sub-Mode (Byte 18) Data Register (SHEAD22)

The post-ECC correction subheader: sub-mode (byte 18) data register (SHEAD22) indicates the sub-mode value in the subheader after ECC correction (byte 18).

Bit:	7	6	5	4	3	2	1	0
	SHEAD22[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SHEAD22 [7:0]	All 0	R	Indicates sub-mode value in the subheader after ECC correction (byte 18).

Bit	Bit Name	Initial Value	R/W	Description
22	4ECCCORRECT	0	R/W	4-Symbol ECC Circuit Correction Execution Specifies to execute error correction for a single sector when the 4-symbol ECC circuit is used. This module suspends sector reading on detection of an ECC error and starts error pattern generation by the 4-symbol ECC circuit. 0: Error pattern is not output but only ECC is output. 1: Reading of sectors is suspended on detection of an ECC error.
21	BUSYON	0	R/W	Busy Select Specifies whether to release the external bus mastership while the FRB pin is busy. The $\overline{\text{FCE}}$ pin, however, is negated regardless of the busy/ready state upon completion of a necessary process. For details, see section 25.7.1, External Bus Mastership Release Timing. 0: Holds the bus mastership while the FRB pin is busy. 1: Releases the bus mastership while the FRB pin is busy. Note: Some flash memory devices do not allow the $\overline{\text{FCE}}$ pin to be negated during the busy state.
20	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18	SNAND	0	R/W	Large-Capacity NAND Flash Memory Select This bit is used to specify 1-Gbit or larger NAND flash memory with the page configuration of 2048 + 64 bytes. 0: When flash memory with the page configuration of 512 + 16 bytes is used. 1: When NAND flash memory with the page configuration of 2048 + 64 is used.

Bit	Bit Name	Initial Value	R/W	Description
19 to 0	RBTIMCNT[19:0]	H'00000	R	Ready Busy Timeout Counter When the FRB pin is placed in a busy state, the values of the bits RBTMOUT[19:0] in FLBSYTMR are copied to these bits. These bits are counted down while the FRB pin is busy. A timeout error occurs when these bits are decremented to 0.

25.3.11 Data FIFO Register (FLDTFIFO)

FLDTFIFO is used to read or write the data FIFO area.

In DMA transfer, this register must be specified as the destination or source.

Note that the direction of read or write specified by the SELRW bit in FLCMDCR must match that specified in this register. When changing the read/write direction, FLDTFIFO should be cleared by setting the AC0CLR bit in FLINTDMACR before use.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DTFO[31:16]															
Initial value:	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTFO[15:0]															
Initial value:	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DTFO[31:0]	H'xxxxxxxx	R/W	Data FIFO Area Read/Write Data In write: Data in this register is written to the data FIFO area. In read: Data read from the data FIFO area is stored in this register.

25.7 Usage Notes

25.7.1 External Bus Mastership Release Timing

This module negates $\overline{\text{FCE}}$ regardless of the busy/ready state when having completed a necessary process. With bit 21 (BUSYON) set to 0 in the common control register (FLCMNCR), this module negates $\overline{\text{FCE}}$ and releases the bus mastership even during the busy state upon completion of the process. With BUSYON = 0, setting bit 24 (DOSR) in the command control register (FLCMDCR) to 1 to read the status enables acquiring the bus mastership even during the busy state.

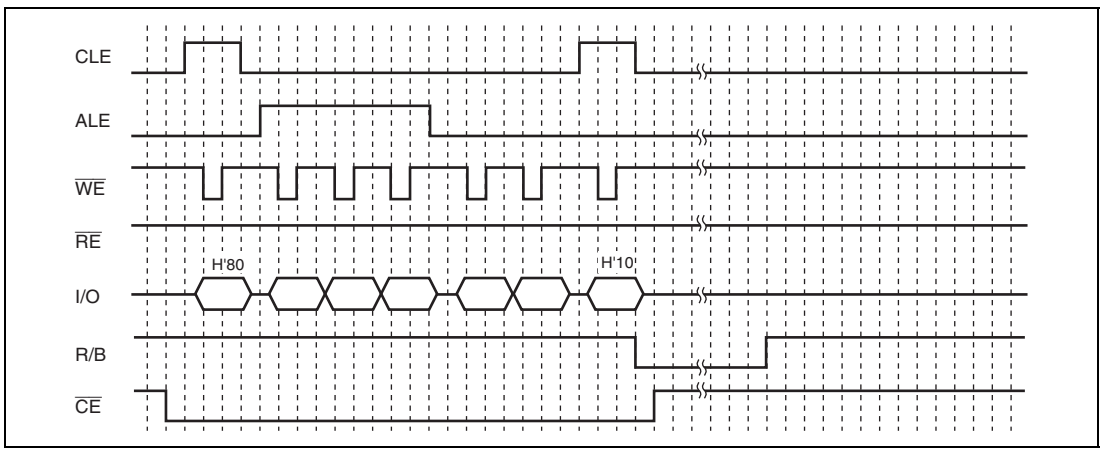

Figure 25.17 BUSYON = 0, DOSR = 0 (Writing to Flash Memory)

26.3.11 Interrupt Enable Register 1 (INTENB1)

INTENB1 is a register that enables or disables the various interrupts when the host controller function is selected. On detecting the interrupt corresponding to the bit in this register that has been set to 1, this module generates the USB interrupt.

This module sets 1 to each status bit in INTSTS1 when a detection condition of the corresponding interrupt source has been satisfied regardless of the set value in INTENB1 (regardless of whether the interrupt output is enabled or disabled).

While the status bit in INTSTS1 corresponding to the interrupt source indicates 1, this module generates the USB interrupt when the corresponding interrupt enable bit in INTENB1 is modified from 0 to 1.

When the function controller function is selected, the interrupts should not be enabled. This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	BCHGE	0	R/W	USB Bus Change Interrupt Enable Enables or disables the USB interrupt request when the BCHG interrupt is detected. 0: Interrupt request disabled 1: Interrupt request enabled
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
12	DTCHE	0	R/W	Disconnection Detection Interrupt Enable Enables or disables the USB interrupt request when the DTCH interrupt is detected. 0: Interrupt request disabled 1: Interrupt request enabled

Table 26.21 Buffer Memory Map

Buffer Memory Number	Buffer Size	Pipe Setting	Note
H'0 to H'3	256 bytes	Fixed area only for the DCP	Single buffer, continuous transfers enabled
H'4	64 bytes	Fixed area for PIPE6	Single buffer
H'5	64 bytes	Fixed area for PIPE7	Single buffer
H'6	64 bytes	Fixed area for PIPE8	Single buffer
H'7	64 bytes	Fixed area for PIPE9	Single buffer
H'8 to H'7F	Up to 7616 bytes	PIPE1 to PIPE5 user area	Double buffer can be set, continuous transfers enabled

(d) Auto Buffer Clear Mode Function

With this module, all of the received data packets are discarded if the ACLRM bit in PIPEnCTR is set to 1. If a normal data packet has been received, the ACK response is returned to the host controller. This function can be set only in the buffer memory reading direction.

Also, if the ACLRM bit is set to 1 and then to 0, the buffer memory of the selected pipe can be cleared regardless of the access direction.

(e) Buffer Memory Specifications (Single/Double Setting)

Either a single or double buffer can be selected for PIPE1 to PIPE5, using the DBLB bit in PIPECFG. The double buffer is a function that assigns two memory areas specified with the BUFSIZE bit in PIPEBUF to the same pipe. Figure 26.10 shows an example of buffer memory settings for this module.

Bit	Bit Name	Initial Value	R/W	Description
6	SUB_SCALE_V	0	R/W	Specifies further scaling of video by multiplying the SCALE_V scaling rate by 6/7. 0: ×1 1: ×6/7
5, 4	SCALE_V[1:0]	00	R/W	These bits specify the vertical scaling rate. Be sure to set to 00 in the video recording mode. 00: ×1/2 01: ×1/3 10: ×1/4 11: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	SUB_SCALE_H	0	R/W	Specifies further scaling of video by multiplying the SCALE_H scaling rate by 6/7. 0: ×1 1: ×6/7
1, 0	SCALE_H[1:0]	00	R/W	These bits specify the horizontal scaling rate. 00: ×1/2 01: ×1/3 10: ×2/3 11: ×1/4

Note: The width of a valid image after horizontal scaling is always an even value.

Bit	Bit Name	Initial Value	R/W	Description
9	PG10F	0	R/(W)*	PG10 Flag 0: No change on the PG10 pin 1: Change on the PG10 pin Note: For 1-Mbyte version, this bit is reserved and always read as 0. The write value should always be 0.
8	NMIF	0	R/(W)*	NMI Flag 0: No interrupt on NMI pin 1: Interrupt on NMI pin
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	RTCARF	0	R/(W)*	RTCAR Flag 0: No realtime clock alarm interrupt generated 1: Realtime clock alarm Interrupt generated
5	PC8F	0	R/(W)*	PC8 Flag 0: No change on the PC8 pin 1: Change on the PC8 pin
4	PC7F	0	R/(W)*	PC7 Flag 0: No change on the PC7 pin 1: Change on the PC7 pin
3	PC6F	0	R/(W)*	PC6 Flag 0: No change on the PC6 pin 1: Change on the PC6 pin
2	PC5F	0	R/(W)*	PC5 Flag 0: No change on the PC5 pin 1: Change on the PC5 pin
1	PJ3F	0	R/(W)*	PJ3 Flag 0: No change on the PJ3 pin 1: Change on the PJ3 pin
0	PJ1F	0	R/(W)*	PJ1 Flag 0: No change on the PJ1 pin 1: Change on the PJ1 pin

Note: * Only 0 can be written after reading 1 to clear the flag.

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
Direct memory access controller	RDMATCR_15	—	—	—	—	—	—	—	—
	DMAOR	—	—	CMS[1]	CMS[0]	—	—	PR[1]	PR[0]
		—	—	—	—	—	AE	NMIF	DME
	DMARS0	CH1MID[5]	CH1MID[4]	CH1MID[3]	CH1MID[2]	CH1MID[1]	CH1MID[0]	CH1RID[1]	CH1RID[0]
		CH0MID[5]	CH0MID[4]	CH0MID[3]	CH0MID[2]	CH0MID[1]	CH0MID[0]	CH0RID[1]	CH0RID[0]
	DMARS1	CH3MID[5]	CH3MID[4]	CH3MID[3]	CH3MID[2]	CH3MID[1]	CH3MID[0]	CH3RID[1]	CH3RID[0]
		CH2MID[5]	CH2MID[4]	CH2MID[3]	CH2MID[2]	CH2MID[1]	CH2MID[0]	CH2RID[1]	CH2RID[0]
	DMARS2	CH5MID[5]	CH5MID[4]	CH5MID[3]	CH5MID[2]	CH5MID[1]	CH5MID[0]	CH5RID[1]	CH5RID[0]
		CH4MID[5]	CH4MID[4]	CH4MID[3]	CH4MID[2]	CH4MID[1]	CH4MID[0]	CH4RID[1]	CH4RID[0]
	DMARS3	CH7MID[5]	CH7MID[4]	CH7MID[3]	CH7MID[2]	CH7MID[1]	CH7MID[0]	CH7RID[1]	CH7RID[0]
		CH6MID[5]	CH6MID[4]	CH6MID[3]	CH6MID[2]	CH6MID[1]	CH6MID[0]	CH6RID[1]	CH6RID[0]
	DMARS4	CH9MID[5]	CH9MID[4]	CH9MID[3]	CH9MID[2]	CH9MID[1]	CH9MID[0]	CH9RID[1]	CH9RID[0]
		CH8MID[5]	CH8MID[4]	CH8MID[3]	CH8MID[2]	CH8MID[1]	CH8MID[0]	CH8RID[1]	CH8RID[0]
	DMARS5	CH11MID[5]	CH11MID[4]	CH11MID[3]	CH11MID[2]	CH11MID[1]	CH11MID[0]	CH11RID[1]	CH11RID[0]
		CH10MID[5]	CH10MID[4]	CH10MID[3]	CH10MID[2]	CH10MID[1]	CH10MID[0]	CH10RID[1]	CH10RID[0]
	DMARS6	CH13MID[5]	CH13MID[4]	CH13MID[3]	CH13MID[2]	CH13MID[1]	CH13MID[0]	CH13RID[1]	CH13RID[0]
		CH12MID[5]	CH12MID[4]	CH12MID[3]	CH12MID[2]	CH12MID[1]	CH12MID[0]	CH12RID[1]	CH12RID[0]
	DMARS7	CH15MID[5]	CH15MID[4]	CH15MID[3]	CH15MID[2]	CH15MID[1]	CH15MID[0]	CH15RID[1]	CH15RID[0]
		CH14MID[5]	CH14MID[4]	CH14MID[3]	CH14MID[2]	CH14MID[1]	CH14MID[0]	CH14RID[1]	CH14RID[0]
Multi-function timer pulse unit 2	TCR_0	CCLR[2]	CCLR[1]	CCLR[0]	CKEG[1]	CKEG[0]	TPSC[2]	TPSC[1]	TPSC[0]
	TMDR_0	—	BFE	BFB	BFA	MD[3]	MD[2]	MD[1]	MD[0]
	TIORH_0	IOB[3]	IOB[2]	IOB[1]	IOB[0]	IOA[3]	IOA[2]	IOA[1]	IOA[0]
	TIORL_0	IOD[3]	IOD[2]	IOD[1]	IOD[0]	IOC[3]	IOC[2]	IOC[1]	IOC[0]
	TIER_0	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA
	TSR_0	—	—	—	TCFV	TGFD	TGFC	TGFB	TGFA
	TCNT_0								

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
NAND flash memory controller	FLHOLDCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	HOLDEN
	FL4ECCRES1	—	—	—	—	—	—	LOC1[9]	LOC1[8]
		LOC1[7]	LOC1[6]	LOC1[5]	LOC1[4]	LOC1[3]	LOC1[2]	LOC1[1]	LOC1[0]
		—	—	—	—	—	—	PAT1[9]	PAT1[8]
		PAT1[7]	PAT1[6]	PAT1[5]	PAT1[4]	PAT1[3]	PAT1[2]	PAT1[1]	PAT1[0]
	FL4ECCRES2	—	—	—	—	—	—	LOC2[9]	LOC2[8]
		LOC2[7]	LOC2[6]	LOC2[5]	LOC2[4]	LOC2[3]	LOC2[2]	LOC2[1]	LOC2[0]
		—	—	—	—	—	—	PAT2[9]	PAT2[8]
		PAT2[7]	PAT2[6]	PAT2[5]	PAT2[4]	PAT2[3]	PAT2[2]	PAT2[1]	PAT2[0]
	FL4ECCRES3	—	—	—	—	—	—	LOC3[9]	LOC3[8]
		LOC3[7]	LOC3[6]	LOC3[5]	LOC3[4]	LOC3[3]	LOC3[2]	LOC3[1]	LOC3[0]
		—	—	—	—	—	—	PAT3[9]	PAT3[8]
		PAT3[7]	PAT3[6]	PAT3[5]	PAT3[4]	PAT3[3]	PAT3[2]	PAT3[1]	PAT3[0]
	FL4ECCRES4	—	—	—	—	—	—	LOC4[9]	LOC4[8]
		LOC4[7]	LOC4[6]	LOC4[5]	LOC4[4]	LOC4[3]	LOC4[2]	LOC4[1]	LOC4[0]
		—	—	—	—	—	—	PAT4[9]	PAT4[8]
		PAT4[7]	PAT4[6]	PAT4[5]	PAT4[4]	PAT4[3]	PAT4[2]	PAT4[1]	PAT4[0]
	FL4ECCCR	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	4ECCFA	4ECCEND	4ECCEXST
	FL4ECCCNT	—	—	—	—	—	ERRCNT[10]	ERRCNT[9]	ERRCNT[8]
		ERRCNT[7]	ERRCNT[6]	ERRCNT[5]	ERRCNT[4]	ERRCNT[3]	ERRCNT[2]	ERRCNT[1]	ERRCNT[0]
		—	—	—	—	—	—	—	—
		—	—	—	—	—	ERRMAX[2]	ERRMAX[1]	ERRMAX[0]

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
USB 2.0 host/function module	SYSCFG	—	—	—	—	—	SCKE	—	—
		HSE	DCFM	DMRPD	DPRPU	—	—	—	USBE
	BUSWAIT		—	—	—	—	—	—	—
		—	—	—	—	BWAIT[3]	BWAIT[2]	BWAIT[1]	BWAIT[0]
	SYSSTS	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	LNST[1]	LNST[0]
	DVSTCTR	—	—	—	—	—	—	—	WKUP
		RWUPE	USBRST	RESUME	UACT	—	RHST[2]	RHST[1]	RHST[0]
	TESTMODE	—	—	—	—	—	—	—	—
		—	—	—	—	UTST[3]	UTST[2]	UTST[1]	UTST[0]
	D0FBCFG	—	—	—	—	—	—	—	—
		—	—	—	TENDE	—	—	—	—
	D1FBCFG	—	—	—	—	—	—	—	—
		—	—	—	TENDE	—	—	—	—
	CFIFO	FIFOPORT [31]	FIFOPORT [30]	FIFOPORT [29]	FIFOPORT [28]	FIFOPORT [27]	FIFOPORT [26]	FIFOPORT [25]	FIFOPORT [24]
		FIFOPORT [23]	FIFOPORT [22]	FIFOPORT [21]	FIFOPORT [20]	FIFOPORT [19]	FIFOPORT [18]	FIFOPORT [17]	FIFOPORT [16]
		FIFOPORT [15]	FIFOPORT [14]	FIFOPORT [13]	FIFOPORT [12]	FIFOPORT [11]	FIFOPORT [10]	FIFOPORT[9]	FIFOPORT[8]
		FIFOPORT[7]	FIFOPORT[6]	FIFOPORT[5]	FIFOPORT[4]	FIFOPORT[3]	FIFOPORT[2]	FIFOPORT[1]	FIFOPORT[0]
	D0FIFO	FIFOPORT [31]	FIFOPORT [30]	FIFOPORT [29]	FIFOPORT [28]	FIFOPORT [27]	FIFOPORT [26]	FIFOPORT [25]	FIFOPORT [24]
		FIFOPORT [23]	FIFOPORT [22]	FIFOPORT [21]	FIFOPORT [20]	FIFOPORT [19]	FIFOPORT [18]	FIFOPORT [17]	FIFOPORT [16]
		FIFOPORT [15]	FIFOPORT [14]	FIFOPORT [13]	FIFOPORT [12]	FIFOPORT [11]	FIFOPORT [10]	FIFOPORT[9]	FIFOPORT[8]
		FIFOPORT[7]	FIFOPORT[6]	FIFOPORT[5]	FIFOPORT[4]	FIFOPORT[3]	FIFOPORT[2]	FIFOPORT[1]	FIFOPORT[0]

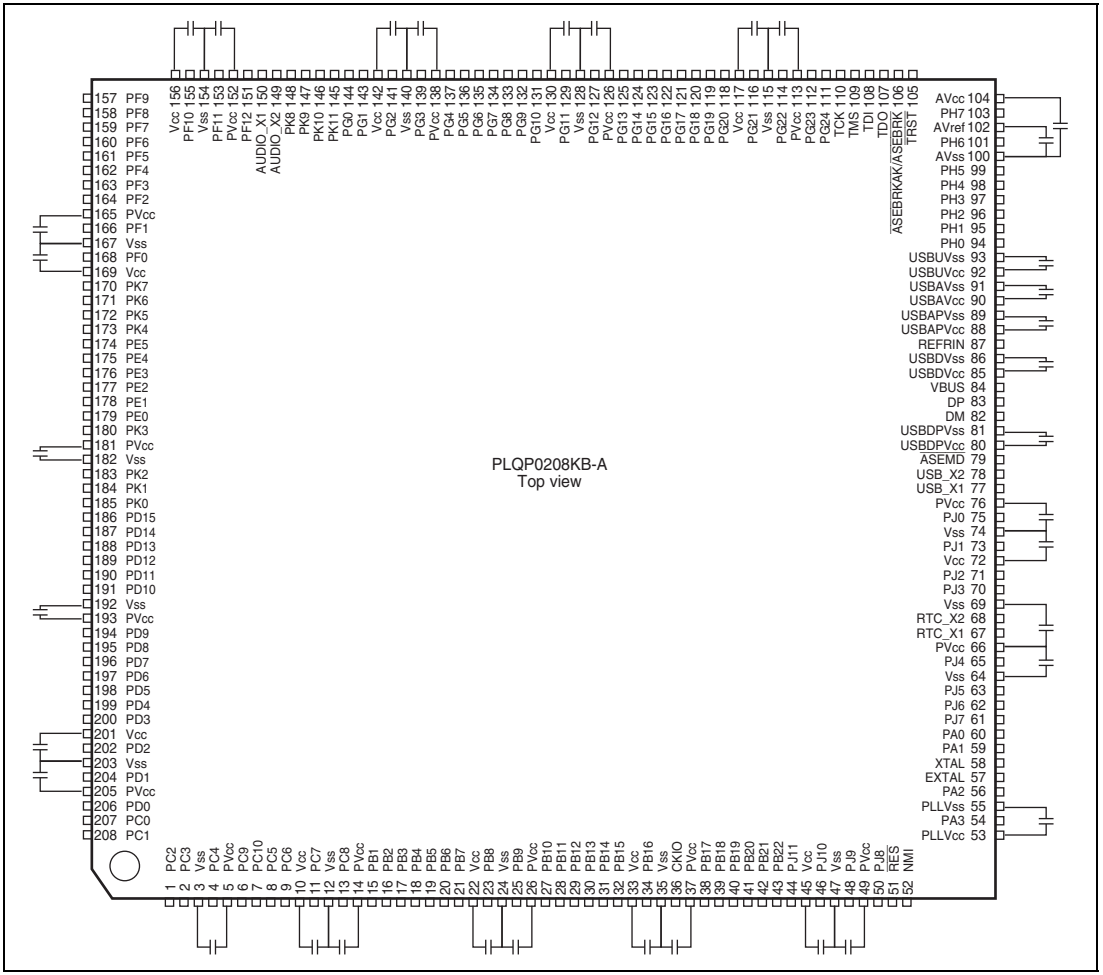

Figure 38.2 Example of Externally Allocated Capacitors in the SH7264 Group