Renesas Electronics America Inc - R5S72621P144FP#UZ Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	89
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72621p144fp-uz

6.2 Resets

6.2.1 Input/Output Pins

Table 6.5 shows the pin configuration.

Table 6.5 Pin Configuration

Pin Name	Symbol	I/O	Function
Power-on reset	$\overline{RES}$	Input	When this pin is driven low, this LSI shifts to the power-on reset processing

6.2.2 Types of Reset

A reset is the highest-priority exception handling source. There are two kinds of reset, power-on and manual. As shown in table 6.6, the CPU state is initialized in both a power-on reset and a manual reset. The FPU state is initialized by a power-on reset, but not by a manual reset. On-chip peripheral module registers except a few registers are also initialized by a power-on reset, but not by a manual reset.

Table 6.6 Reset States

Type	Conditions for Transition to Reset State			Internal States				
	$\overline{RES}$	User Debugging Interface Command	Watchdog Timer Overflow	CPU	Other Modules	On-Chip High-Speed RAM	On-Chip Large-Capacity RAM (Excluding On-Chip Data Retention RAM)	On-Chip Data Retention RAM
Power-on reset	Low	—	—	Initialized	Initialized	Initialized or Retained contents*2	Initialized or Retained contents*3	Initialized or Retained contents*4, *5
	High	User debugging interface reset assert command is set	—	Initialized	Initialized	Initialized or Retained contents*2	Initialized or Retained contents*3	Initialized or Retained contents*4
	High	Command other than user debugging interface reset assert is set	Power-on reset	Initialized	*1	Initialized or Retained contents*2	Initialized or Retained contents*3	Initialized or Retained contents*4

6. PCMCIA direct interface
   - Supports the IC memory card and I/O card interface defined in JEIDA specifications Ver. 4.2 (PCMCIA2.1 Rev. 2.1).
   - Wait-cycle insertion controllable by program.
7. SRAM interface with byte selection
   - Can connect directly to a SRAM with byte selection.
8. Burst ROM interface (clocked synchronous)
   - Can connect directly to a burst ROM of the clocked synchronous type.
9. Bus arbitration
   - Shares all of the resources with other CPU and outputs the bus enable after receiving the bus request from external devices.
10. Refresh function
    - Supports the auto-refresh and self-refresh functions.
    - Specifies the refresh interval using the refresh counter and clock selection.
    - Can execute concentrated refresh by specifying the refresh counts (1, 2, 4, 6, or 8).
11. Usage as interval timer for refresh counter
    - Generates an interrupt request at compare match.

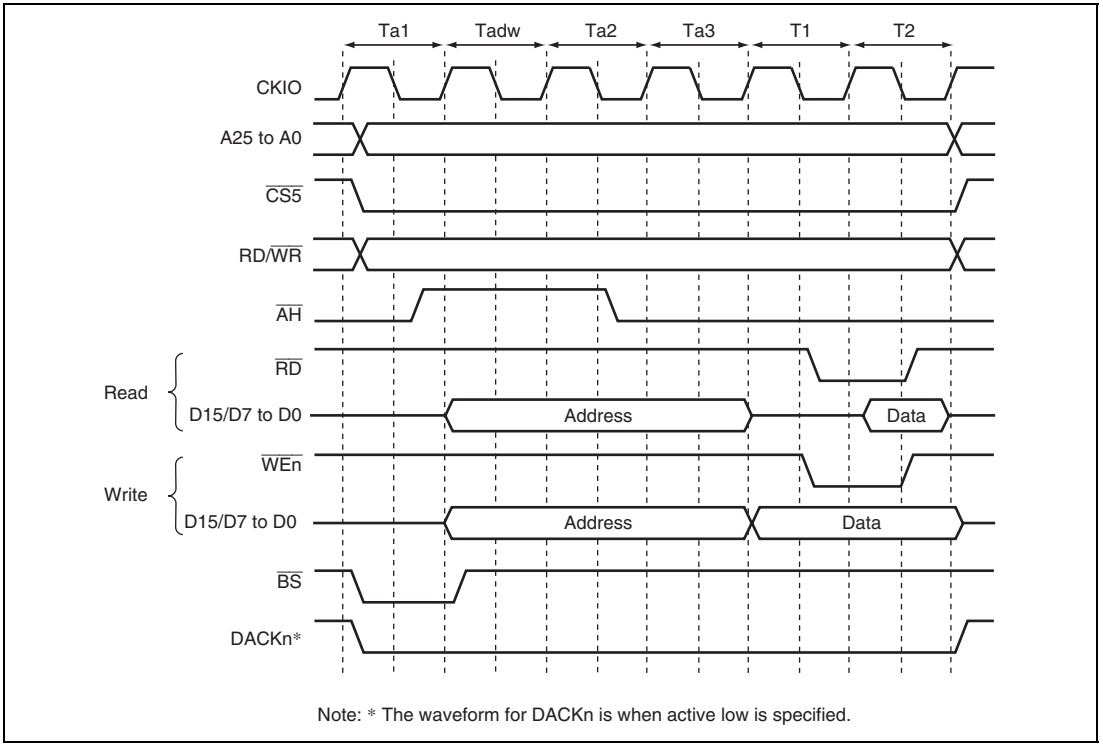


Figure 9.12 Access Timing for MPX Space (Address Cycle Wait 1, Data Cycle No Wait)

CHCR	DMARS		DMA Transfer Request Source	DMA Transfer Request Signal	Transfer Source	Transfer Destination	Bus Mode
RS[3:0]	MID	RID					
1000	010001	01	Sampling rate converter Channel 1	IDEI1 (input data empty)	Any	SRCIDR_1	Cycle steal
		10		ODFI1 (output data full)	SRCODR_1	Any	
	010100	01	Renesas serial peripheral interface Channel 0	SPTI0 (transmit buffer empty)	Any	SPDR_0	
		10		SPRI0 (receive buffer full)	SPDR_0	Any	
	010101	01	Renesas serial peripheral interface Channel 1	SPTI1 (transmit buffer empty)	Any	SPDR_1	
		10		SPRI1 (receive buffer full)	SPDR_1	Any	
	011000	01	I^2C bus interface 3 Channel 0	TXI0 (transmit data empty)	Any	ICDRT_0	
		10		RXI0 (receive data full)	ICDRR_0	Any	
	011001	01	I^2C bus interface 3 Channel 1	TXI1 (transmit data empty)	Any	ICDRT_1	
		10		RXI1 (receive data full)	ICDRR_1	Any	
	011010	01	I^2C bus interface 3 Channel 2	TXI2 (transmit data empty)	Any	ICDRT_2	
		10		RXI2 (receive data full)	ICDRR_2	Any	
	011100	11	CD-ROM decoder	IREADY (decode end)	STRMDOUT	Any	Cycle steal or burst
	100000	01	Serial communication interface with FIFO Channel 0	TXI0 (transmit FIFO data empty)	Any	SCFTDR_0	Cycle steal
		10		RXI0 (receive FIFO data full)	SCFRDR_0	Any	
	100001	01	Serial communication interface with FIFO Channel 1	TXI1 (transmit FIFO data empty)	Any	SCFTDR_1	
		10		RXI1 (receive FIFO data full)	SCFRDR_1	Any	
	100010	01	Serial communication interface with FIFO Channel 2	TXI2 (transmit FIFO data empty)	Any	SCFTDR_2	
		10		RXI2 (receive FIFO data full)	SCFRDR_2	Any	

Table 11.25 TIORH_4 (Channel 4)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_4 Function**	**TIOC4A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

11.7 Usage Notes

11.7.1 Module Standby Mode Setting

Operation of this module can be disabled or enabled using the standby control register. The initial setting is for the operation to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 33, Power-Down Modes.

11.7.2 Input Clock Restrictions

The input clock pulse width must be at least 1.5 states in the case of single-edge detection, and at least 2.5 states in the case of both-edge detection. This module will not operate properly at narrower pulse widths.

In phase counting mode, the phase difference and overlap between the two input clocks must be at least 1.5 states, and the pulse width must be at least 2.5 states. Figure 11.98 shows the input clock conditions in phase counting mode.

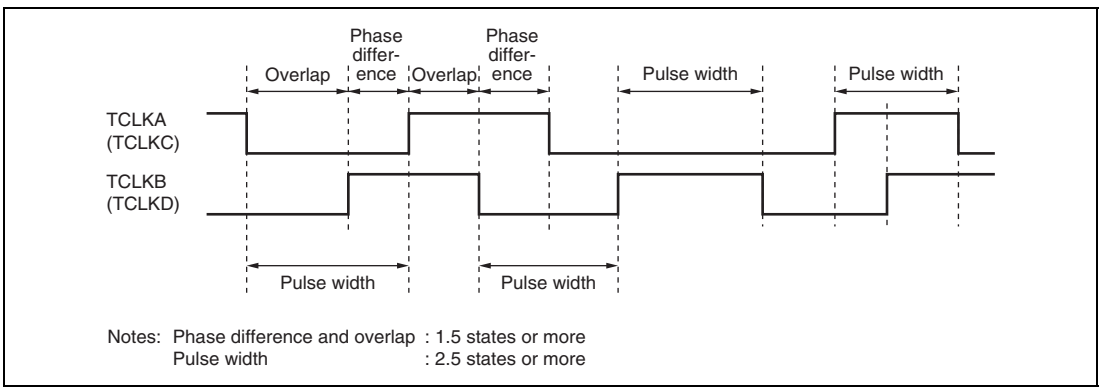
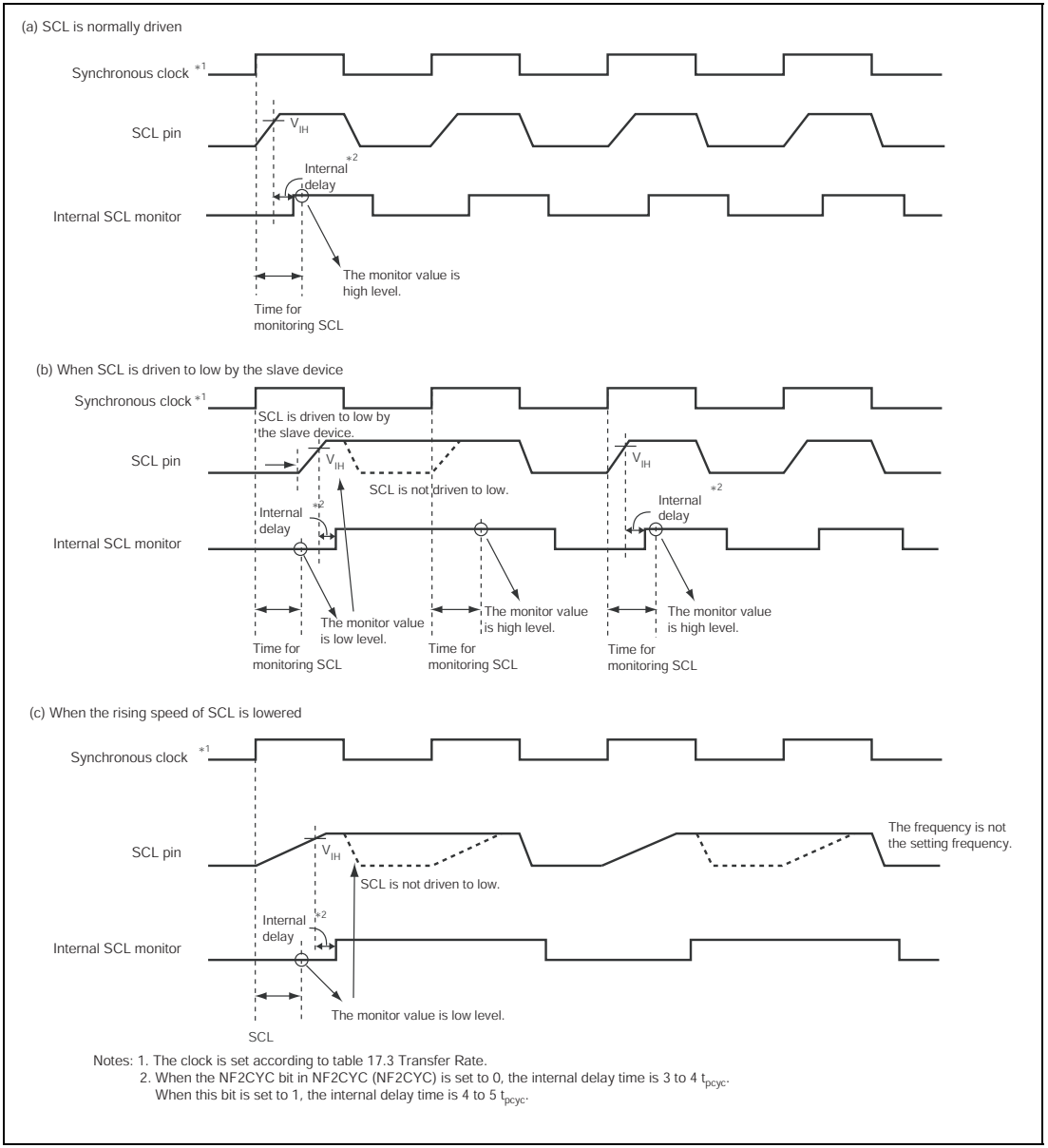


Figure 11.98 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode



Notes: 1. The clock is set according to table 17.3 Transfer Rate.
2. When the NF2CYC bit in NF2CYC (NF2CYC) is set to 0, the internal delay time is 3 to 4 t_{pcyc}.
When this bit is set to 1, the internal delay time is 4 to 5 t_{pcyc}.

Figure 17.22 Bit Synchronous Circuit Timing

Bit	Bit Name	Initial Value	R/W	Description
0	RDF	0	R/(W)*	Receive Data Full Indicates that, when the FIFO is operating for reception, the received data is transferred to the receive FIFO data register (SSIFRDR) and the number of data bytes in the FIFO data register has become greater than the receive trigger number specified by RTRG[1:0] in the FIFO control register (SSIFCR). 0: Number of received data bytes in SSIFRDR is less than the set receive trigger number. [Clearing conditions] • Power-on reset • 0 is written to RDF after the receive FIFO is empty with writing 1 to RFRST. • 0 is written to RDF after data is read from SSIFRDR until the number of data bytes in SSIFRDR becomes less than the set receive trigger number. • The direct memory access controller is activated by receive data full (RXI) interrupt, and data is read from SSIFRDR until the number of data bytes in SSIFRDR becomes less than the set receive trigger number. 1: Number of received data bytes in SSIFRDR is equal to or greater than the set receive trigger number. [Setting condition] • Data of the number of bytes that is equal to or greater than the set receive trigger number is stored in SSIFRDR.*[1] Note: 1. Since SSIFRDR is an 8-stage FIFO register, the amount of data that can be read from it while RDF = 1 is the set receive trigger number of bytes at maximum. Continuing to read data from SSIFRDR after reading all the data will result in undefined data to be read. The number of data bytes in SSIFRDR is indicated in the RDC bits in SSIFSR.

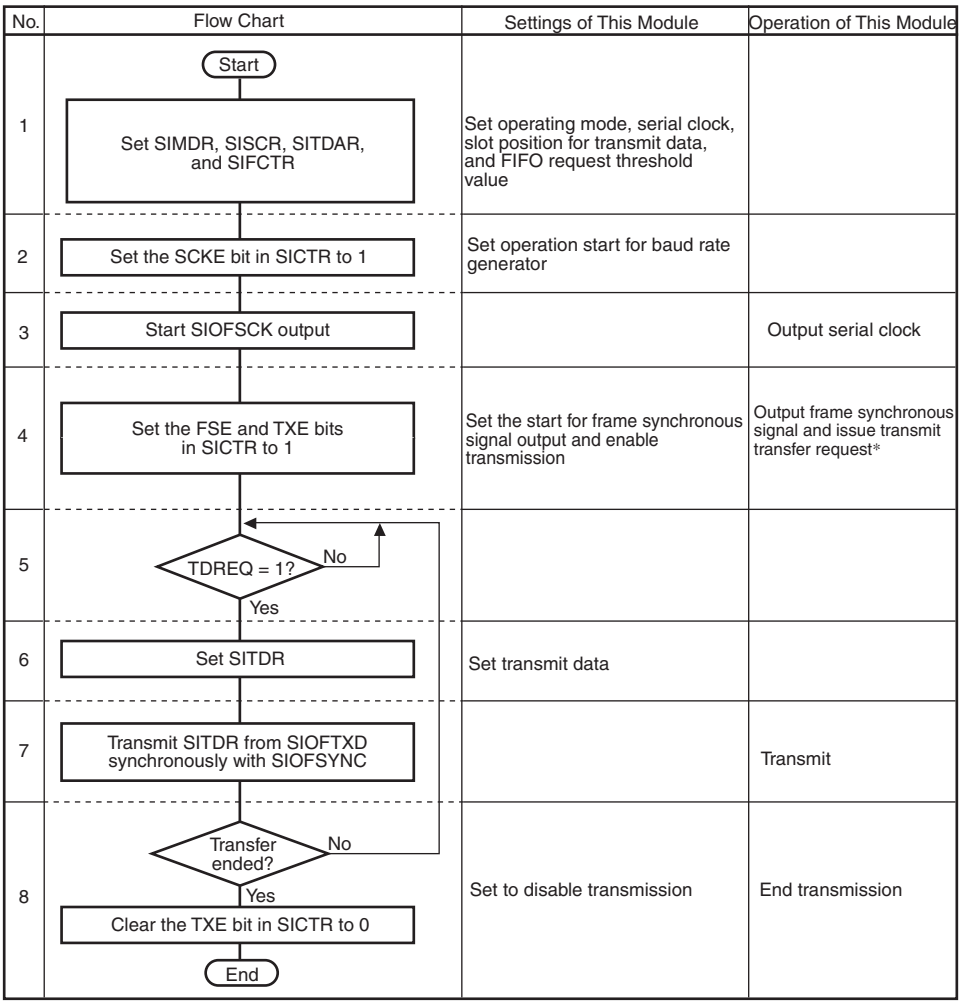
Note: * The bit can be read or written to. Writing 0 initializes the bit, but writing 1 is ignored.

Bit	Bit Name	Initial Value	R/W	Description
7	RFWM2	0	R/W	Receive FIFO Watermark
6	RFWM1	0	R/W	000: Issue a transfer request when 1 stage or more of the receive FIFO are valid.
5	RFWM0	0	R/W	001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: Issue a transfer request when 4 or more stages of the receive FIFO are valid. 101: Issue a transfer request when 8 or more stages of the receive FIFO are valid. 110: Issue a transfer request when 12 or more stages of the receive FIFO are valid. 111: Issue a transfer request when 16 stages of the receive FIFO are valid. • A transfer request to the receive FIFO is issued by the RDREQE bit in SISTR. • The receive FIFO is always used as 16 stages of the FIFO regardless of these bit settings.
4	RFUA4	0	R	Receive FIFO Usable Area
3	RFUA3	0	R	Indicate the number of stages of FIFO that can be transferred as B'00000 (empty) to B'10000 (full).
2	RFUA2	0	R	
1	RFUA1	0	R	
0	RFUA0	0	R	

19.4.6 Transmit and Receive Procedures

(1) Transmission in Master Mode

Figure 19.6 shows an example of transmission settings and operation when this module is used as a master.



Note: * To avoid occurrence of a transmit data underflow, the TXE bit should be set to 1 after setting the no. 6 transmit data,

Figure 19.6 Example of Transmit Operation in Master Mode

Timer Clear-Set:

The Timer value can only be cleared when a Compare Match occurs if it is enabled by the Bit6 in the TTCR0. TCMR1 and TCMR2 do not have this function.

Cancellation of the messages in the transmission queue:

The messages in the transmission queue can only be cleared by the TCMR2 through setting TXCR when a Compare Match occurs while this module is not in the halt status. TCMR1 and TCMR0 do not have this function.

- TCMR0 (Address = H'098)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCMR0[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 15 to 0 — Timer Compare Match Register (TCMR0): Indicates the value of TCNTR when compare match occurs.

- TCMR1 (Address = H'09C)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCMR1[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 15 to 0 — Timer Compare Match Register (TCMR1): Indicates the value of CYCTR when compare match occurs.

- TCMR2 (Address = H'0A0)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCMR2[15:0]															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 15 to 0 — Timer Compare Match Register (TCMR2): Indicates the value of CYCTR when compare match occurs.

(2) Communications Mode

The IEBus has three communications modes with different transfer speeds. Table 21.2 shows the transfer speed in each communications mode and the maximum number of transfer bytes in one communications frame.

Table 21.2 Transfer Speed and Maximum Number of Transfer Bytes in Each Communications Mode

Communications Mode	Maximum Number of Transfer Bytes (bytes/frame)	Effective Transfer Speed*1 (kbps)	
		IEBϕ*2 = 12, 18, 24*3, 30, 36 MHz	IEBϕ*2 = 12.58, 18.87*3, 25.16, 31.45 MHz
0	16	About 3.9	About 4.1
1	32	About 17	About 18
2	128	About 26	About 27

Notes: Each unit connected to the IEBus should select a communications mode prior to performing communications. Note that correct communications is not guaranteed if the master and slave units do not adopt the same communications mode.

In the case of communications between a unit with IEBϕ = 6 MHz and a unit with IEBϕ = 6.29 MHz, correct communications are not possible even if the same communications mode is adopted. Communications must be done with the same oscillation frequency.

1. Effective transfer speed when the maximum number of transfer bytes is transmitted.
2. Peripheral clock (Pϕ), or clocks for AUDIO_X1 and AUDIO_X2
3. Oscillation frequency when this LSI is used

(3) Communications Address

In the IEBus, a specific 12-bit communications address is allocated to each individual unit. A communications address is configured as follows.

- Upper four bits: group number (number identifying a group to which the unit belongs)
- Lower eight bits: unit number (number identifying individual units in a group)

21.3.18 IEBus Receive Status Register (IERSR)

IERSR detects receive busy, receive start, receive normal completion, or receive completion with an error. Each status flag in IERSR corresponds to a bit in the IEIER that enables/disables each interrupt. This register is cleared by writing 1 to each bit.

Bit:	7	6	5	4	3	2	1	0
	RXBSY	RXS	RXF	RXEDE	RXEOVE	RXE RTME	RXEDLE	RXEPE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R/(W)*

Bit	Bit Name	Initial Value	R/W	Description
7	RXBSY	0	R/(W)*	Receive Busy Indicates that the receive data is stored in the receive data buffer (IERB001 to IERB128). Clear this bit after reading out all data. The next receive data cannot be received while this bit is set. [Setting condition] • When all receive data has been written to the receive data buffer. [Clearing condition] • When 1 is written
6	RXS	0	R/(W)*	Receive Start Detection Indicates that this module starts reception. [Setting condition] • When the data from the master unit to message length field has been received correctly in slave reception [Clearing condition] • When 1 is written

21.5.2 Master Transmission

Figure 21.9 shows the flowchart for master transmission.

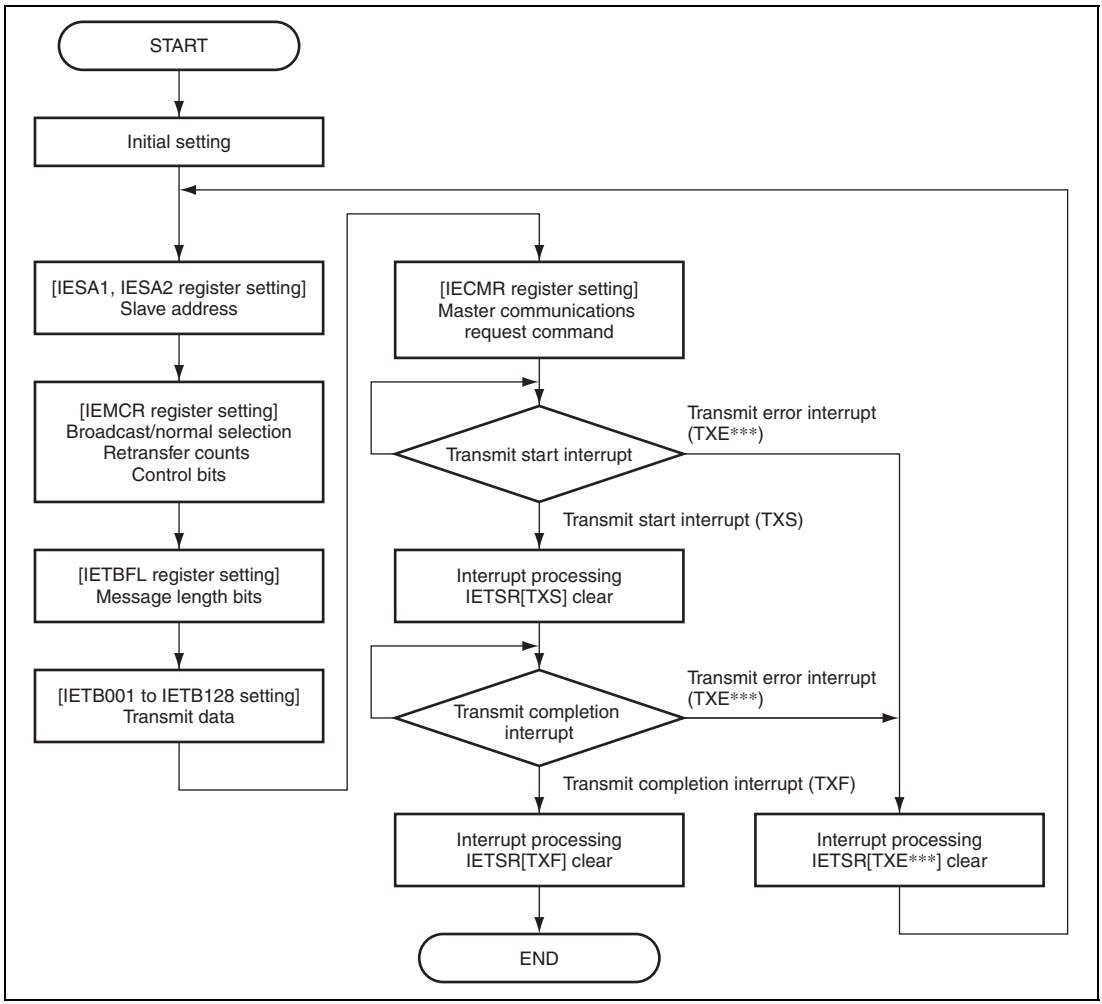


Figure 21.9 Flowchart for Master Transmission

Bit	Bit Name	Initial Value	R/W	Description
23 to 20	CHNO[3:0]	All 0	R	Channel Number 0000: Don't care 0001: A (left channel) 0010: B (left channel) 0011: C
19 to 16	SRCNO[3:0]	All 0	R	Source Number 0000: Don't care 0001: 1 0010: 2 0011: 3
15 to 8	CATCD[7:0]	All 0	R	Category Code (Example) 00000000: 2-channel general format 00000001: 2-channel compact disc (IEC 908) 00000010: 2-channel PCM encoder/decoder 00000011: 2-channel digital audio tape recorder
7, 6	—	All 0	R	Reserved
5 to 1	CTL[4:0]	All 0	R	Control The control bits are copied from the source (see IEC60958 standard).
0	—	0	R	Reserved

27.7.32 Panel Clock Select Register (PANEL_CLKSEL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	ICKSEL	ICKEN	-	-	-	-	-	-	DCDR[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	ICKSEL	0	R/W	Selects the source of the panel clock. 0: External clock is selected (LCD_EXTCLK). 1: Bus clock is selected (Bϕ).
12	ICKEN	0	R/W	Enables or disables the operation of the blocks using the panel clock in this module and output of the panel clock. 0: Operation of the blocks using the panel clock is disabled. 1: Operation of the blocks using the panel clock is enabled. Note: Be sure to clear this bit to 0 before modifying the ICKSEL or DCDR bit.
11 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DCDR[5:0]	000001	R/W	Specifies the division ratio of the input clock frequency. For details, see table 27.14. Note: The settings not shown in table 27.14 are prohibited.

This module can select the bus clock or external clock as the source of the panel clock. It also has a frequency divider providing a division ratio from 1/1 to 1/32.

(2) Port B Port Register 0 (PBPR0)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PB15PR	PB14PR	PB13PR	PB12PR	PB11PR	PB10PR	PB9PR	PB8PR	PB7PR	PB6PR	PB5PR	PB4PR	PB3PR	PB2PR	PB1PR	-
Initial value:	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	PB15PR	Pin state	R	The pin state is returned. These bits cannot be modified.
14	PB14PR	Pin state	R	
13	PB13PR	Pin state	R	
12	PB12PR	Pin state	R	
11	PB11PR	Pin state	R	
10	PB10PR	Pin state	R	
9	PB9PR	Pin state	R	
8	PB8PR	Pin state	R	
7	PB7PR	Pin state	R	
6	PB6PR	Pin state	R	
5	PB5PR	Pin state	R	
4	PB4PR	Pin state	R	
3	PB3PR	Pin state	R	
2	PB2PR	Pin state	R	
1	PB1PR	Pin state	R	
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	PF12DR	0	R/W	See table 32.18
11	PF11DR	0	R/W	
10	PF10DR	0	R/W	
9	PF9DR	0	R/W	
8	PF8DR	0	R/W	
7	PF7DR	0	R/W	
6	PF6DR	0	R/W	
5	PF5DR	0	R/W	
4	PF4DR	0	R/W	
3	PF3DR	0	R/W	
2	PF2DR	0	R/W	
1	PF1DR	0	R/W	
0	PF0DR	0	R/W	

Table 32.18 Port F Data Register 0 (PFDR0) Read/Write Operation

- Bits 12 to 0 of PFDR0

PFIOR0	Pin Operation	Read Operation	Write Operation
0	General input	Pin state	Can write to PFDR0, but it has no effect on the pin state
	Other than general input	Pin state	Can write to PFDR0, but it has no effect on the pin state
1	General output	PFDR0 value	Value written is output from pin
	Other than general output	PFDR0 value	Can write to PFDR0, but it has no effect on the pin state

38.4 Recommended Combination of Bypass Capacitor

Mount a multilayer ceramic capacitor between a pair of the power supply pins as a bypass capacitor. These capacitors must be placed as close as the power supply pins of the LSI. The capacitance of the capacitors should be used 0.1 μF to 0.33 μF (recommended values). For details of the capacitor related to the crystal resonator, see section 5, Clock Pulse Generator.

Figures 38.1 and 38.2 are examples of externally allocated capacitors in the SH7262 Group and SH7264 Group, respectively.

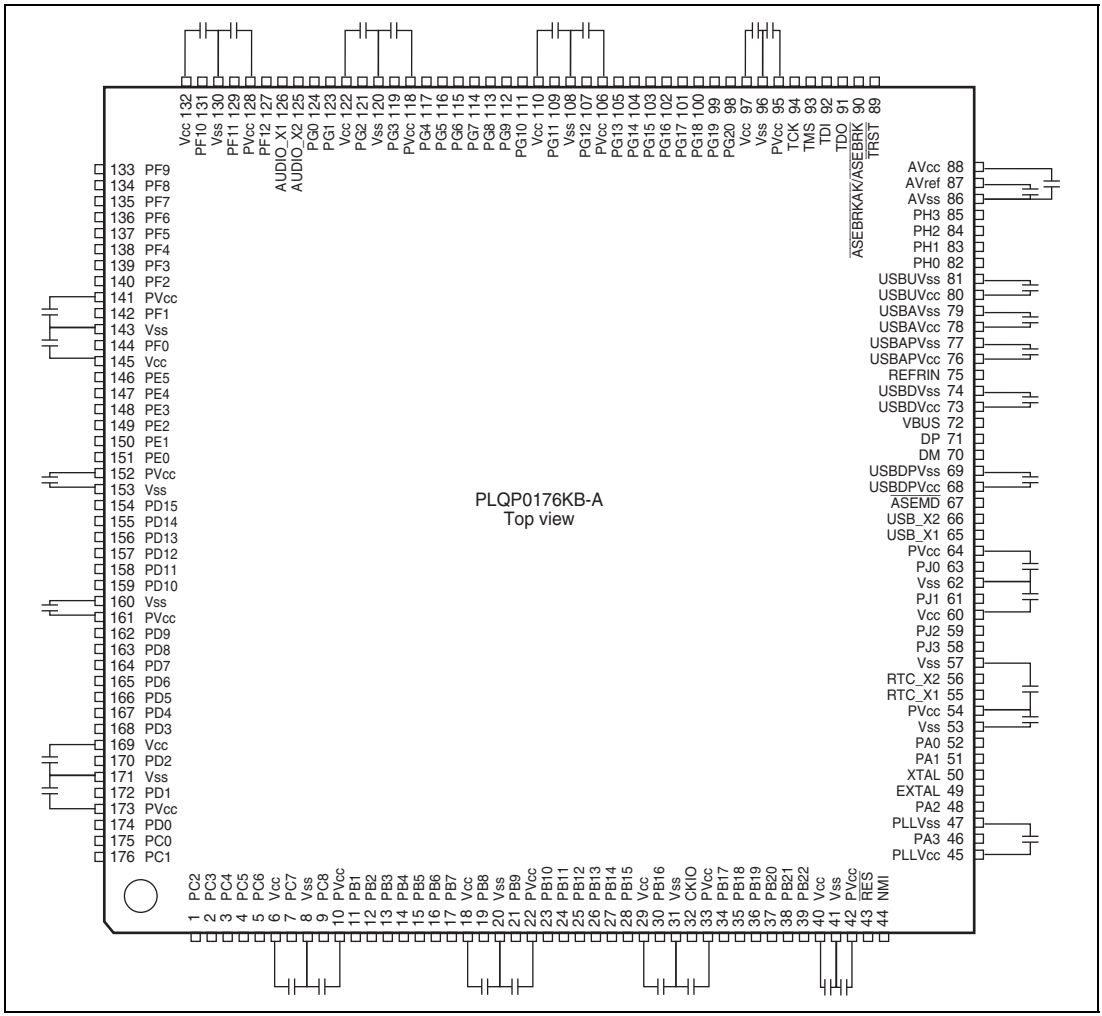


Figure 38.1 Example of Externally Allocated Capacitors in the SH7262 Group

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SH7262 Group, SH7264 Group
User's Manual: Hardware

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