Renesas Electronics America Inc - R5S72624P144FP#UZ Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	89
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72624p144fp-uz

3.3.2 Floating-Point Status/Control Register (FPSCR)

FPSCR is a 32-bit register that controls floating-point instructions, sets FPU exceptions, and selects the rounding mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	QIS	-	SZ	PR	DN	Cause	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Cause				Enable					Flag					RM1	RM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	QIS	0	R/W	Nonnunerical Processing Mode 0: Processes qNaN or ±∞ as such 1: Treats qNaN or ±∞ as the same as sNaN (valid only when FPSCR.Enable.V = 1)
21	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
20	SZ	0	R/W	Transfer Size Mode 0: Data size of FMOV instruction is 32-bits 1: Data size of FMOV instruction is a 32-bit register pair (64 bits)
19	PR	0	R/W	Precision Mode 0: Floating-point instructions are executed as single-precision operations 1: Floating-point instructions are executed as double-precision operations (graphics support instructions are undefined)
18	DN	1	R	Denormalization Mode (Always fixed to 1 in SH2A-FPU) 1: Denormalized number is treated as zero

Table 9.5 16-Bit External Device Access and Data Alignment in Big Endian

Operation		Data Bus		Strobe Signals	
		D15 to D8	D7 to D0	$\overline{WE1}$, DQMU	$\overline{WE0}$, DQML
Byte access at address 0		Data 7 to 0	—	Assert	—
Byte access at address 1		—	Data 7 to 0	—	Assert
Byte access at address 2		Data 7 to 0	—	Assert	—
Byte access at address 3		—	Data 7 to 0	—	Assert
Word access at address 0		Data 15 to 8	Data 7 to 0	Assert	Assert
Word access at address 2		Data 15 to 8	Data 7 to 0	Assert	Assert
Longword access at address 0	1st access at address 0	Data 31 to 24	Data 23 to 16	Assert	Assert
	2nd access at address 2	Data 15 to 8	Data 7 to 0	Assert	Assert

Table 9.6 8-Bit External Device Access and Data Alignment in Big Endian

Operation		Data Bus		Strobe Signals	
		D15 to D8	D7 to D0	$\overline{WE1}$, DQMU	$\overline{WE0}$, DQML
Byte access at address 0		—	Data 7 to 0	—	Assert
Byte access at address 1		—	Data 7 to 0	—	Assert
Byte access at address 2		—	Data 7 to 0	—	Assert
Byte access at address 3		—	Data 7 to 0	—	Assert
Word access at address 0	1st access at address 0	—	Data 15 to 8	—	Assert
	2nd access at address 1	—	Data 7 to 0	—	Assert
Word access at address 2	1st access at address 2	—	Data 15 to 8	—	Assert
	2nd access at address 3	—	Data 7 to 0	—	Assert
Longword access at address 0	1st access at address 0	—	Data 31 to 24	—	Assert
	2nd access at address 1	—	Data 23 to 16	—	Assert
	3rd access at address 2	—	Data 15 to 8	—	Assert
	4th access at address 3	—	Data 7 to 0	—	Assert

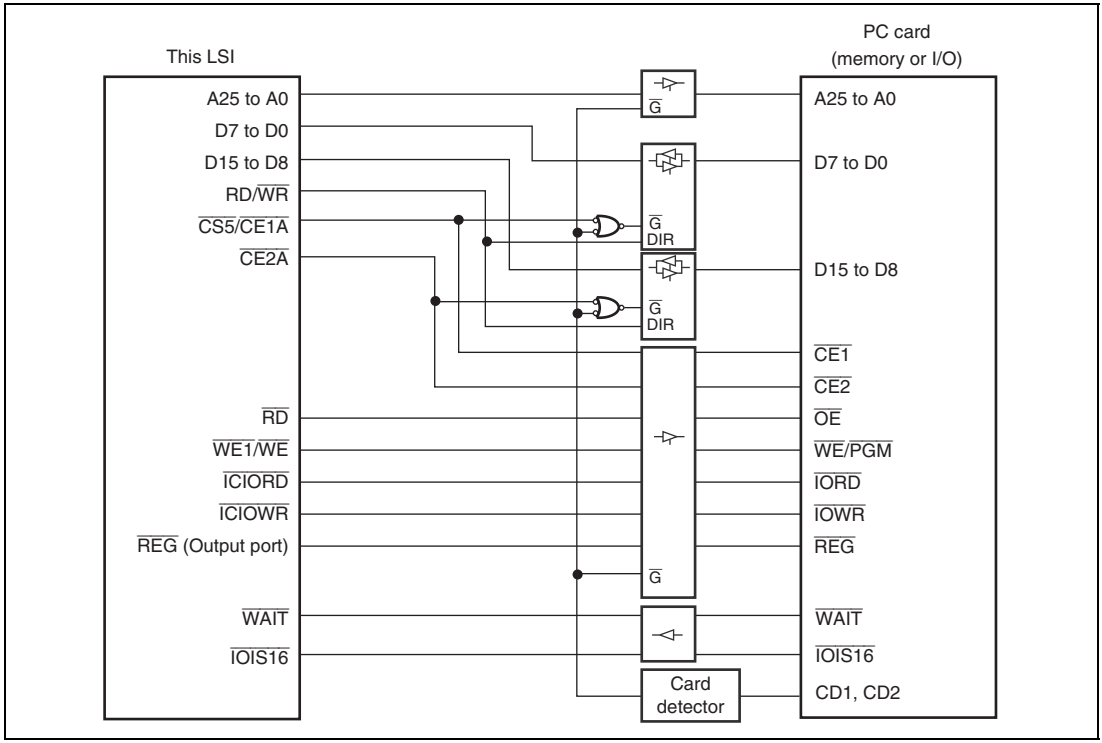

Figure 9.38 Example of PCMCIA Interface Connection

Table 11.12 TIORL_0 (Channel 0)

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_0 Function**	**TIOC0D Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges
	1	X	X		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down

[Legend]

X: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFB bit in TMDR_0 is set to 1 and TGRD_0 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 11.24 TIORL_3 (Channel 3)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_3 Function**	**TIOC3C Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_3 is set to 1 and TGRC_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

11.3.27 Timer Buffer Transfer Set Register (TBTER)

TBTER is an 8-bit readable/writable register that enables or disables transfer from the buffer registers* used in complementary PWM mode to the temporary registers and specifies whether to link the transfer with interrupt skipping operation. This module has one TBTER.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	BTE[1:0]	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	BTE[1:0]	00	R/W	These bits enable or disable transfer from the buffer registers* used in complementary PWM mode to the temporary registers and specify whether to link the transfer with interrupt skipping operation. For details, see table 11.40.

Note: * Applicable buffer registers:
TGRC_3, TGRD_3, TGRC_4, TGRD_4, and TCBR

14.3.9 Second Alarm Register (RSECAR)

RSECAR is an alarm register corresponding to the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, a comparison with the RSECCNT value is performed. From among RSECAR/RMINAR/RHRAR/RWKAR/RDAYAR/RMONAR/RCR3, the counter and alarm register comparison is performed only on those with ENB bits set to 1, and if each of those coincides, an alarm flag of RCR1 is set to 1.

The assignable range is from 00 through 59 + ENB bits (practically in BCD), otherwise operation errors occur.

Bit:	7	6	5	4	3	2	1	0
	ENB	10 seconds			1 second			
Initial value:	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ENB	Undefined	R/W	When this bit is set to 1, a comparison with the RSECCNT value is performed.
6 to 4	10 seconds	Undefined	R/W	Ten's position of seconds setting value
3 to 0	1 second	Undefined	R/W	One's position of seconds setting value

Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	Receive Enable Enables or disables the serial receiver. 0: Receiver disabled*[1] 1: Receiver enabled*[2] Notes: 1. Clearing RE to 0 does not affect the receive flags (DR, ER, BRK, RDF, FER, PER, and ORER). These flags retain their previous values. 2. Serial reception starts when a start bit is detected in asynchronous mode, or synchronous clock is detected in clock synchronous mode. Select the receive format in SCSMR and SCFCR and reset the receive FIFO before setting RE to 1.
3	REIE	0	R/W	Receive Error Interrupt Enable Enables or disables the receive-error (ERI) interrupts and break (BRI) interrupts. The setting of REIE bit is valid only when RIE bit is set to 0. 0: Receive-error interrupt (ERI) and break interrupt (BRI) requests are disabled 1: Receive-error interrupt (ERI) and break interrupt (BRI) requests are enabled* Note: * ERI or BRI interrupt requests can be cleared by reading the ER, BR or ORER flag after it has been set to 1, then clearing the flag to 0, or by clearing RIE and REIE to 0. Even if RIE is set to 0, when REIE is set to 1, ERI or BRI interrupt requests are enabled.

18.4.4 Transmit Operation

Transmission can be controlled either by DMA transfer or interrupt.

DMA control is preferred to reduce the processor load. In DMA control mode, the processor will only receive interrupts if there is an underflow or overflow of data or if the DMA transfer has been completed.

The alternative method is using the interrupts that this module generates to supply data as required.

When disabling this module, the clock* must be kept supplied to this module until the IIRQ bit indicates that the module is in the idle state.

Figure 18.20 shows the transmit operation in DMA control mode, and figure 18.21 shows the transmit operation in interrupt control mode.

Note: * Input clock from the SSISCK pin when SCKD = 0.
Oversampling clock when SCKD = 1.

(2) Regarding Transmit and Receive Classification

The transmit request and receive request are signals indicating the state; after being set, if the state of the transmit/receive FIFO change, they are automatically cleared by this module.

When the DMA transfer is used, the signal is cleared to 0 by the direct memory access controller. If the setting condition is still satisfied after the access using the direct memory access controller, it is set to 1 again.

(3) Processing when Errors Occur

On occurrence of each of the errors indicated as a status in SISTR, this module performs the following operations.

- Transmit FIFO underflow (TFUDF)
  The immediately preceding transmit data is again transmitted.
- Transmit FIFO overflow (TFOVF)
  The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)
  Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)
  The read value is undefined.
- FS error (FSERR)
  The internal counter is reset according to the sync signal in which an error occurs.

23.3 Register Descriptions

This module has the following registers.

Table 23.1 Register Configuration

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Enable control register	CROMEN	R/W	H'00	H'FFFF9000	8
Sync code-based synchronization control register	CROMSY0	R/W	H'89	H'FFFF9001	8
Decoding mode control register	CROMCTL0	R/W	H'82	H'FFFF9002	8
EDC/ECC check control register	CROMCTL1	R/W	H'D1	H'FFFF9003	8
Automatic decoding stop control register	CROMCTL3	R/W	H'00	H'FFFF9005	8
Decoding option setting control register	CROMCTL4	R/W	H'00	H'FFFF9006	8
HEAD20 to HEAD22 representation control register	CROMCTL5	R/W	H'00	H'FFFF9007	8
Sync code status register	CROMST0	R	H'00	H'FFFF9008	8
Post-ECC header error status register	CROMST1	R	H'00	H'FFFF9009	8
Post-ECC subheader error status register	CROMST3	R	H'00	H'FFFF900B	8
Header/subheader validity check status register	CROMST4	R	H'00	H'FFFF900C	8
Mode determination and link sector detection status register	CROMST5	R	H'00	H'FFFF900D	8
ECC/EDC error status register	CROMST6	R	H'00	H'FFFF900E	8
Buffer status register	CBUFST0	R	H'00	H'FFFF9014	8
Decoding stoppage source status register	CBUFST1	R	H'00	H'FFFF9015	8
Buffer overflow status register	CBUFST2	R	H'00	H'FFFF9016	8
Pre-ECC correction header: minutes data register	HEAD00	R	H'00	H'FFFF9018	8
Pre-ECC correction header: seconds data register	HEAD01	R	H'00	H'FFFF9019	8
Pre-ECC correction header: frames (1/75 second) data register	HEAD02	R	H'00	H'FFFF901A	8
Pre-ECC correction header: mode data register	HEAD03	R	H'00	H'FFFF901B	8

23.3.22 Pre-ECC Correction Subheader: Channel Number (Byte 17) Data Register (SHEAD01)

The pre-ECC correction subheader: channel number (byte 17) data register (SHEAD01) indicates the channel number value in the subheader before ECC correction (byte 17).

Bit:	7	6	5	4	3	2	1	0
	SHEAD01[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SHEAD01 [7:0]	All 0	R	Indicate channel number value in the subheader before ECC correction (byte 17). For sectors not in Mode 2, this register contains the byte of data at the corresponding position.

23.3.23 Pre-ECC Correction Subheader: Sub-Mode (Byte 18) Data Register (SHEAD02)

The pre-ECC correction subheader: sub-mode (byte 18) data register (SHEAD02) indicates the sub-mode value in the subheader before ECC correction (byte 18).

Bit:	7	6	5	4	3	2	1	0
	SHEAD02[7:0]							
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	SHEAD02 [7:0]	All 0	R	Indicate sub-mode value in the subheader before ECC correction (byte 18). For sectors not in Mode 2, this register contains the byte of data at the corresponding position.

24.4.6 External Trigger Input Timing

A/D conversion can also be externally triggered. When the TRGS[3:0] bits in ADCSR are set to B'1001, an external trigger is input to the $\overline{\text{ADTRG}}$ pin. The ADST bit in ADCSR is set to 1 at the falling edge of the $\overline{\text{ADTRG}}$ pin, thus starting A/D conversion. Other operations, regardless of the operating mode, are the same as when the ADST bit has been set to 1 by software. Figure 24.6 shows the timing.

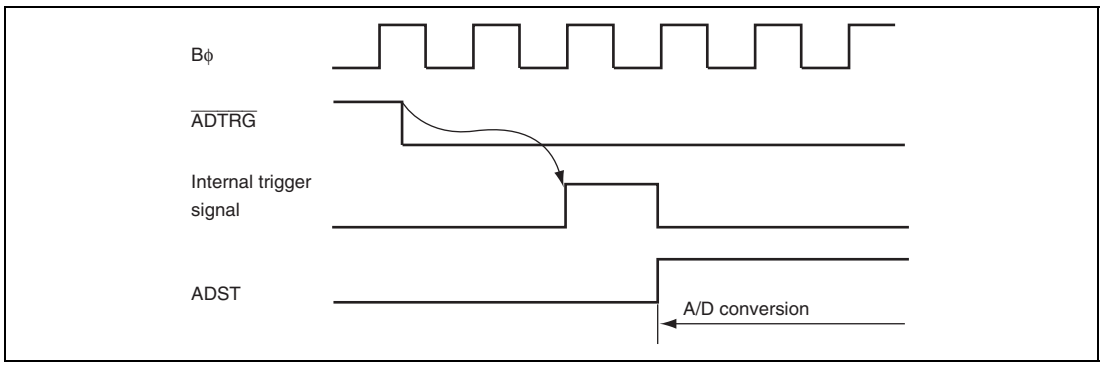

Figure 24.6 External Trigger Input Timing

Bit	Bit Name	Initial Value	R/W	Description
8	STERB	0	R/(W)*	Status Error Indicates the result of status read. This bit is set to 1 if the specific bit in the bits STAT[7:0] in FLBSYCNT is set to 1 in status read. This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no status error occurs (the specific bit in the bits STAT[7:0] in FLBSYCNT is 0.) 1: Indicates that a status error occurs For details on the specific bit in STAT7 to STAT0 bits, see section 25.4.7, Status Read.
7	BTOERB	0	R/(W)*	R/$\overline{B}$ Timeout Error This bit is set to 1 if an R/$\overline{B}$ timeout error occurs (the bits RBTIMCNT[19:0] in FLBSYCNT are decremented to 0). This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no R/$\overline{B}$ timeout error occurs 1: Indicates that an R/$\overline{B}$ timeout error occurs
6	TRREQF1	0	R/(W)*	FLECFIFO Transfer Request Flag Indicates that a transfer request is issued from FLECFIFO. This bit is a flag. 1 cannot be written to this bit. Only 0 can be written to clear the flag. 0: Indicates that no transfer request is issued from FLECFIFO 1: Indicates that a transfer request is issued from FLECFIFO

Bit	Bit Name	Initial Value	R/W	Description
5	ISEL	0	R/W	CFIFO Port Access Direction When DCP is Selected 0: Reading from the buffer memory is selected 1: Writing to the buffer memory is selected After writing to this bit with the DCP being a selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process. Even if an attempt is made to modify the setting of this bit during access to the FIFO buffer, the current access setting is retained until the access is completed. Then, the modification becomes effective thus enabling continuous access. Set this bit and the CURPIPE bits simultaneously.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. Only 0 can be read and 1 can be written.
2. Modify each bit in this register while CSSTS is 0 and PID is NAK. Before modifying each bit after modifying the PID bits for the corresponding pipe from BUF to NAK, check that CSSTS and PBUSY are 0. However, if the PID bits have been modified to NAK by this module, checking PBUSY is not necessary.

26.3.38 PIPEn Transaction Counter Registers (PIPEnTRN) (n = 1 to 5)

PIPEnTRN is a transaction counter corresponding to PIPE1 to PIPE5.

This register is initialized by a power-on reset, but retains the set value by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRNCNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT[15:0]	All 0	R/W	Transaction Counter When written to: Specifies the number of transactions to be transferred through DMA. When read from: Indicates the specified number of transactions if TRENB is 0. Indicates the number of currently counted transaction if TRENB is 1.

Table 31.2 Address Spaces of On-Chip Large-Capacity RAM (1-Mbyte Version)

Page	Cache-enabled Address	Cache-disabled Address
Page 0 (160 Kbytes)	H'1C000000 to H'1C027FFF	H'3C000000 to H'3C027FFF
Page 1 (80 Kbytes)	H'1C028000 to H'1C03BFFF	H'3C028000 to H'3C03BFFF
Page 2 (80 Kbytes)	H'1C03C000 to H'1C04FFFF	H'3C03C000 to H'3C04FFFF
Page 3 (160 Kbytes)	H'1C050000 to H'1C077FFF	H'3C050000 to H'3C077FFF
Page 4 (240 Kbytes)	H'1C078000 to H'1C0B3FFF	H'3C078000 to H'3C0B3FFF
Page 5 (304 Kbytes)	H'1C0B4000 to H'1C0FFFFF	H'3C0B4000 to H'3C0FFFFF

Table 31.3 Address Spaces of On-Chip Data Retention RAM (1-Mbyte Version)

Page	Cache-enabled Address	Cache-disabled Address
Page 0 (16 Kbytes)	H'1C0F8000 to H'1C0FBFFF	H'3C0F8000 to H'3C0FBFFF
Page 1 (16 Kbytes)	H'1C0FC000 to H'1C0FFFFF	H'3C0FC000 to H'3C0FFFFF

Table 31.4 Address Spaces of On-Chip Large-Capacity RAM (640-Kbyte Version)

Page	Cache-enabled Address	Cache-disabled Address
Page 0 (160 Kbytes)	H'1C000000 to H'1C027FFF	H'3C000000 to H'3C027FFF
Page 1 (80 Kbytes)	H'1C028000 to H'1C03BFFF	H'3C028000 to H'3C03BFFF
Page 2 (80 Kbytes)	H'1C03C000 to H'1C04FFFF	H'3C03C000 to H'3C04FFFF
Page 3 (160 Kbytes)	H'1C050000 to H'1C077FFF	H'3C050000 to H'3C077FFF
Page 4 (160 Kbytes)	H'1C078000 to H'1C09FFFF	H'3C078000 to H'3C09FFFF

Table 31.5 Address Spaces of On-Chip Data Retention RAM (640-Kbyte Version)

Page	Cache-enabled Address	Cache-disabled Address
Page 0 (16 Kbytes)	H'1C000000 to H'1C003FFF	H'3C000000 to H'3C003FFF
Page 1 (16 Kbytes)	H'1C004000 to H'1C007FFF	H'3C004000 to H'3C007FFF
Page 2 (128 Kbytes)	H'1C008000 to H'1C027FFF	H'3C008000 to H'3C027FFF
Page 3 (160 Kbytes)	H'1C028000 to H'1C04FFFF	H'3C028000 to H'3C04FFFF

32.2.25 Port G I/O Registers 0, 1 (PGIOR0, PGIOR1)

PGIOR1 and PGIOR0 are 16-bit readable/writable registers that are used to set the pins on port G as inputs or outputs. The PG24IOR to PG0IOR bits correspond to the PG24 to PG0, respectively. PGIOR1 and PGIOR0 are enabled when the port G pins are functioning as general-purpose I/O (PG24 to PG0) or TIOC I/O of multi-function timer pulse unit 2. In other states, they are disabled. If bits in PGIOR1 and PGIOR0 are set to 1, corresponding pins on port G functions as outputs. If they are cleared to 0, the corresponding pins function as inputs.

Bits15 to 9 in PGIOR1, and bits 8 to 5 in PGIOR1 in the SH7262 Group are reserved. These bits are always read as 0. The write values should always be 0.

(1) Port G IO Register 1 (PGIOR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	PG24 IOR	PG23 IOR	PG22 IOR	PG21 IOR	PG20 IOR	PG19 IOR	PG18 IOR	PG17 IOR	PG16 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(2) Port G IO Register 0 (PGIOR0)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PG15 IOR	PG14 IOR	PG13 IOR	PG12 IOR	PG11 IOR	PG10 IOR	PG9 IOR	PG8 IOR	PG7 IOR	PG6 IOR	PG5 IOR	PG4 IOR	PG3 IOR	PG2 IOR	PG1 IOR	PG0 IOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

32.2.26 Port G Data Register 0, 1 (PGDR0, PGDR1)

PGDR1 and PGDR0 are 16-bit readable/writable registers that store port G data. The PG24DR to PG0DR bits correspond to the PG24 to PGDR0 pins, respectively.

When a pin function is general output, if a value is written to PGDR1 or PGDR0, that value is output from the pin, and if PGDR1 or PGDR0 is read, the register value is returned directly regardless of the pin state.

When a pin function is general input, if PGDR1 or PGDR0 is read, the pin state, not the register value, is returned directly. If a value is written to PGDR1 or PGDR0, although that value is written into PGDR1 or PGDR0, it does not affect the pin state. Table 32.19 summarizes PGDR1/PGDR0 read/write operation.

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
General purpose I/O ports	PBPR0	PB15PR	PB14PR	PB13PR	PB12PR	PB11PR	PB10PR	PB9PR	PB8PR
		PB7PR	PB6PR	PB5PR	PB4PR	PB3PR	PB2PR	PB1PR	—
	PCCR2	—	—	—	—	—	—	—	PC10MD0
		—	—	—	PC9MD0	—	—	PC8MD1	PC8MD0
	PCCR1	—	—	PC7MD1	PC7MD0	—	—	PC6MD1	PC6MD0
		—	—	PC5MD1	PC5MD0	—	—	—	PC4MD0
	PCCR0	—	—	—	PC3MD0	—	—	—	PC2MD0
		—	—	—	PC1MD0	—	—	—	PC0MD0
	PCIOR0	—	—	—	—	—	PC10IOR	PC9IOR	PC8IOR
		PC7IOR	PC6IOR	PC5IOR	PC4IOR	PC3IOR	PC2IOR	PC1IOR	PC0IOR
	PCDR0	—	—	—	—	—	PC10DR	PC9DR	PC8DR
		PC7DR	PC6DR	PC5DR	PC4DR	PC3DR	PC2DR	PC1DR	PC0DR
	PCPR0	—	—	—	—	—	PC10PR	PC9PR	PC8PR
		PC7PR	PC6PR	PC5PR	PC4PR	PC3PR	PC2PR	PC1PR	PC0PR
	PDCR3	—	—	PD15MD1	PD15MD0	—	—	PD14MD1	PD14MD0
		—	—	PD13MD1	PD13MD0	—	—	PD12MD1	PD12MD0
	PDCR2	—	—	PD11MD1	PD11MD0	—	—	PD10MD1	PD10MD0
		—	—	PD9MD1	PD9MD0	—	—	PD8MD1	PD8MD0
	PDCR1	—	—	PD7MD1	PD7MD0	—	—	PD6MD1	PD6MD0
		—	—	PD5MD1	PD5MD0	—	—	PD4MD1	PD4MD0
	PDCR0	—	—	PD3MD1	PD3MD0	—	—	PD2MD1	PD2MD0
		—	—	PD1MD1	PD1MD0	—	—	PD0MD1	PD0MD0
	PDIOR0	PD15IOR	PD14IOR	PD13IOR	PD12IOR	PD11IOR	PD10IOR	PD9IOR	PD8IOR
		PD7IOR	PD6IOR	PD5IOR	PD4IOR	PD3IOR	PD2IOR	PD1IOR	PD0IOR
	PDDR0	PD15DR	PD14DR	PD13DR	PD12DR	PD11DR	PD10DR	PD9DR	PD8DR
		PD7DR	PD6DR	PD5DR	PD4DR	PD3DR	PD2DR	PD1DR	PD0DR
	PDPR0	PD15PR	PD14PR	PD13PR	PD12PR	PD11PR	PD10PR	PD9PR	PD8PR
		PD7PR	PD6PR	PD5PR	PD4PR	PD3PR	PD2PR	PD1PR	PD0PR
	PECR1	—	—	—	—	—	—	—	—
		—	—	PE5MD1	PE5MD0	—	—	PE4MD1	PE4MD0