Renesas Electronics America Inc - R5S72625W144FP#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	89
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72625w144fp-u0

(6) Delayed Branch Instructions

With the exception of some instructions, unconditional branch instructions, etc., are executed as delayed branch instructions. With a delayed branch instruction, the branch is taken after execution of the instruction immediately following the delayed branch instruction. This reduces disturbance of the pipeline control when a branch is taken.

In a delayed branch, the actual branch operation occurs after execution of the slot instruction. However, instruction execution such as register updating excluding the actual branch operation, is performed in the order of delayed branch instruction → delay slot instruction. For example, even though the contents of the register holding the branch destination address are changed in the delay slot, the branch destination address remains as the register contents prior to the change.

Table 2.3 Delayed Branch Instructions

SH-2A CPU		Description	Example of Other CPU	
BRA	TRGET	Executes the ADD before branching to TRGET.	ADD.W	R1,R0
ADD	R1,R0		BRA	TRGET

(7) Unconditional Branch Instructions with No Delay Slot

The SH-2A additionally features unconditional branch instructions in which a delay slot instruction is not executed. This eliminates unnecessary NOP instructions, and so reduces the code size.

(8) Multiply/Multiply-and-Accumulate Operations

16-bit × 16-bit → 32-bit multiply operations are executed in one to two cycles. 16-bit × 16-bit + 64-bit → 64-bit multiply-and-accumulate operations are executed in two to three cycles. 32-bit × 32-bit → 64-bit multiply and 32-bit × 32-bit + 64-bit → 64-bit multiply-and-accumulate operations are executed in two to four cycles.

(9) T Bit

The T bit in the status register (SR) changes according to the result of the comparison. Whether a conditional branch is taken or not taken depends upon the T bit condition (true/false). The number of instructions that change the T bit is kept to a minimum to improve the processing speed.

No.	Condition	Description	Range	Note
[7]	Write data wait cycles	During write access, a write cycle is executed on the external bus only after the write data becomes ready. This write data wait period generates idle cycles before the write cycle. Note that when the previous cycle is a write cycle and the internal bus idle cycles are shorter than the previous write cycle, write data can be prepared in parallel with the previous write cycle and therefore, no idle cycle is generated (write buffer effect).	0 or 1	For write → write or write → read access cycles, successive access cycles without idle cycles are frequently available due to the write buffer effect described in the left column. If successive access cycles without idle cycles are not allowed, specify the minimum number of idle cycles between access cycles through CSnBCR.
[8]	Idle cycles between different memory types	To ensure the minimum pulse width on the signal-multiplexed pins, idle cycles may be inserted before access after memory types are switched. For some memory types, idle cycles are inserted even when memory types are not switched.	0 to 2.5	The number of idle cycles depends on the target memory types. See table 9.19.

Table 11.24 TIORL_3 (Channel 3)

				Description	
Bit 3 IOC3	**Bit 2 IOC2**	**Bit 1 IOC1**	**Bit 0 IOC0**	**TGRC_3 Function**	**TIOC3C Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFA bit in TMDR_3 is set to 1 and TGRC_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

14.3.9 Second Alarm Register (RSECAR)

RSECAR is an alarm register corresponding to the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, a comparison with the RSECCNT value is performed. From among RSECAR/RMINAR/RHRAR/RWKAR/RDAYAR/RMONAR/RCR3, the counter and alarm register comparison is performed only on those with ENB bits set to 1, and if each of those coincides, an alarm flag of RCR1 is set to 1.

The assignable range is from 00 through 59 + ENB bits (practically in BCD), otherwise operation errors occur.

Bit:	7	6	5	4	3	2	1	0
	ENB	10 seconds			1 second			
Initial value:	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	ENB	Undefined	R/W	When this bit is set to 1, a comparison with the RSECCNT value is performed.
6 to 4	10 seconds	Undefined	R/W	Ten's position of seconds setting value
3 to 0	1 second	Undefined	R/W	One's position of seconds setting value

In serial reception, this module operates as described below.

1. The transmission line is monitored, and if a 0 start bit is detected, internal synchronization is performed and reception is started.
2. The received data is stored in SCRSR in LSB-to-MSB order.
3. The parity bit and stop bit are received.

   After receiving these bits, this module carries out the following checks.

   A. Stop bit check: Checks whether the stop bit is 1. If there are two stop bits, only the first is checked.

   B. Checks whether receive data can be transferred from the receive shift register (SCRSR) to SCFRDR.

   C. Overrun check: Checks that the ORER flag is 0, indicating that the overrun error has not occurred.

   D. Break check: Checks that the BRK flag is 0, indicating that the break state is not set.

   If all the above checks are passed, the receive data is stored in SCFRDR.

   Note: When a parity error or a framing error occurs, reception is not suspended.

4. If the RIE bit in SCSCR is set to 1 when the RDF or DR flag changes to 1, a receive-FIFO-data-full interrupt (RXI) request is generated. If the RIE bit or the REIE bit in SCSCR is set to 1 when the ER flag changes to 1, a receive-error interrupt (ERI) request is generated. If the RIE bit or the REIE bit in SCSCR is set to 1 when the BRK or ORER flag changes to 1, a break reception interrupt (BRI) request is generated.

Bit	Bit Name	Initial Value	R/W	Description
2	AL/OVE	0	R/W	Arbitration Lost Flag/Overrun Error Flag Indicates that arbitration was lost in master mode with the I²C bus format and that the final bit has been received while RDRF = 1 with the clocked synchronous format. When two or more master devices attempt to seize the bus at nearly the same time, if the I²C bus interface 3 detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been occupied by another master. [Clearing condition] • When 0 is written in AL/OVE after reading AL/OVE = 1 [Setting conditions] • If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode • When the SDA pin outputs high in master mode while a start condition is detected • When the final bit is received with the clocked synchronous format while RDRF = 1
1	AAS	0	R/W	Slave Address Recognition Flag In slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA[6:0] in SAR. [Clearing condition] • When 0 is written in AAS after reading AAS = 1 [Setting conditions] • When the slave address is detected in slave receive mode • When the general call address is detected in slave receive mode.
0	ADZ	0	R/W	General Call Address Recognition Flag This bit is valid in slave receive mode with the I²C bus format. [Clearing condition] • When 0 is written in ADZ after reading ADZ = 1 [Setting condition] • When the general call address is detected in slave receive mode

Bit	Bit Name	Initial Value	R/W	Description
25	IIRQ	1	R	Idle Mode Interrupt Status Flag This interrupt status flag indicates whether this module is in idle state. This bit is set regardless of the value of the IIEN bit to allow polling. The interrupt can be masked by clearing IIEN, but cannot be cleared by writing to this bit. If IIRQ = 1 and IIEN = 1, an interrupt occurs. 0: This module is not in idle state. 1: This module is in idle state.
24 to 7	—	Undefined	R	Reserved The read value is undefined. The write value should always be 0.
6, 5	TCHNO [1:0]	00	R	Transmit Channel Number These bits show the current channel number. These bits indicate which channel is required to be written to SSITDR. This value will change as the data is copied to the shift register, regardless of whether the data is written to SSITDR.
4	TSWNO	1	R	Transmit Serial Word Number This status bit indicates the current word number. This bit indicates which system word is required to be written to SSITDR. This value will change as the data is copied to the shift register, regardless of whether the data is written to SSITDR.
3, 2	RCHNO [1:0]	00	R	Receive Channel Number These bits show the current channel number. These bits indicate which channel the data in SSIRDR currently represents. This value will change as the data in SSIRDR is updated from the shift register.

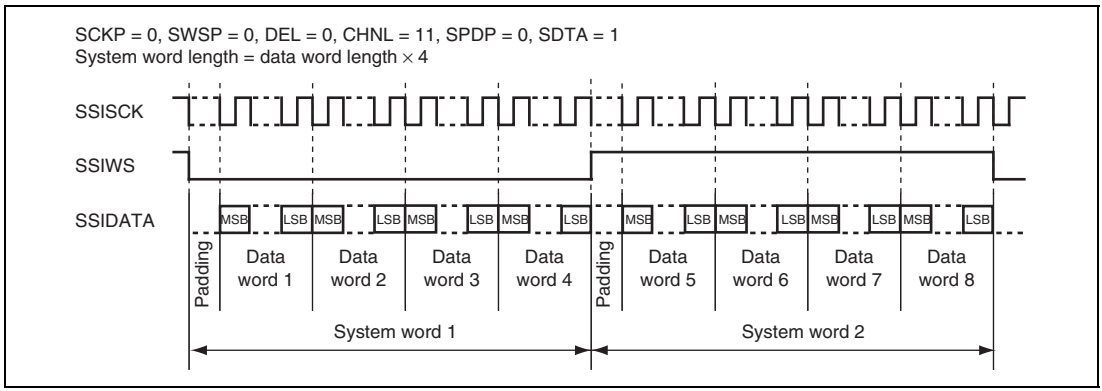

Figure 18.9 Multi-Channel Format (8 Channels; Transmitting and Receiving in the Order of Serial Data and Padding Bits; with Padding)

(9) Bit Setting Configuration Format

Several more configuration bits in non-compressed mode are shown below. These bits are not mutually exclusive, but some combinations may not be useful for any other device.

These configuration bits are described below with reference to figure 18.10.

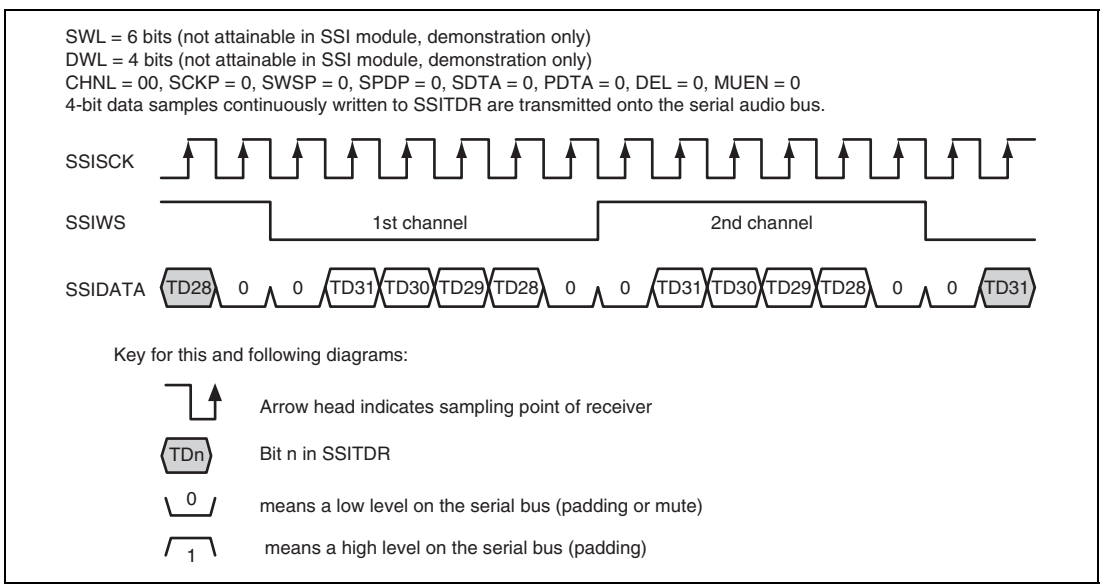

Figure 18.10 Basic Sample Format (Transmit Mode with Example System/Data Word Length)

Bit5 to 0 — Timer Prescaler (TPSC[5:0]): This control field allows the timer source clock (4*[this module system clock]) to be divided before it is used for the timer. This function is available only in event-trigger mode. In time trigger mode (CMAX is not 3'b111), one nominal Bit Timing (= one bit length of CAN bus) is automatically chosen as source clock of TCNTR.

The following relationship exists between source clock period and the timer period.

Bit[5:0]: TPSC[5:0]	Description
0 0 0 0 0 0	1 X Source Clock (initial value)
0 0 0 0 0 1	2 X Source Clock
0 0 0 0 1 0	3 X Source Clock
0 0 0 0 1 1	4 X Source Clock
0 0 0 1 0 0	5 X Source Clock
. . . . .	. . . . .
. . . . .	. . . . .
1 1 1 1 1 1	64 X Source Clock

(2) Cycle Maximum/Tx-Enable Window Register (CMAX_TEW)

This register is a 16-bit read/write register. CMAX specifies the maximum value for the cycle counter (CCR) for TT Transmissions to set the number of basic cycles in the matrix system. When the Cycle Counter reaches the maximum value (CCR = CMAX), after a full basic cycle, it is cleared to zero and an interrupt is generated on IRR.10.

TEW specifies the width of Tx-Enable window.

- CMAX_TEW (Address = H'084)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	CMAX[2:0]			-	-	-	-	TEW[3:0]			
Initial value:	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bits 15 to 11: Reserved. The written value should always be '0' and the returned value is '0'.

- Halt mode

When this module is in Halt mode, it cannot take part to the CAN bus activity. Consequently the user can modify all the requested registers without influencing existing traffic on the CAN Bus. It is important for this that the user waits for this module to be in halt mode before to modify the requested registers - note that the transition to Halt Mode is not always immediate (transition will occurs when the CAN Bus is idle or in intermission). After this module transit to Halt Mode, GSR4 is set.

Once the configuration is completed the Halt request needs to be released. This module will join CAN Bus activity after the detection of 11 recessive bits on the CAN Bus.

- Sleep mode

When this module is in sleep mode the clock for the main blocks of the IP is stopped in order to reduce power consumption. Only the following user registers are clocked and can be accessed: MCR, GSR, IRR and IMR. Interrupt related to transmission (TXACK and ABACK) and reception (RXPR and RFPR) cannot be cleared when in sleep mode (as TXACK, ABACK, RXPR and RFPR are not accessible) and must to be cleared beforehand.

Figure 20.15 shows allowed state transitions.

— Please don't set MCR5 (Sleep Mode) without entering Halt Mode.

— After MCR1 is set, please don't clear it before GSR4 is set and this module enters Halt Mode.

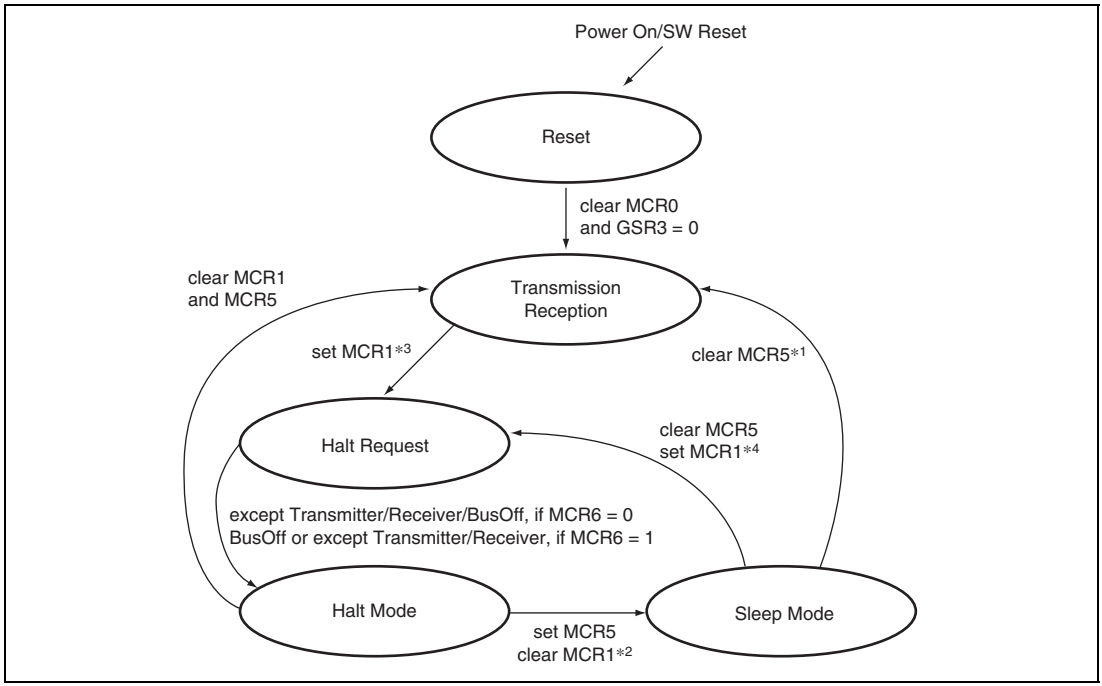

Figure 20.15 Halt Mode/Sleep Mode

Notes: 1. MCR5 can be cleared by automatically by detecting a dominant bit on the CAN Bus if MCR7 is set or by writing '0'.

2. MCR1 is cleared in SW. Clearing MCR1 and setting MCR5 have to be carried out by the same instruction.

3. MCR1 must not be cleared in SW, before GSR4 is set. MCR1 can be set automatically in HW when this module moves to Bus Off and MCR14 and MCR6 are both set.

4. When MCR5 is cleared and MCR1 is set at the same time, this module moves to Halt Request. Right after that, it moves to Halt Mode with no reception/transmission.

The following table shows conditions to access registers.

CMAX	Specifies the maximum number of basic cycles when working as potential time master
TEW	Specify the width of Tx_Enable
TCMR0	Init_Watch_Trigger (compare match with Local Time)
TCMR1	Compare match with Cycle Time to monitor users-specified events
TCMR2	Watch_Trigger (compare match with Cycle Time). This can be programmed to abort all pending transmissions
TTW	Specifies the attribute of a time window used for transmission
TTTSEL	Specifies the next Mailbox waiting for transmission

- Time Master/Time Slave

This module can be programmed to work as a potential time master of the network or as a time slave. The following table shows the settings and the operation automatically performed by this module in each mode.

Bit	Bit Name	Initial Value	R/W	Description
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11 to 0	DTLN[11:0]	H'000	R	Receive Data Length Indicates the length of the receive data. While the FIFO buffer is being read, these bits indicate the different values depending on the RCNT bit value as described below. • RCNT = 0: This module sets these bits to indicate the length of the receive data until all the received data has been read from a single FIFO buffer plane. While BFRE is 1, these bits retain the length of the receive data until BCLR is set to 1 even after all the data has been read. • RCNT = 1: This module decrements the value indicated by these bits each time data is read from the FIFO buffer. (The value is decremented by one when MBW is 00, by two when MBW is 01, and by four when MBW is 10.) This module sets these bits to 0 when all the data has been read from one FIFO buffer plane. However, in double buffer mode, if data has been received in one FIFO buffer plane before all the data has been read from the other plane, this module sets these bits to indicate the length of the receive data in the former plane when all the data has been read from the latter plane. Note: When RCNT is 1, it takes 10 bus cycles for these bits to be updated after the FIFO port has been read.

Notes: 1. Only 0 can be read and 1 can be written.
2. Only 1 can be written.

Bit	Bit Name	Initial Value	R/W	Description
8	SQCLR	0	R/W*	Toggle Bit Clear This bit should be set to 1 to clear the expected value (to set DATA0 as the expected value) of the sequence toggle bit for the next transaction of the pertinent pipe. 0: Invalid 1: Specifies DATA0. Setting this bit to 1 allows this module to set DATA0 as the expected value of the sequence toggle bit of the pertinent pipe. This module always sets this bit to 0. When the host controller function is selected, setting this bit to 1 for the pipe for bulk OUT transfer, this module starts the next transfer of the pertinent pipe with the PING token. Set the SQCLR bit to 1 while CSSTS is 0 and PID is NAK. Before modifying this bit after modifying the PID bits for the corresponding pipe from BUF to NAK, check that CSSTS and PBUSY are 0. However, if the PID bits have been modified to NAK by this module, checking PBUSY is not necessary.

Table 26.14 (1) Information Cleared by this Module by Setting ACLRM = 1

No.	Information Cleared by ACLRM Bit Manipulation
1	All the information in the FIFO buffer assigned to the pertinent pipe
2	When the host controller function is selected, the interval count value when the pertinent pipe is for isochronous transfer

Table 26.14 (2) Cases That Require Setting ACLRM to 1

No.	Cases in which Clearing the Information is Necessary
1	When it is necessary to clear all the information assigned to the pertinent pipe from the FIFO buffer
2	When the interval count value is to be reset
3	When the BFRE setting is modified
4	When the transaction count function is forcibly terminated

26.3.37 PIPEn Transaction Counter Enable Registers (PIPEnTRE) (n = 1 to 5)

PIPEnTRE is a register that enables or disables the transaction counter corresponding to PIPE1 to PIPE5, and clears the transaction counter.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W*1	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Figure 26.4 shows the timing at which an NRDY interrupt is generated when the function controller function is selected.

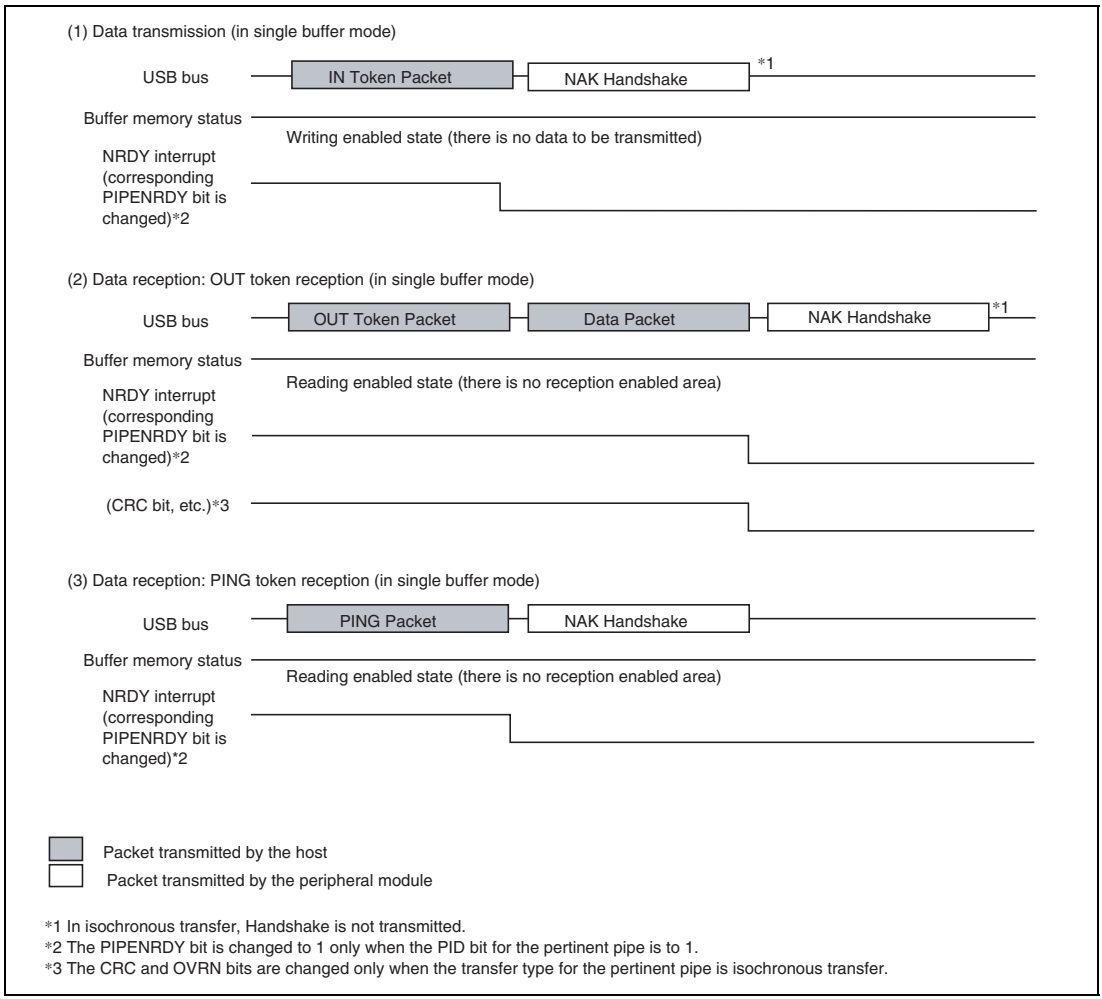

Figure 26.4 Timing at which NRDY Interrupt is Generated when Function Controller Function is Selected

Table 26.23 FIFO Port Function Settings

Register Name	Bit Name	Function	Note
C/DnFIFOSEL	RCNT	Selects DTLN read mode	
	REW	Buffer memory rewind (re-read, rewrite)	
	DCLRM	Automatically clears data received for a specified pipe after the data has been read	For DnFIFO only
	DREQE	Enables DMA transfers	For DnFIFO only
	MBW	FIFO port access bit width	
	BIGEND	Selects FIFO port endian	
	ISEL	FIFO port access direction	
	CURPIPE	Selects the current pipe	For DCP only
C/DnFIFOCTR	BVAL	Ends writing to the buffer memory	
	BCLR	Clears the buffer memory on the CPU side	
	DTLN	Checks the length of received data	

(a) FIFO Port Selection

Table 26.24 shows the pipes that can be selected with the various FIFO ports. The pipe to be accessed is selected using the CURPIPE bit in C/DnFIFOSEL. After the pipe is selected, whether the CURPIPE value for the pipe, which was written last, can be correctly read should be checked. (If the previous pipe number is read, it indicates that the pipe modification is being executed by this module.) Then, the FIFO port can be accessed after FRDY = 1 is checked .

Also, the bus width to be accessed should be selected using the MBW bit. The buffer memory access direction conforms to the DIR bit in PIPECFG. The ISEL bit determines this only for the DCP.

Table 26.24 FIFO Port Access Categorized by Pipe

Pipe	Access Method	Port that can be Used
DCP	CPU access	CFIFO port register
PIPE1 to PIPE9	CPU access	CFIFO port register
	DMA access	D0FIFO/D1FIFO port register

Register Name	Setting
VIDEO_VSTART[24:16]	For BT.656 NTSC: H'010 For BT.656 PAL: H'016 For BT.601: Specify the vertical start position of the valid video in the TOP field.
VIDEO_VSTART[8:0]	For BT.656 NTSC: H'117 For BT.656 PAL: H'14F For BT.601: Specify the vertical start position of the valid video in the BOTTOM field.
VIDEO_HSTART[8:0]	For BT.656 NTSC: H'114 For BT.656 PAL: H'120 For BT.601: Specify the horizontal start position of the valid video.
VIDEO_VSYNC_TIM1[25:16]	Refer to (1) Video Display Position and Register Settings described below.
VIDEO_VSYNC_TIM1[9:0]	Refer to (1) Video Display Position and Register Settings described below.
VIDEO_SAVE_NUM[9:0]	H'000
VIDEO_IMAGE_CNT[6:4]	Specify the vertical scaling ratio.
VIDEO_IMAGE_CNT[2:0]	Specify the horizontal scaling ratio.
VIDEO_BASEADR[31:0]	Specify the base address.
VIDEO_LINE_OFFSET[31:0]	Specify the line offset.
VIDEO_FIELD_OFFSET[31:0]	H'000
VIDEO_LINEBUFF_NUM[8:0]	Refer to (1) Video Display Position and Register Settings described below.
VIDEO_DISP_SIZE[24:16]	Specify the vertical size of the video to be displayed.
VIDEO_DISP_SIZE [9:0]	Specify the horizontal size of the video to be displayed.
VIDEO_DISP_HSTART	Specify the horizontal position of the video to be displayed.
SG_MODE [16]	H'1
VIDEO_VSYNC_TIM2	Refer to (1) Video Display Position and Register Settings described below.
VIDEO_MODE [1]	H'1
VIDEO_MODE [0]	H'1
GRCMEN2[0], [31]	H'1, H'1
GRCMEN1[0], [31]	H'1, H'1 (This setting starts display. Set this bit at the end of the procedure.)

	Setting Mode Bit (PBnMD[1:0])		
	00	01	10
Setting Register	Function 1	Function 2	Function 3
PDCR0	PD3	D3	PWM1D
	PD2	D2	PWM1C
	PD1	D1	PWM1B
	PD0	D0	PWM1A

Note: The function 2 of bus state controller and /or the function of NAND flush memory controller change automatically. (See section 9, Bus State Controller.).

Table 32.6 Multiplexed Pins (Port E)

	Setting Mode Bit (PEnMD[2:0])					
	000	001	010	011	100	101
Setting Register	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6
PECR1	PE5	SDA2	—	DV_HSYNC	—	—
	PE4	SCL2	—	DV_VSYNC	—	—
PECR0	PE3	SDA1	—	IRQ3	—	—
	PE2	SCL1	—	IRQ2	—	—
	PE1	SDA0	$\overline{\text{IOIS16}}$	IRQ1	TCLKA	$\overline{\text{ADTRG}}$
	PE0	SCL0	AUDIO_CLK	IRQ0	—	—

Item	Page	Revision (See Manual for Details)
26.3.28 DCP Configuration Register (DCPCFG)	1415, 1416	Table amended

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CNTMD	0	R/W	Continuous Transfer Mode Specifies whether the DCP operates in continuous transfer mode or not. 0: Non-continuous transfer mode 1: Continuous transfer mode Change the setting of this bit only when CSSTS = 0 and PID = NAK, and no pipe has been selected using the CURPIPE bits. When changing the setting of this bit after USB communication using the DCP, write 1 to BCLR and clear the FIFO buffer assigned to the DCP in addition to ensuring that the above three registers are in the states indicated. Before changing the setting of this bit after changing the DCP's PID bit from BUF to NAK, confirm that the values of CSSTS and PBUSY are 0. However, it is not necessary for this module to confirm the state of the PBUSY bit if the value of the PID bit has already been changed to NAK.
7	SHTNAK	0	R/W	Disable Pipe when Transfer Finishes Specifies whether the PID bit is changed to NAK when a transfer finishes while the DCP is operating in the receive direction. 0: Continue using pipe after transfer finishes. 1: Disable pipe when transfer finishes. When this bit is set to 1, this module changes the PID bit corresponding to the DCP to NAK when it determines that a transfer to the DCP has finished. This module determines that a transfer has finished when a short packet of data (or a zero-length packet) is received successfully. Change the setting of this bit only when CSSTS = 0 and PID = NAK. Before changing the setting of this bit after changing the DCP's PID bit from BUF to NAK, confirm that the values of CSSTS and PBUSY are 0. However, it is not necessary for this module to confirm the state of the PBUSY bit if the value of the PID bit has already been changed to NAK.
6, 5	—	0	R/W	Reserved These bits are always read as 0. The write value should always be 0.

Item	Page	Revision (See Manual for Details)
26.3.36 PIPEn Control Registers (PIPEnCTR) (n = 1 to 9) (1) PIPEnCTR (n = 1 to 5) Table 26.13 Operation of This Module depending on PID Setting (when Function Controller Function is Selected)	1455	Table amended

PID	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
00 (NAK)	Bulk or interrupt	Operation does not depend on the setting.	Returns NAK in response to the token from the USB host.