# Renesas Electronics America Inc - R5S72640W144FP#U0 Datasheet

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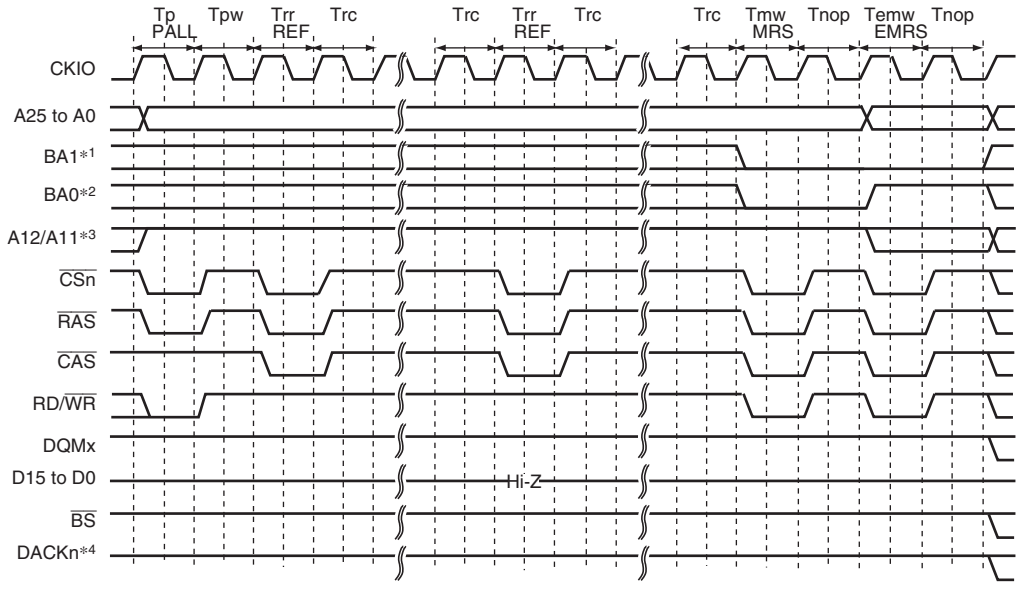
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Last Time Buy |
| Core Processor | SH2A-FPU |
| Core Size | 32-Bit Single-Core |
| Speed | 144MHz |
| Connectivity | I²C, SCI, SD, SIO, SPI, USB |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 115 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1M x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.1V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | External |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-LQFP |
| Supplier Device Package | 208-LFQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72640w144fp-u0 |




Notes: 1. Address pin to be connected to pin BA1 of SDRAM.
2. Address pin to be connected to pin BA0 of SDRAM.
3. Address pin to be connected to pin A10 of SDRAM.
4. The waveform for DACKn is when active low is specified.

**Figure 9.31 EMRS Command Issue Timing**

| CHCR | DMARS | | DMA Transfer Request Source | DMA Transfer Request Signal | Transfer Source | Transfer Destination | Bus Mode |
|---|---|---|---|---|---|---|---|
| RS[3:0] | MID | RID | | | | | |
| 1000 | 111000 | 11 | Multi-function timer pulse unit 2 Channel 0 | TGI0A (input capture or compare match) | Any | Any | Cycle steal or burst |
| | 111001 | 11 | Multi-function timer pulse unit 2 Channel 1 | TGI1A (input capture or compare match) | Any | Any | |
| | 111010 | 11 | Multi-function timer pulse unit 2 Channel 2 | TGI2A (input capture or compare match) | Any | Any | |
| | 111011 | 11 | Multi-function timer pulse unit 2 Channel 3 | TGI3A (input capture or compare match) | Any | Any | |
| | 111100 | 11 | Multi-function timer pulse unit 2 Channel 4 | TGI4A (input capture or compare match) | Any | Any | |
| | 111110 | 11 | Compare match timer Channel 0 | CMI0 (compare match) | Any | Any | |
| | 111111 | 11 | Compare match timer Channel 1 | CMI1 (compare match) | Any | Any | |

**Table 11.6 TPSC0 to TPSC2 (Channel 0)**

| Channel | Bit 2 TPSC2 | Bit 1 TPSC1 | Bit 0 TPSC0 | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Internal clock: counts on Pϕ/1 |
| | | | 1 | Internal clock: counts on Pϕ/4 |
| | | 1 | 0 | Internal clock: counts on Pϕ/16 |
| | | | 1 | Internal clock: counts on Pϕ/64 |
| | 1 | 0 | 0 | External clock: counts on TCLKA pin input |
| | | | 1 | External clock: counts on TCLKB pin input |
| | | 1 | 0 | External clock: counts on TCLKC pin input |
| | | | 1 | External clock: counts on TCLKD pin input |

**Table 11.7 TPSC0 to TPSC2 (Channel 1)**

| Channel | Bit 2 TPSC2 | Bit 1 TPSC1 | Bit 0 TPSC0 | Description |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | Internal clock: counts on Pϕ/1 |
| | | | 1 | Internal clock: counts on Pϕ/4 |
| | | 1 | 0 | Internal clock: counts on Pϕ/16 |
| | | | 1 | Internal clock: counts on Pϕ/64 |
| | 1 | 0 | 0 | External clock: counts on TCLKA pin input |
| | | | 1 | External clock: counts on TCLKB pin input |
| | | 1 | 0 | Internal clock: counts on Pϕ/256 |
| | | | 1 | Counts on TCNT_2 overflow/underflow |

Note: This setting is ignored when channel 1 is in phase counting mode.

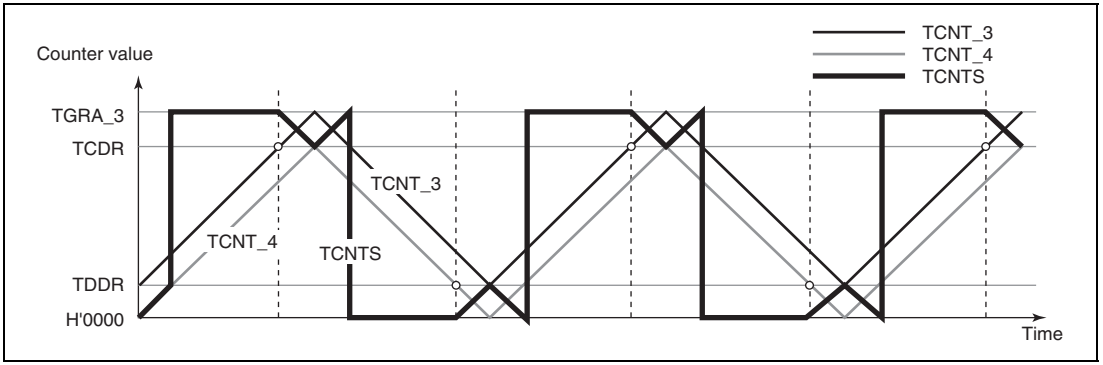



**Figure 11.39 Complementary PWM Mode Counter Operation**

### (b) Register Operation

In complementary PWM mode, nine registers are used, comprising compare registers, buffer registers, and temporary registers. Figure 11.40 shows an example of complementary PWM mode operation.

The registers which are constantly compared with the counters to perform PWM output are TGRB_3, TGRA_4, and TGRB_4. When these registers match the counter, the value set in bits OLSN and OLSP in the timer output control register (TOCR) is output.

The buffer registers for these compare registers are TGRD_3, TGRC_4, and TGRD_4.

Between a buffer register and compare register there is a temporary register. The temporary registers cannot be accessed by the CPU.

Data in a compare register is changed by writing the new data to the corresponding buffer register. The buffer registers can be read or written at any time.

The data written to a buffer register is constantly transferred to the temporary register in the Ta interval. Data is not transferred to the temporary register in the Tb interval. Data written to a buffer register in this interval is transferred to the temporary register at the end of the Tb interval.

The value transferred to a temporary register is transferred to the compare register when TCNTS for which the Tb interval ends matches TGRA_3 when counting up, or H'0000 when counting down. The timing for transfer from the temporary register to the compare register can be selected with bits MD3 to MD0 in the timer mode register (TMDR). Figure 11.40 shows an example in which the mode is selected in which the change is made in the trough.

### (15) Operation when Error Occurs during PWM Mode 2 Operation, and Operation is Restarted in PWM Mode 2

Figure 11.129 shows an explanatory diagram of the case where an error occurs in PWM mode 2 and operation is restarted in PWM mode 2 after re-setting.

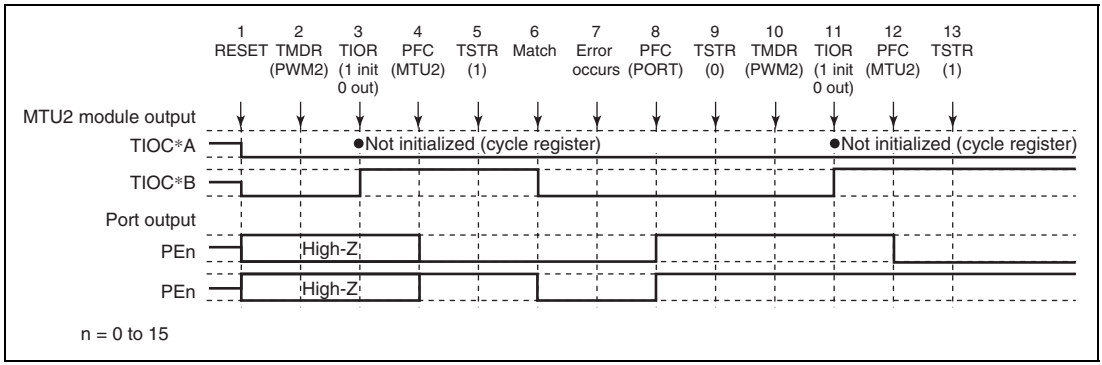



**Figure 11.129 Error Occurrence in PWM Mode 2, Recovery in PWM Mode 2**

1 to 9 are the same as in figure 11.127.

10. Not necessary when restarting in PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized.)
12. Set the multi-function timer pulse unit 2 output with the general I/O port.
13. Operation is restarted by TSTR.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | — | 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 6 | 1 Hz | Undefined | R | Indicate the state of the divider circuit between 64 Hz and 1 Hz. |
| 5 | 2 Hz | Undefined | R | |
| 4 | 4 Hz | Undefined | R | |
| 3 | 8 Hz | Undefined | R | |
| 2 | 16 Hz | Undefined | R | |
| 1 | 32 Hz | Undefined | R | |
| 0 | 64 Hz | Undefined | R | |

### 14.3.2 Second Counter (RSECCNT)

RSECCNT is used for setting/counting in the BCD-coded second section. The count operation is performed by a carry for each second of the 64-Hz counter.

The assignable range is from 00 through 59 (practically in BCD), otherwise operation errors occur. Carry out write processing after stopping the count operation through the setting of the START bit in RCR2.

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | 10 seconds | | | 1 second | | | |
| Initial value: | 0 | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined | Undefined |
| R/W: | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 | — | 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 6 to 4 | 10 seconds | Undefined | R/W | Counting Ten's Position of Seconds<br>Counts on 0 to 5 for 60-seconds counting. |
| 3 to 0 | 1 second | Undefined | R/W | Counting One's Position of Seconds<br>Counts on 0 to 9 once per second. When a carry is generated, 1 is added to the ten's position. |

- Parallel Right-Aligned with Delay

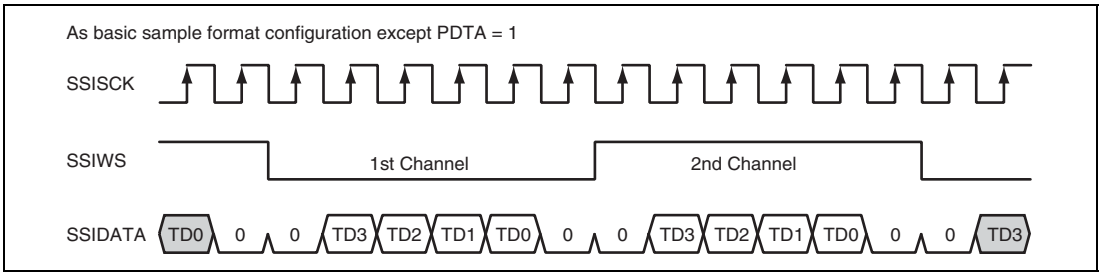



**Figure 18.17 Parallel Right-Aligned with Delay**

- Mute Enabled

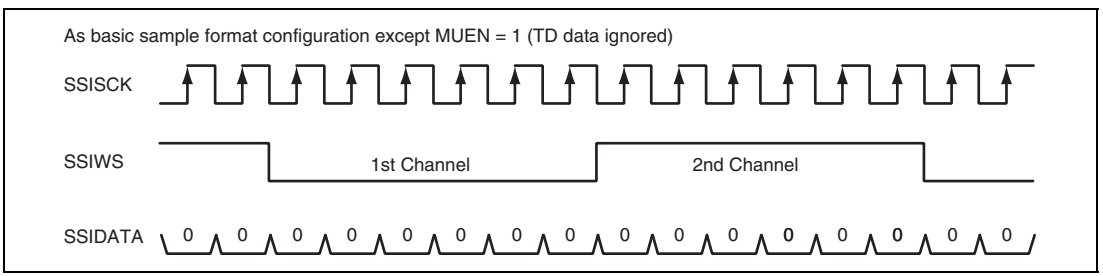



**Figure 18.18 Mute Enabled**

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 1 | ST_SECS | 0 | R | Indicates that a sector has been processed as a short sector with the aid of interpolated sync codes. If this bit is set to 1, stop decoding immediately and retry the procedure starting from the sector prior to the currently being decoded sector. |
| 0 | ST_SECL | 0 | R | Indicates that a sector has been processed as a long sector with the aid of interpolated sync codes. If this bit is set to 1, stop decoding immediately and retry the procedure starting from two sectors prior to the sector currently being decoded. |

### 23.3.9 Post-ECC Header Error Status Register (CROMST1)

The post-ECC header error status register (CROMST1) indicates error status in the post-ECC header.

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | - | - | - | - | ER2_HEAD0 | ER2_HEAD1 | ER2_HEAD2 | ER2_HEAD3 |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 7 to 4 | — | All 0 | R | Reserved<br>These bits are always read as 0 and cannot be modified. |
| 3 | ER2_HEAD0 | 0 | R | Indicates an error in the minutes field of the header after ECC correction. |
| 2 | ER2_HEAD1 | 0 | R | Indicates an error status in the seconds field of the header after ECC correction. |
| 1 | ER2_HEAD2 | 0 | R | Indicates an error in the frames (1/75 second) field of the header after ECC correction. |
| 0 | ER2_HEAD3 | 0 | R | Indicates an error in the mode field of the header after ECC correction. |

### 23.6.6 Note on Stream Data Transfer (1)

When reading of the stream data is slower than writing of the stream data, the buffer of the CD-ROM decoder will overflow. This causes the CD-ROM decoder to be abnormally stopped. Caution is required in writing and reading of the stream data. Sample combinations of stream data transfer settings are shown below.

**Table 23.4 Sample Combinations of Stream Data Transfer Settings**

| Stream Input | Stream Output |
|---|---|
| LW/cycle-stealing transfer by direct memory access controller (without padding) | (1) 16-byte/cycle-stealing transfer by direct memory access controller (16 bytes*)<br>(2) Burst transfer by direct memory access controller (16 bytes*, longword, word) |
| LW/cycle-stealing transfer by direct memory access controller (with padding) | (1) Cycle-stealing transfer by direct memory access controller (16 bytes*, longword)<br>(2) Burst transfer by direct memory access controller (16 bytes*, longword, word) |
| LW write by CPU | (1) Cycle-stealing transfer by direct memory access controller (16 bytes*, longword, word)<br>(2) Burst transfer by direct memory access controller (16 bytes*, longword, word) |

Note: * Set bit 25 in the DMA channel control register (CHCR_n) to 1, as well as making the regular settings for 16-byte transfer.

### 23.6.7 Note on Stream Data Transfer (2)

When reading the stream data, be sure to use either the direct memory access controller or the CPU. If both the direct memory access controller and the CPU are used for reading, the stream data may not be recognized as being in the CD-ROM format.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 12 | — | 0 | R | Reserved<br>This bit is always read as 0. The write value should always be 0. |
| 11 to 0 | DTLN[11:0] | H'000 | R | Receive Data Length<br>Indicates the length of the receive data.<br>While the FIFO buffer is being read, these bits indicate the different values depending on the RCNT bit value as described below.<br>• RCNT = 0:<br>This module sets these bits to indicate the length of the receive data until all the received data has been read from a single FIFO buffer plane.<br>While BFRE is 1, these bits retain the length of the receive data until BCLR is set to 1 even after all the data has been read.<br>• RCNT = 1:<br>This module decrements the value indicated by these bits each time data is read from the FIFO buffer. (The value is decremented by one when MBW is 00, by two when MBW is 01, and by four when MBW is 10.)<br>This module sets these bits to 0 when all the data has been read from one FIFO buffer plane. However, in double buffer mode, if data has been received in one FIFO buffer plane before all the data has been read from the other plane, this module sets these bits to indicate the length of the receive data in the former plane when all the data has been read from the latter plane.<br>Note: When RCNT is 1, it takes 10 bus cycles for these bits to be updated after the FIFO port has been read. |

Notes: 1. Only 0 can be read and 1 can be written.
2. Only 1 can be written.

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 9 | NRDY | 0 | R | Buffer Not Ready Interrupt Status<br>0: NRDY interrupts not generated<br>1: NRDY interrupts generated<br>This module sets this bit to 1 when at least one PIPENRDY bit in NRDYSTS is set to 1 among the PIPENRDY bits corresponding to the PIPENRDYE bits in NRDYENB to which 1 has been set (when this module detects the NRDY interrupt status in at least one pipe among the pipes for which the NRDY interrupt output is enabled).<br>For the conditions for PIPENRDY status assertion, refer to section 26.4.2 (2), NRDY Interrupt.<br>This module clears this bit to 0 when 0 is written to all the PIPENRDY bits corresponding to the PIPENRDYE bits to which 1 has been set.<br>This bit cannot be cleared to 0 even if 0 is written to this bit. |
| 8 | BRDY | 0 | R | Buffer Ready Interrupt Status<br>Indicates the BRDY interrupt status.<br>0: BRDY interrupts not generated<br>1: BRDY interrupts generated<br>This module sets this bit to 1 when at least one PIPEBRDY bit in BRDYSTS is set to 1 among the PIPEBRDY bits corresponding to the PIPEBRDYE bits in BRDYENB to which 1 has been set (when this module detects the BRDY interrupt status in at least one pipe among the pipes for which the BRDY interrupt output is enabled).<br>For the conditions for PIPEBRDY status assertion, refer to section 26.4.2 (1), BRDY Interrupt.<br>This module clears this bit to 0 when 0 is written to all the PIPEBRDY bits corresponding to the PIPEBRDYE bits to which 1 has been set.<br>This bit cannot be cleared to 0 even if 0 is written to this bit. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 4 | SACK | 0 | R/W*[1] | Setup Transaction Normal Response Interrupt Status<br>Indicates the status of the setup transaction normal response interrupt when the host controller function is selected.<br>0: SACK interrupts not generated<br>1: SACK interrupts generated<br>This module detects the SACK interrupt when ACK response is returned from the peripheral device during the setup transactions issued by this module, and sets this bit to 1. Here, if the corresponding interrupt enable bit has been set to 1, this module generates the SACK interrupt. |
| 3 to 0 | — | All 0 | R | Reserved<br>These bits are always read as 0. The write value should always be 0. |

Notes: 1. Only 0 can be written.

2. This module can detect a change in the status indicated by the BCHG bit even while the clock supply is stopped (while SCKE is 0), and outputs an interrupt when the corresponding interrupt enable bit is enabled. Clearing the status should be done after enabling the clock supply.
No interrupts other than BCHG can be detected while the clock supply is stopped (while SCKE is 0).

### 26.3.18 BRDY Interrupt Status Register (BRDYSTS)

BRDYSTS is a register that indicates the BRDY interrupt status for each pipe.

This register is initialized by a power-on reset.

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | PIPE9 BRDY | PIPE8 BRDY | PIPE7 BRDY | PIPE6 BRDY | PIPE5 BRDY | PIPE4 BRDY | PIPE3 BRDY | PIPE2 BRDY | PIPE1 BRDY | PIPE0 BRDY |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] | R/W*[1] |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 1 | HSYNC_TIM | 0 | R/W | Specifies the timing of the DV_HSYNC input signal.<br>0: Latched at the rising edge of the DV_CLK.<br>1: Latched at the falling edge of the DV_CLK. |
| 0 | VIDEO_TIM | 0 | R/W | Specifies the timing of the DV_DATA input signal.<br>0: Latched at the rising edge of the DV_CLK.<br>1: Latched at the falling edge of the DV_CLK. |

| Bit | Bit Name | Initial Value | R/W | Description |
|---|---|---|---|---|
| 2 | OVF | 0 | R/(W)*[1] | Output Data FIFO Overwrite Interrupt Request Flag<br>Indicates that the sampling rate conversion for the next data has been completed when the output data FIFO is full. The conversion is stopped until the OVF flag is cleared.<br>[Clearing conditions]<br>• When 0 has been written to the OVF bit after reading OVF = 1 while the OVEN bit in SRCCTRL is 1.<br>• When the number of data units in the output FIFO decreases after reading SRCOD while the OVEN bit in SRCCTRL is 0.<br>• When 1 has been written to the CL bit in SRCCTRL.<br>• When 1 has been written to the SRCEN bit in SRCCTRL while SRCEN is 0.<br>[Setting condition]<br>• When the sampling rate conversion for the next data has been completed when the output FIFO is full. |

| | Setting Mode Bit (PBnMD[1:0]) | | |
|---|---|---|---|
| | 00 | 01 | 10 |
| Setting Register | Function 1 | Function 2 | Function 3 |
| PDCR0 | PD3 | D3 | PWM1D |
| | PD2 | D2 | PWM1C |
| | PD1 | D1 | PWM1B |
| | PD0 | D0 | PWM1A |

Note: The function 2 of bus state controller and /or the function of NAND flush memory controller change automatically. (See section 9, Bus State Controller.).

**Table 32.6 Multiplexed Pins (Port E)**

| | Setting Mode Bit (PEnMD[2:0]) | | | | | |
|---|---|---|---|---|---|---|
| | 000 | 001 | 010 | 011 | 100 | 101 |
| Setting Register | Function 1 | Function 2 | Function 3 | Function 4 | Function 5 | Function 6 |
| PECR1 | PE5 | SDA2 | — | DV_HSYNC | — | — |
| | PE4 | SCL2 | — | DV_VSYNC | — | — |
| PECR0 | PE3 | SDA1 | — | IRQ3 | — | — |
| | PE2 | SCL1 | — | IRQ2 | — | — |
| | PE1 | SDA0 | $\overline{\text{IOIS16}}$ | IRQ1 | TCLKA | $\overline{\text{ADTRG}}$ |
| | PE0 | SCL0 | AUDIO_CLK | IRQ0 | — | — |

| Module Name | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| Direct memory access controller | RDMATCR_3 | — | — | — | — | — | — | — | — |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | SAR_4 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | DAR_4 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | DMATCR_4 | — | — | — | — | — | — | — | — |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | CHCR_4 | TC | — | RLDSAR | RLDDAR | — | DAF | SAF | — |
| | | — | — | — | TEMASK | HE | HIE | — | — |
| | | DM[1] | DM[0] | SM[1] | SM[0] | RS[3] | RS[2] | RS[1] | RS[0] |
| | | — | — | TB | TS[1] | TS[0] | IE | TE | DE |
| | RSAR_4 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | RDAR_4 | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |
| | | | | | | | | | |

| Module Name | Register Abbreviation | Bit 31/23/15/7 | Bit 30/22/14/6 | Bit 29/21/13/5 | Bit 28/20/12/4 | Bit 27/19/11/3 | Bit 26/18/10/2 | Bit 25/17/9/1 | Bit 24/16/8/0 |
|---|---|---|---|---|---|---|---|---|---|
| Controller area network | CYCTR_1 | CYCTR[15] | CYCTR[14] | CYCTR[13] | CYCTR[12] | CYCTR[11] | CYCTR[10] | CYCTR[9] | CYCTR[8] |
| | | CYCTR[7] | CYCTR[6] | CYCTR[5] | CYCTR[4] | CYCTR[3] | CYCTR[2] | CYCTR[1] | CYCTR[0] |
| | RFMK_1 | RFMK[15] | RFMK[14] | RFMK[13] | RFMK[12] | RFMK[11] | RFMK[10] | RFMK[9] | RFMK[8] |
| | | RFMK[7] | RFMK[6] | RFMK[5] | RFMK[4] | RFMK[3] | RFMK[2] | RFMK[1] | RFMK[0] |
| | TCMR0_1 | TCMR0[15] | TCMR0[14] | TCMR0[13] | TCMR0[12] | TCMR0[11] | TCMR0[10] | TCMR0[9] | TCMR0[8] |
| | | TCMR0[7] | TCMR0[6] | TCMR0[5] | TCMR0[4] | TCMR0[3] | TCMR0[2] | TCMR0[1] | TCMR0[0] |
| | TCMR1_1 | TCMR1[15] | TCMR1[14] | TCMR1[13] | TCMR1[12] | TCMR1[11] | TCMR1[10] | TCMR1[9] | TCMR1[8] |
| | | TCMR1[7] | TCMR1[6] | TCMR1[5] | TCMR1[4] | TCMR1[3] | TCMR1[2] | TCMR1[1] | TCMR1[0] |
| | TCMR2_1 | TCMR2[15] | TCMR2[14] | TCMR2[13] | TCMR2[12] | TCMR2[11] | TCMR2[10] | TCMR2[9] | TCMR2[8] |
| | | TCMR2[7] | TCMR2[6] | TCMR2[5] | TCMR2[4] | TCMR2[3] | TCMR2[2] | TCMR2[1] | TCMR2[0] |
| | TTTSEL_1 | — | TTTSEL[14] | TTTSEL[13] | TTTSEL[12] | TTTSEL[11] | TTTSEL[10] | TTTSEL[9] | TTTSEL[8] |
| | | — | — | — | — | — | — | — | — |
| | MBn_CONTROL0_H_1 (n = 0 to 31)*1 | — | STDID[10] | STDID[9] | STDID[8] | STDID[7] | STDID[6] | STDID[5] | STDID[4] |
| | | STDID[3] | STDID[2] | STDID[1] | STDID[0] | RTR | IDE | EXTID[17] | EXTID[16] |
| | MBn_CONTROL0_H_1 (n = 0 to 31)*2 | IDE | RTR | — | STDID[10] | STDID[9] | STDID[8] | STDID[7] | STDID[6] |
| | | STDID[5] | STDID[4] | STDID[3] | STDID[2] | STDID[1] | STDID[0] | EXTID[17] | EXTID[16] |
| | MBn_CONTROL0_L_1 (n = 0 to 31) | EXTID[15] | EXTID[14] | EXTID[13] | EXTID[12] | EXTID[11] | EXTID[10] | EXTID[9] | EXTID[8] |
| | | EXTID[7] | EXTID[6] | EXTID[5] | EXTID[4] | EXTID[3] | EXTID[2] | EXTID[1] | EXTID[0] |
| | MBn_LAFM0_1 (n = 0 to 31)*1 | — | STDID_LAFM[10] | STDID_LAFM[9] | STDID_LAFM[8] | STDID_LAFM[7] | STDID_LAFM[6] | STDID_LAFM[5] | STDID_LAFM[4] |
| | | STDID_LAFM[3] | STDID_LAFM[2] | STDID_LAFM[1] | STDID_LAFM[0] | — | IDE | EXTID_LAFM[17] | EXTID_LAFM[16] |
| | MBn_LAFM0_1 (n = 0 to 31)*2 | IDE | — | — | STDID_LAFM[10] | STDID_LAFM[9] | STDID_LAFM[8] | STDID_LAFM[7] | STDID_LAFM[6] |
| | | STDID_LAFM[5] | STDID_LAFM[4] | STDID_LAFM[3] | STDID_LAFM[2] | STDID_LAFM[1] | STDID_LAFM[0] | EXTID_LAFM[17] | EXTID_LAFM[16] |
| | MBn_LAFM1_1 (n = 0 to 31) | EXTID_LAFM[15] | EXTID_LAFM[14] | EXTID_LAFM[13] | EXTID_LAFM[12] | EXTID_LAFM[11] | EXTID_LAFM[10] | EXTID_LAFM[9] | EXTID_LAFM[8] |
| | | EXTID_LAFM[7] | EXTID_LAFM[6] | EXTID_LAFM[5] | EXTID_LAFM[4] | EXTID_LAFM[3] | EXTID_LAFM[2] | EXTID_LAFM[1] | EXTID_LAFM[0] |

| Item | Symbol | Bϕ = 72 MHz*1 Min. | Max. | Unit | Figure |
|---|---|---|---|---|---|
| $\overline{\text{IOIS16}}$ hold time | $T_{IO16H}$ | $1/2t_{cyc} + 3.5$ | — | ns | Figure 37.39 |
| $\overline{\text{RAS}}$ delay time 1 | $t_{RASD1}$ | 2*4 | 10.5 | ns | Figures 37.17 to 37.33 |
| $\overline{\text{RAS}}$ delay time 2 | $t_{RASD2}$ | $1/2t_{cyc}$ | $1/2t_{cyc} + 10.5$ | ns | Figures 37.34, 37.35 |
| $\overline{\text{CAS}}$ delay time 1 | $t_{CASD1}$ | 2*4 | 10.5 | ns | Figures 37.17 to 37.33 |
| $\overline{\text{CAS}}$ delay time 2 | $t_{CASD2}$ | $1/2t_{cyc}$ | $1/2t_{cyc} + 10.5$ | ns | Figures 37.34, 37.35 |
| DQM delay time 1 | $t_{DQMD1}$ | 2*4 | 10.5 | ns | Figures 37.17 to 37.30 |
| DQM delay time 2 | $t_{DQMD2}$ | $1/2t_{cyc}$ | $1/2t_{cyc} + 10.5$ | ns | Figures 37.34, 37.35 |
| CKE delay time 1 | $t_{CKED1}$ | 2*4 | 10.5 | ns | Figure 37.32 |
| CKE delay time 2 | $t_{CKED2}$ | $1/2t_{cyc}$ | $1/2t_{cyc} + 10.5$ | ns | Figure 37.35 |
| $\overline{\text{AH}}$ delay time | $t_{AHD}$ | $1/2t_{cyc}$ | $1/2t_{cyc} + 10.5$ | ns | Figure 37.13 |
| Multiplexed address delay time | $t_{MAD}$ | — | 10.5 | ns | Figure 37.13 |
| Multiplexed address hold time | $t_{MAH}$ | 1 | — | ns | Figure 37.13 |
| Address setup time for $\overline{\text{AH}}$ | $t_{AVVH}$ | $1/2t_{cyc} - 2$ | — | ns | Figure 37.13 |
| DACK, TEND delay time | $t_{DACD}$ | Refer to section 37.4.4, Direct Memory Access Controller Timing | | ns | Figures 37.9 to 37.30, 37.34, 37.36 to 37.39 |
| $\overline{\text{ICIORD}}$ delay time | $t_{ICRSD}$ | — | $1/2t_{cyc} + 10.5$ | ns | Figures 37.38, 37.39 |
| $\overline{\text{ICIOWR}}$ delay time | $t_{ICWSD}$ | — | $1/2t_{cyc} + 10.5$ | ns | Figures 37.38, 37.39 |

Notes: 1. The maximum value (fmax) of Bϕ (external bus clock) depends on the number of wait cycles and the system configuration of your board.

2. 1/2 $t_{cyc}$ indicated in minimum and maximum values for the item of delay, setup, and hold times represents a half cycle from the rising edge with a clock. That is, 1/2 $t_{cyc}$ describes a reference of the falling edge with a clock.

3. Values when SDRAM is used. Be sure to make necessary settings in ACSWR. (For details, refer to the descriptions from section 9.4.8, AC Characteristics Switching Register (ACSWR), to section 9.4.10, Sequence to Write to ACSWR.)

4. Be sure to make necessary settings in ACSWR. (For details, refer to the descriptions from section 9.4.8, AC Characteristics Switching Register (ACSWR), to section 9.4.10, Sequence to Write to ACSWR.)

### 37.4.10 Serial Sound Interface Timing

**Table 37.14 Serial Sound Interface Timing**

| Item | Symbol | Min. | Max. | Unit | Remarks | Figure |
|---|---|---|---|---|---|---|
| Output clock cycle | $t_O$ | 80 | 64000 | ns | Output | Figure 37.53 |
| Input clock cycle | $t_I$ | 80 | 64000 | ns | Input | |
| Clock high | $t_{HC}$ | 32 | — | ns | Bidirectional | |
| Clock low | $t_{LC}$ | 32 | — | ns | | |
| Clock rise time | $t_{RC}$ | — | 25 | ns | Output | |
| Delay | $t_{DTR}$ | –5 | 25 | ns | Transmit | Figures 37.54, 37.55 |
| Setup time | $t_{SR}$ | 25 | — | ns | Receive | |
| Hold time | $t_{HTR}$ | 5 | — | ns | Receive, transmit | |

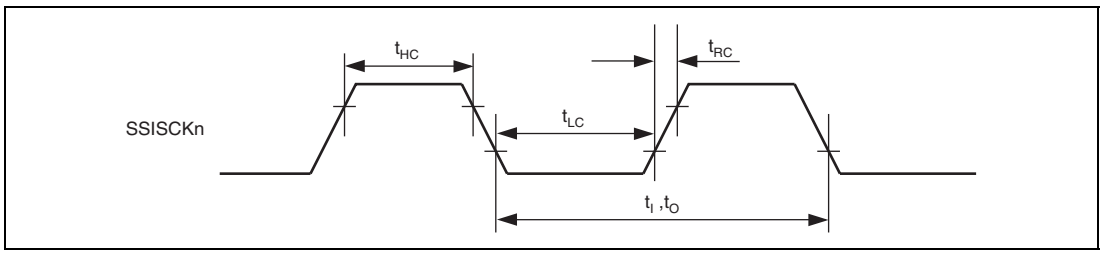



**Figure 37.53 Clock Input/Output Timing**

## P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## R


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