Renesas Electronics America Inc - R5S72641W144FP#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	115
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LFQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72641w144fp-u0

Section 2 CPU

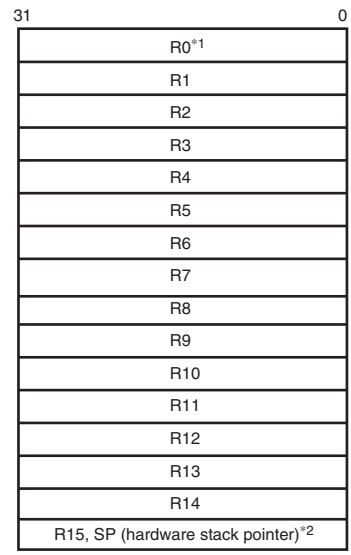
2.1 Register Configuration

The register set consists of sixteen 32-bit general registers, four 32-bit control registers, and four 32-bit system registers.

2.1.1 General Registers

Figure 2.1 shows the general registers.

The sixteen 32-bit general registers are numbered R0 to R15. General registers are used for data processing and address calculation. R0 is also used as an index register. Several instructions have R0 fixed as their only usable register. R15 is used as the hardware stack pointer (SP). Saving and restoring the status register (SR) and program counter (PC) in exception handling is accomplished by referencing the stack using R15.



Notes: 1. R0 functions as an index register in the indexed register indirect addressing mode and indexed GBR indirect addressing mode. In some instructions, R0 functions as a fixed source register or destination register.
2. R15 functions as a hardware stack pointer (SP) during exception processing.

Figure 2.1 General Registers

Bit	Bit Name	Initial Value	R/W	Description
4, 3	TRWL[1:0]*	00	R/W	Number of Auto-Precharge Startup Wait Cycles Specify the number of minimum auto-precharge startup wait cycles as shown below. • Cycle number from the issuance of the WRITA command by this LSI until the completion of auto-precharge in the SDRAM. Equivalent to the cycle number from the issuance of the WRITA command until the issuance of the ACTV command. Confirm that how many cycles are required between the WRITA command receive in the SDRAM and the auto-precharge activation, referring to each SDRAM data sheet. And set the cycle number so as not to exceed the cycle number specified by this bit. • Cycle number from the issuance of the WRIT command until the issuance of the PRE command. This is the case when accessing another low address in the same bank in bank active mode. The setting for areas 2 and 3 is common. 00: No cycle 01: 1 cycle 10: 2 cycles 11: 3 cycles
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

9.4.6 Refresh Timer Counter (RTCNT)

RTCNT is an 8-bit counter that increments using the clock selected by bits CKS[2:0] in RTCSR. When RTCNT matches RTCOR, RTCNT is cleared to 0. The value in RTCNT returns to 0 after counting up to 255. When the RTCNT is written, the upper 16 bits of the write data must be H'A55A to cancel write protection.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0.
7 to 0		All 0	R/W	8-Bit Counter

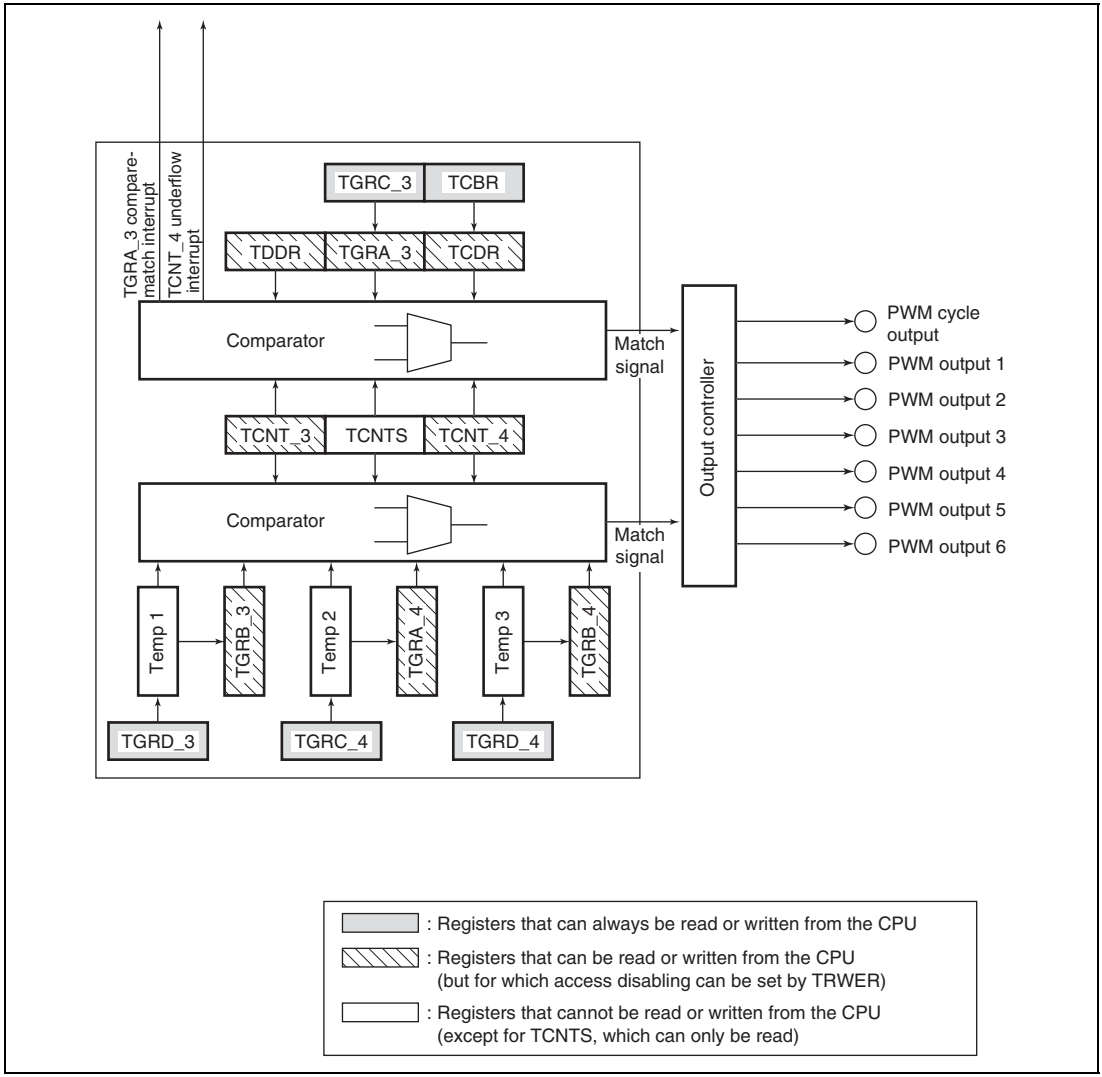


Figure 11.37 Block Diagram of Channels 3 and 4 in Complementary PWM Mode

11.7.16 Overflow Flags in Reset Synchronous PWM Mode

When set to reset synchronous PWM mode, TCNT_3 and TCNT_4 start counting when the CST3 bit of TSTR is set to 1. At this point, TCNT_4's count clock source and count edge obey the TCR_3 setting.

In reset synchronous PWM mode, with cycle register TGRA_3's set value at H'FFFF, when specifying TGR3A compare-match for the counter clear source, TCNT_3 and TCNT_4 count up to H'FFFF, then a compare-match occurs with TGRA_3, and TCNT_3 and TCNT_4 are both cleared. At this point, TSR's overflow flag TCFV bit is not set.

Figure 11.110 shows a TCFV bit operation example in reset synchronous PWM mode with a set value for cycle register TGRA_3 of H'FFFF, when a TGRA_3 compare-match has been specified without synchronous setting for the counter clear source.

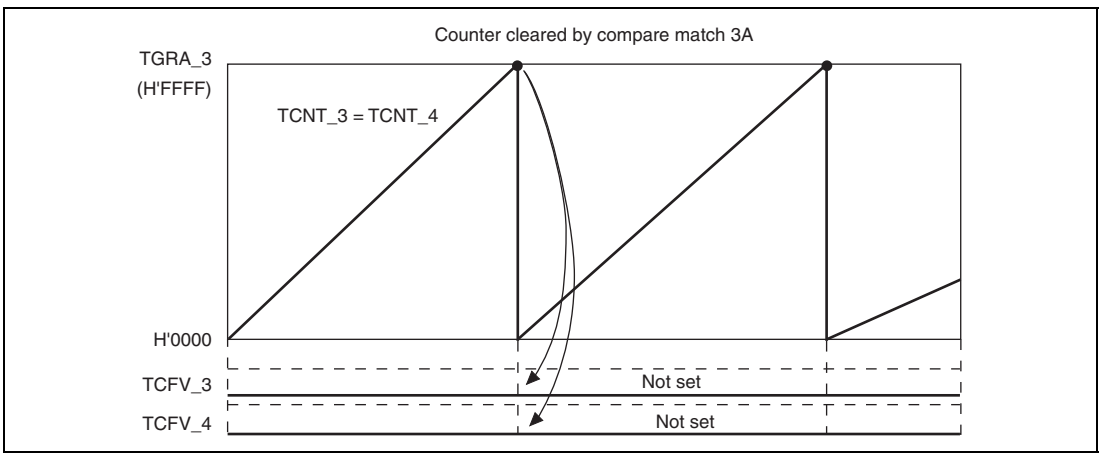


Figure 11.110 Reset Synchronous PWM Mode Overflow Flag

(3) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in PWM Mode 2

Figure 11.117 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in PWM mode 2 after re-setting.

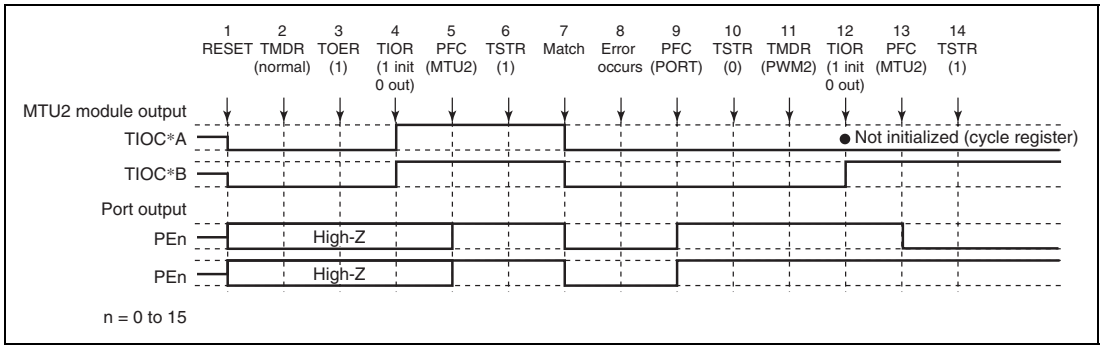


Figure 11.117 Error Occurrence in Normal Mode, Recovery in PWM Mode 2

1 to 10 are the same as in figure 11.115.

11. Set PWM mode 2.
12. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized. If initialization is required, initialize in normal mode, and then switch to PWM mode 2.)
13. Set the multi-function timer pulse unit 2 output with the general I/O port.
14. Operation is restarted by TSTR.

Note: PWM mode 2 can only be set for channels 0 to 2, and therefore TOER setting is not necessary.

(25) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Reset-Synchronized PWM Mode

Figure 11.139 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in reset-synchronized PWM mode.

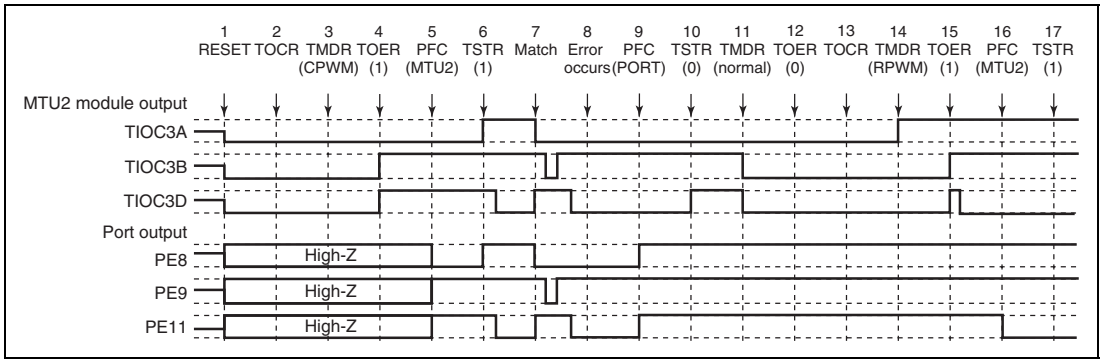


Figure 11.139 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

1 to 10 are the same as in figure 11.135.

11. Set normal mode. (This module outputs a low-level signal.)
12. Disable channel 3 and 4 output with TOER.
13. Select the reset-synchronized PWM mode output level and cyclic output enabling/disabling with TOCR.
14. Set reset-synchronized PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set the multi-function timer pulse unit 2 output with the general I/O port.
17. Operation is restarted by TSTR.

16.3.13 Command Register (SPCMD)

Each channel has four command registers (SPCMD0 to SPCMD3). SPCMD0 to SPCMD3 are used to set a transfer format for master mode operation. Some of the bits in SPCMD0 are used to set a transfer mode for slave mode operation. In master mode, this module sequentially references SPCMD0 to SPCMD3 according to the settings in bits SPSLN1 and SPSLN0 in the sequence control register (SPSCR), and executes the serial transfer that is set in the referenced SPCMD.

While bit TEND in the status register (SPSR) indicates that transmission is not completed, correct operation of this module cannot be guaranteed if SPCMD is changed that is referred by this module. SPCMD referenced by this module in master mode can be checked by means of bits SPCP1 and SPCP0 in the sequence status register (SPSSR). When the function of this module in master mode is enabled, operation cannot be guaranteed if the value set in SPCMD0 is changed.

Bit:	15	14	13	12	11	10	9	8
	SCK DEN	SLN DEN	SPN DEN	LSBF	SPB3	SPB2	SPB1	SPB0
Initial value:	0	0	0	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	SSLKP	—	—	—	BRDV1	BRDV0	CPOL	CPHA
Initial value:	0	0	0	0	1	1	0	1
R/W:	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SCKDEN	0	R/W	RSPCK Delay Setting Enable Sets the period from the point this module in master mode activates the SSL signal until the RSPCK starts oscillation (RSPCK delay). If the SCKDEN bit is 0, this module sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, this module starts the oscillation of RSPCK at an RSPCK delay in compliance with the clock delay register (SPCKD) settings. To use this module in slave mode, the SCKDEN bit should be set to 0. 0: An RSPCK delay of 1 RSPCK 1: An RSPCK delay equal to SPCKD settings.

(e) Initialization Flowchart

Figure 16.19 is a flowchart illustrating an example of initialization in SPI operation when this module is used in slave mode. For a description of how to set up the interrupt controller, direct memory access controller, and input/output ports, see the descriptions given in the individual blocks.

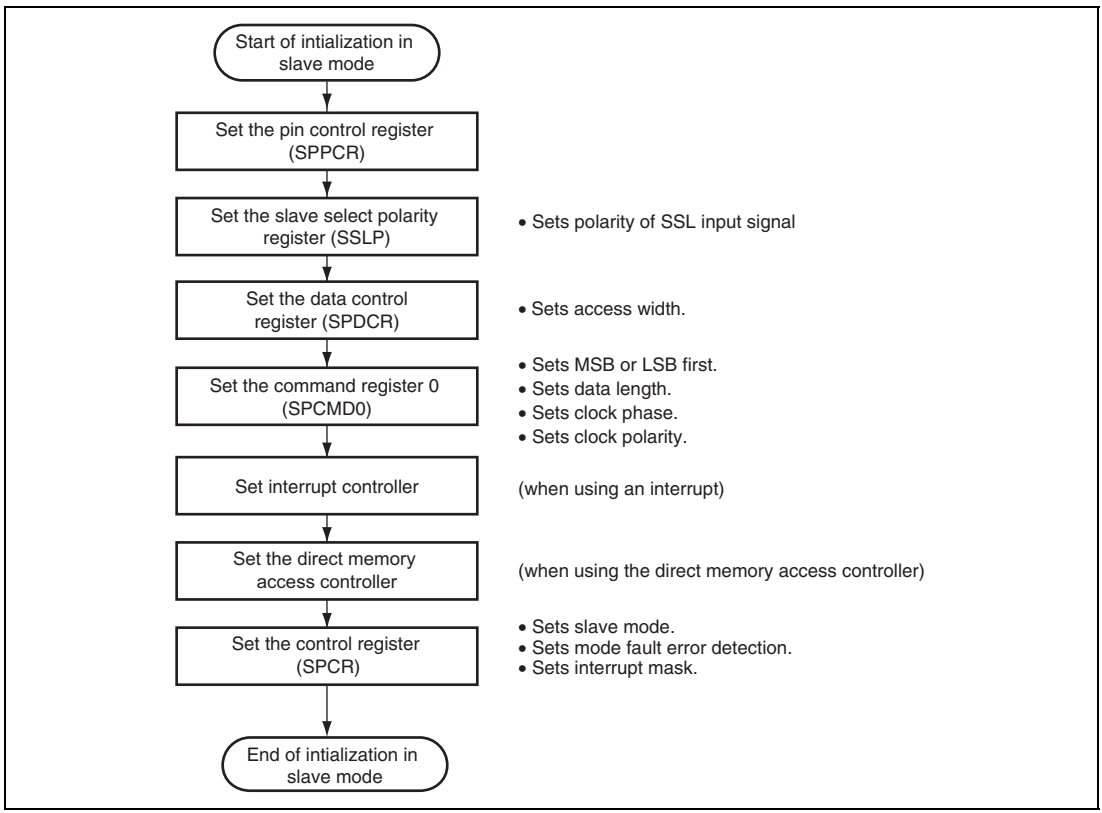


Figure 16.19 Example of Initialization Flowchart in Slave Mode

Bit	Interrupt Name	Cause of Interrupt	Function That Generates the Interrupt	Related Status
CTRT	Control transfer stage transition interrupt	When a stage transition is detected in control transfer • Setup stage completed • Control write transfer status stage transition • Control read transfer status stage transition • Control transfer completed • A control transfer sequence error occurred	Function	CTSQ
BEMP	Buffer empty interrupt	• When transmission of all of the data in the buffer memory has been completed • When an excessive maximum packet size error has been detected	Host, Function	BEMPSTS. PIPEBEMP

26.4.7 Interrupt Transfers (PIPE6 to PIPE9)

When the function controller function is selected, this module carries out interrupt transfers in accordance with the timing controlled by the host controller. For interrupt transfers, PING packets are ignored (no responses are sent), and the ACK, NAK, and STALL responses are carried out without an NYET handshake response being made.

When the host controller function is selected, this module can set the timing of issuing a token using the interval timer. At this time, this module issues an OUT token even in the OUT direction, without issuing a PING token.

This module does not support high bandwidth transfers of interrupt transfers.

(1) Interval Counter during Interrupt Transfers when the Host Controller Function is Selected

For interrupt transfers, intervals between transactions are set in the IITV bits in PIPEPERI. This controller issues an interrupt transfer token based on the specified intervals.

(a) Counter Initialization

This controller initializes the interval counter under the following conditions.

- Power-on reset
  The IITV bits are initialized.
- Buffer memory initialization using the ACLRM bit
  The IITV bits are not initialized but the count value is. Setting the ACLRM bit to 0 starts counting from the value set in the IITV bits.

Note that the interval counter is not initialized in the following case.

- USB bus reset, USB suspended
  The IITV bits are not initialized. Setting 1 to the UACT bit starts counting from the value before entering the USB bus reset state or USB suspended state.

Section 32 General Purpose I/O Ports

This LSI has 10 general purpose I/O ports: A, B, C, D, E, F, G, H, J, and K.

All port pins are multiplexed with other peripheral module pin functions.

Each port is provided with registers for selecting the pin functions and those I/O directions of multiplex pins, data registers for storing the pin data and port registers for reading the states of the pins.

32.1 Features

- By setting the control registers, multiplexed pin functions can be selectable.
- When the general I/O function or TIOC I/O function of multi-function timer pulse unit 2 is specified, the I/O direction can be selected by I/O register settings.

Table 32.1 Number of General Purpose I/O Pins

Port	SH7262	SH7264
A	4 I/O pins	
B	22 I/O pins	
C	9 I/O pins	11 I/O pins
D	16 I/O pins	
E	6 input pins with open-drain outputs	
F	13 I/O pins	
G	21 I/O pins	25 I/O pins
H	4 input pins	8 input pins
J	4 I/O pins	12 I/O pins
K	No pin	12 I/O pins
Total	99 pins (89 I/O pins, 6 input pins with open-drain outputs, and 4 input pins)	129 pins (115 I/O pins, 6 input pins with open-drain outputs, and 8 input pins)

(4) Port B Control Register 2 (PBCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PB11MD[1:0]		-	-	PB10MD[1:0]		-	-	PB9MD[1:0]		-	-	PB8MD[1:0]	
Initial value:	0	0	0	0/1	0	0	0	0/1	0	0	0	0/1	0	0	0	0/1
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	PB11MD[1:0]	00/01	R/W	PB11 Mode Select the function of the PB11. Boot mode 0 / Boot mode 1 to 3 00: Setting prohibited / 00: PB11 (initial value) 01: A11 (initial value) / 01: A11 (initial value) 10: Setting prohibited / 10: TIOC2B 11: Setting prohibited / 11: Setting prohibited
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PB10MD[1:0]	00/01	R/W	PB10 Mode Select the function of the PB10. Boot mode 0 / Boot mode 1 to 3 00: Setting prohibited / 00: PB10 (initial value) 01: A10 (initial value) / 01: A10 (initial value) 10: Setting prohibited / 10: TIOC2A 11: Setting prohibited / 11: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	MSTP43	1	R/W	Module Stop 43 When the MSTP43 bit is set to 1, the clock supply to channel 4 of the serial communication unit with FIFO is halted. 0: Channel 4 of the serial communication unit with FIFO runs. 1: Clock supply to channel 4 of the serial communication unit with FIFO is halted.
2	MSTP42	1	R/W	Module Stop 42 When the MSTP42 bit is set to 1, the clock supply to channel 5 of the serial communication unit with FIFO is halted. 0: Channel 5 of the serial communication unit with FIFO runs. 1: Clock supply to channel 5 of the serial communication unit with FIFO is halted.
1	MSTP41	1	R/W	Module Stop 41 When the MSTP41 bit is set to 1, the clock supply to channel 6 of the serial communication unit with FIFO is halted. 0: Channel 6 of the serial communication unit with FIFO runs. 1: Clock supply to channel 6 of the serial communication unit with FIFO is halted.
0	MSTP40	1	R/W	Module Stop 40 When the MSTP40 bit is set to 1, the clock supply to channel 7 of the serial communication unit with FIFO is halted. 0: Channel 7 of the serial communication unit with FIFO runs. 1: Clock supply to channel 7 of the serial communication unit with FIFO is halted.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	RRAMWE3	0	R/W	RAM Write Enable 3 (corresponding area: page 3*3*4 in on-chip data-retention RAM) 0: Writing to page 3 is disabled. 1: Writing to page 3 is enabled.
2	RRAMWE2	0	R/W	RAM Write Enable 2 (corresponding area: page 2*2 in on-chip data-retention RAM 0: Writing to page 2 is disabled. 1: Writing to page 2 is enabled.
1	RRAMWE1	0	R/W	RAM Write Enable 1 (corresponding area: page 1*2 in on-chip data-retention RAM 0: Writing to page 1 is disabled. 1: Writing to page 1 is enabled.
0	RRAMWE0	0	R/W	RAM Write Enable 0 (corresponding area: page 0*2 in on-chip data-retention RAM) 0: Writing to page 0 is disabled. 1: Writing to page 0 is enabled.

Notes: 1. For addresses in each page, see section 31, On-Chip RAM.

2. When the VRAME0 bit in SYSCR3 is cleared to 0 (access to page 0 in large-capacity on-chip RAM is invalid), the on-chip data-retention RAM cannot be accessed (read and written), regardless of the setting of this bit.
When the VRAMWE0 bit in SYSCR4 is cleared to 0 (writing to page 0 in large-capacity on-chip RAM is invalid), the on-chip data-retention RAM cannot be written, regardless of the setting of this bit.

3. When the VRAME1 bit in SYSCR3 is cleared to 0 (access to page 1 in large-capacity on-chip RAM is invalid), the first half (page 1 in large-capacity on-chip RAM) of the on-chip data-retention RAM cannot be accessed (read and written), regardless of the setting of this bit.
When the VRAME1 bit in SYSCR4 is cleared to 0 (writing to page 1 in large-capacity on-chip RAM is invalid), the first half of the on-chip data-retention RAM cannot be written, regardless of the setting of this bit.

4. When the VRAME2 bit in SYSCR3 is cleared to 0 (access to page 2 in large-capacity on-chip RAM is invalid), the second half (page 2 in large-capacity on-chip RAM) of the on-chip data-retention RAM cannot be accessed (read and written), regardless of the setting of this bit.
When the VRAMWE2 bit in SYSCR4 is cleared to 0 (writing to page 2 in large-capacity on-chip RAM is invalid), the second half of the on-chip data-retention RAM cannot be written, regardless of the setting of this bit.

33.3.2 Software Standby Mode

(1) Transition to Software Standby Mode

The LSI switches from a program execution state to software standby mode by executing the SLEEP instruction when the STBY bit and DEEP bit in STBCR1 are 1 and 0 respectively. In software standby mode, not only the CPU but also the clock and on-chip peripheral modules halt. The clock output from the CKIO pin also stops.

The contents of the CPU and cache registers remain unchanged. Some registers of on-chip peripheral modules are, however, initialized. As for the states of on-chip peripheral module registers in software standby mode, see section 36.3, Register States in Each Operating Mode.

The CPU takes one cycle to finish writing to STBCR1, and then executes processing for the next instruction. However, it takes one or more cycles to actually write. Therefore, execute a SLEEP instruction after reading STBCR1 to have the values written to STBCR1 by the CPU to be definitely reflected in the SLEEP instruction.

The procedure for switching to software standby mode is as follows:

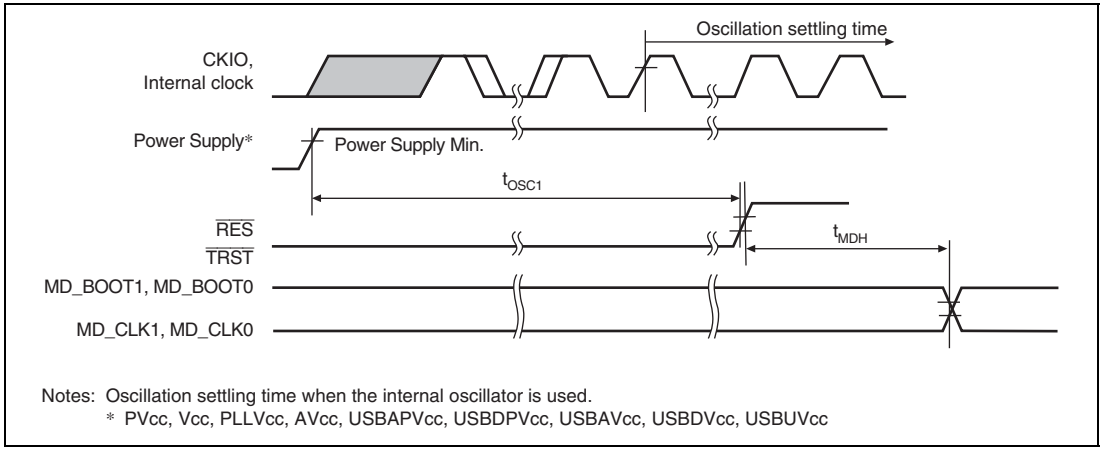
1. Clear the TME bit in the timer control register of the watchdog timer (WTCSR) to 0 to stop the watchdog time.
2. Set the timer counter of the watchdog timer (WTCNT) to 0 and the CKS[2:0] bits in WTCSR to appropriate values to secure the specified oscillation settling time.
3. After setting the STBY and DEEP bits in STBCR1 to 1 and 0 respectively, read STBCR1. Then, execute a SLEEP instruction.

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
CD-ROM decoder	Post-ECC correction subheader: sub-mode (byte 22) data register	SHEAD26	8	H'FFFF902E	8
	Post-ECC correction subheader: data type (byte 23) data register	SHEAD27	8	H'FFFF902F	8
	Automatic buffering setting control register	CBUFCTL0	8	H'FFFF9040	8
	Automatic buffering start sector setting:minutes control register	CBUFCTL1	8	H'FFFF9041	8
	Automatic buffering start sector setting:seconds control register	CBUFCTL2	8	H'FFFF9042	8
	Automatic buffering start sector setting:frames control register	CBUFCTL3	8	H'FFFF9043	8
	ISY interrupt source mask control register	CROMST0M	8	H'FFFF9045	8
	CD-ROM decoder reset control register	ROMDECRST	8	H'FFFF9100	8
	CD-ROM decoder reset status register	RSTSTAT	8	H'FFFF9101	8
	Serial sound interface data control register	SSI	8	H'FFFF9102	8
	Interrupt flag register	INTHOLD	8	H'FFFF9108	8
	Interrupt source mask control register	INHINT	8	H'FFFF9109	8
	CD-ROM decoder stream data input register	STRMDIN0	16	H'FFFF9200	16, 32*
	CD-ROM decoder stream data input register	STRMDIN2	16	H'FFFF9202	16
	CD-ROM decoder stream data output register	STRMDOUT0	16	H'FFFF9204	16, 32
A/D converter	A/D data register A	ADDRA	16	H'FFFF9800	16
	A/D data register B	ADDRB	16	H'FFFF9802	16
	A/D data register C	ADDRC	16	H'FFFF9804	16
	A/D data register D	ADDRD	16	H'FFFF9806	16
	A/D data register E	ADDRE	16	H'FFFF9808	16
	A/D data register F	ADDRF	16	H'FFFF980A	16
	A/D data register G	ADDRG	16	H'FFFF980C	16
	A/D data register H	ADDRH	16	H'FFFF980E	16
	A/D control/status register	ADCSR	16	H'FFFF9820	16

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
Serial I/O with FIFO	SICTR	SCKE	FSE	—	—	—	—	TXE	RXE
		—	—	—	—	—	—	TXRST	RXRST
	SIFCTR	TFWM[2]	TFWM[1]	TFWM[0]	TFUA[4]	TFUA[3]	TFUA[2]	TFUA[1]	TFUA[0]
		RFWM[2]	RFWM[1]	RFWM[0]	RFUA[4]	RFUA[3]	RFUA[2]	RFUA[1]	RFUA[0]
	SISTR	—	—	TFEMP	TDREQ	—	—	RFFUL	RDREQ
		—	—	—	FSERR	TFOVF	TFUDF	RFUDF	RFOVF
	SIIER	TDMAE	—	TFEMPE	TDREQE	RDMAE	—	RFFULE	RDREQE
		—	—	—	FSERRE	TFOVFE	TFUDFE	RFUDFE	RFOVFE
	SITDR	SITDL[15]	SITDL[14]	SITDL[13]	SITDL[12]	SITDL[11]	SITDL[10]	SITDL[9]	SITDL[8]
		SITDL[7]	SITDL[6]	SITDL[5]	SITDL[4]	SITDL[3]	SITDL[2]	SITDL[1]	SITDL[0]
		SITDR[15]	SITDR[14]	SITDR[13]	SITDR[12]	SITDR[11]	SITDR[10]	SITDR[9]	SITDR[8]
		SITDR[7]	SITDR[6]	SITDR[5]	SITDR[4]	SITDR[3]	SITDR[2]	SITDR[1]	SITDR[0]
	SIRDR	SIRDL[15]	SIRDL[14]	SIRDL[13]	SIRDL[12]	SIRDL[11]	SIRDL[10]	SIRDL[9]	SIRDL[8]
		SIRDL[7]	SIRDL[6]	SIRDL[5]	SIRDL[4]	SIRDL[3]	SIRDL[2]	SIRDL[1]	SIRDL[0]
		SIRDR[15]	SIRDR[14]	SIRDR[13]	SIRDR[12]	SIRDR[11]	SIRDR[10]	SIRDR[9]	SIRDR[8]
		SIRDR[7]	SIRDR[6]	SIRDR[5]	SIRDR[4]	SIRDR[3]	SIRDR[2]	SIRDR[1]	SIRDR[0]
Controller area network	MCR_0	MCR15	MCR14	—	—	—	TST[2]	TST[1]	TST[0]
		MCR7	MCR6	MCR5	—	—	MCR2	MCR1	MCR0
	GSR_0	—	—	—	—	—	—	—	—
		—	—	GSR5	GSR4	GSR3	GSR2	GSR1	GSR0
	BCR1_0	TSG1[3]	TSG1[2]	TSG1[1]	TSG1[0]	—	TSG2[2]	TSG2[1]	TSG2[0]
		—	—	SJW[1]	SJW[0]	—	—	—	BSP
	BCR0_0	—	—	—	—	—	—	—	—
		BRP[7]	BRP[6]	BRP[5]	BRP[4]	BRP[3]	BRP[2]	BRP[1]	BRP[0]
	IRR_0	IRR15	IRR14	IRR13	IRR12	IRR11	IRR10	IRR9	IRR8
		IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0
	IMR_0	IMR15	IMR14	IMR13	IMR12	IMR11	IMR10	IMR9	IMR8
		IMR7	IMR6	IMR5	IMR4	IMR3	IMR2	IMR1	IMR0
	TEC_REC_0	TEC[7]	TEC[6]	TEC[5]	TEC[4]	TEC[3]	TEC[2]	TEC[1]	TEC[0]
		REC[7]	REC[6]	REC[5]	REC[4]	REC[3]	REC[2]	REC[1]	REC[0]

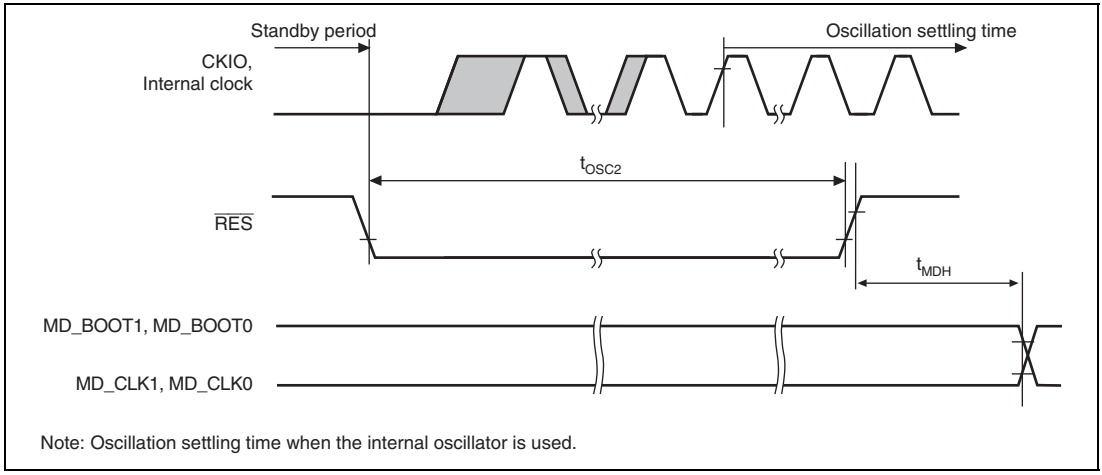
Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
Motor control PWM timer	PWBFR_2A	—	—	—	OTS	—	—	DT9	DT8
		DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
	PWBFR_2C	—	—	—	OTS	—	—	DT9	DT8
		DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
	PWBFR_2E	—	—	—	OTS	—	—	DT9	DT8
		DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
	PWBFR_2G	—	—	—	OTS	—	—	DT9	DT8
		DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
	PWBTCR	BTC2G	BTC2E	BTC2C	BTC2A	BTC1G	BTC1E	BTC1C	BTC1A
		—	—	—	—	—	—	—	—

Notes: 1. When MCR15=0
2. When MCR15=1
3. In command access mode
4. In sector access mode



Notes: Oscillation settling time when the internal oscillator is used.
* PVcc, Vcc, PLLVcc, AVcc, USBAPVcc, USBDPVcc, USBAVcc, USBDVcc, USBUVcc

Figure 37.3 Power-On Oscillation Settling Time



Note: Oscillation settling time when the internal oscillator is used.

Figure 37.4 Oscillation Settling Time on Return from Standby (Return by Reset)