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Details	
Product Status	Last Time Buy
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	115
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LFQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72643p144fp-uz

Classification	Symbol	I/O	Name	Function
NAND flash memory controller	FALE	O	Flash memory address latch enable	Asserted for address output and negated for data I/O. Negated at data input/output.
	$\overline{\text{FRE}}$	O	Flash memory read enable	Reads data at falling edge.
	$\overline{\text{FCE}}$	O	Flash memory chip enable	Enables the flash memory connected to this LSI.
	FCLE	O	Flash memory command latch enable	Asserted at command output.
	FRB	I	Flash memory ready/busy	High level indicates ready state and low level indicates busy state.
	$\overline{\text{FWE}}$	O	Flash memory write enable	Flash memory latches commands, addresses, and data at rising edge.
	NAF7 to NAF0	I/O	Flash memory data	Data I/O pins.
USB 2.0 host/function module	DP	I/O	USB 2.0 host/function module D+ data	D+ data pin for USB 2.0 host/function module bus.
	DM	I/O	USB 2.0 host/function module D– data	D– data pin for USB 2.0 host/function module bus.
	VBUS	I	VBUS input	Connected to Vbus on USB 2.0 host/function module bus.
	REFRIN	I	Reference input	Connected to USBAPVss via 5.6-k$\Omega \pm 1\%$ resistance.
	USB_X1	I	Crystal resonator/ external clock for USB 2.0 host/function module	Connected to a crystal resonator for USB 2.0 host/function module. An external clock signal may also be input to the USB_X1 pin.
	USB_X2	O		
	USBAPVcc	I	Power supply for transceiver analog pins	Power supply for pins.

6.7 When Exception Sources Are Not Accepted

When an address error, FPU exception, register bank error (overflow), or interrupt is generated immediately after a delayed branch instruction, it is sometimes not accepted immediately but stored instead, as shown in table 6.11. When this happens, it will be accepted when an instruction that can accept the exception is decoded.

Table 6.11 Exception Source Generation Immediately after Delayed Branch Instruction

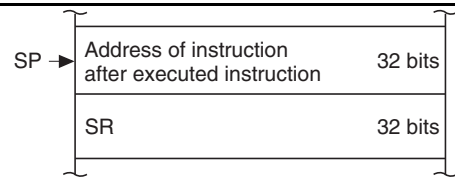
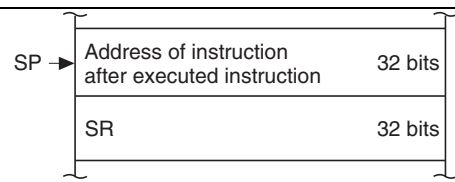
	Exception Source			
Point of Occurrence	Address Error	Floating-Point Unit Exception	Register Bank Error (Overflow)	Interrupt
Immediately after a delayed branch instruction*	Not accepted	Not accepted	Not accepted	Not accepted

Note: * Delayed branch instructions: JMP, JSR, BRA, BSR, RTS, RTE, BF/S, BT/S, BSRF, BRAF

6.8 Stack Status after Exception Handling Ends

The status of the stack after exception handling ends is as shown in table 6.12.

Table 6.12 Stack Status After Exception Handling Ends

Exception Type	Stack Status
Address error	
Interrupt	

(4) The Other Exceptions

Before the exception handling vector table is stored in a memory and the settings necessary to access the memory are completed, the exception handling should not be generated.

9.4.8 AC Characteristics Switching Register (ACSWR)

To use the SDRAM, set the AC characteristics switching register (ACSWR) and AC characteristics key switching register (ACKEYR).

Only a special sequence can write to this register to prevent accidental erroneous write. The setting procedure is shown in section 9.4.10, Sequence to Write to ACSWR. Read is done by the normal longword.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	ACOSW[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	ACOSW[3:0]	0000	R/W	AC Characteristics Switch Specifies AC characteristics switching 0000: Not extend the delay time 0010: Switches characteristics and extends the delay time Others: Setting prohibited

- DMARS6

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH13 MID[5:0]						CH13 RID[1:0]		CH12 MID[5:0]						CH12 RID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- DMARS7

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CH15 MID[5:0]						CH15 RID[1:0]		CH14 MID[5:0]						CH14 RID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Transfer requests from the various modules specify MID and RID as shown in table 10.3.

Table 10.3 DMARS Settings

Peripheral Module	Setting Value for One Channel ({MID, RID})	MID	RID	Function
USB 2.0 host/function module	H'03	B'000000	B'11	Channel 0 FIFO
	H'07	B'000001	B'11	Channel 1 FIFO
Renesas SPDIF interface	H'09	B'000010	B'01	Transmit
	H'0A	B'000010	B'10	Receive
SD host interface	H'11	B'000100	B'01	SD_BUF write
	H'12		B'10	SD_BUF read
Clock synchronous serial I/O with FIFO	H'19	B'000110	B'01	Transmit
	H'1A		B'10	Receive
Serial sound interface Channel 0	H'21	B'001000	B'01	Transmit
	H'22		B'10	Receive
Serial sound interface Channel 1	H'27	B'001001	B'11	—
Serial sound interface Channel 2	H'2B	B'001010	B'11	—

Table 11.25 TIORH_4 (Channel 4)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_4 Function**	**TIOC4A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	X	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

Bit	Bit Name	Initial Value	R/W	Description
4	CIE	0	R/W	Carry Interrupt Enable Flag When the carry flag (CF) is set to 1, the CIE bit enables interrupts. 0: A carry interrupt is not generated when the CF flag is set to 1 1: A carry interrupt is generated when the CF flag is set to 1
3	AIE	0	R/W	Alarm Interrupt Enable Flag When the alarm flag (AF) is set to 1, the AIE bit allows interrupts. 0: An alarm interrupt is not generated when the AF flag is set to 1 1: An alarm interrupt is generated when the AF flag is set to 1
2, 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	AF	Undefined	R/W	Alarm Flag The AF flag is set when the alarm time, which is set by an alarm register (ENB bit in RSECAR, RMINAR, RHRAR, RWKAR, RDAYAR, RMONAR, or RYRAR is set to 1), and counter match. 0: Alarm register and counter not match [Clearing condition] When 0 is written to AF. 1: Alarm register and counter match* [Setting condition] When alarm register (only a register with ENB bit set to 1) and counter match Note: * Writing 1 holds previous value.

15.3.12 Line Status Register (SCLSR)

The CPU can always read or write to SCLSR, but cannot write 1 to the ORER flag. This flag can be cleared to 0 only if it has first been read (after being set to 1).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ORER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*

Note: * Only 0 can be written to clear the flag after 1 is read.

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ORER	0	R/(W)*	Overrun Error Indicates the occurrence of an overrun error. 0: Receiving is in progress or has ended normally*[1] [Clearing conditions] • ORER is cleared to 0 when the chip is a power-on reset • ORER is cleared to 0 when 0 is written after 1 is read from ORER. 1: An overrun error has occurred*[2] [Setting condition] • ORER is set to 1 when the next serial receiving is finished while the receive FIFO is full of 16-byte receive data. Notes: 1. Clearing the RE bit to 0 in SCSCR does not affect the ORER bit, which retains its previous value. 2. The receive FIFO data register (SCFRDR) retains the data before an overrun error has occurred, and the next received data is discarded. When the ORER bit is set to 1, the next serial reception cannot be continued.

16.3.5 Data Register (SPDR)

SPDR is a buffer that holds data for transmission and reception.

The transmit buffer (SPTX) and receive buffer (SPRX) are independent and are mapped to SPDR.

SPDR should be read or written to in byte, word, or longword units according to the access width specification bit (SPLW) in the data control register (SPDCR).

The bit length to be used is determined by the data length specification bits (SPB3 to SPB0) in the command register (SPCMD).

When data is written to SPDR, the data will be written to the transmit buffer from SPDR if the transmit buffer has a space equal to or more than the SPDR access width. If there is not enough space, data will not be written to the transmit buffer. Even if an attempt is made to write data to the buffer, the data is ignored.

When data is read from SPDR, receive data in the receive buffer will be read. If SPDR is read when there is no receive data in the receive buffer, the read value is undefined.

When SPDR is written to with the longword-, word-, or byte-access width, the transmit data should be written to the following bits. If data is written to the other bits, the data is not guaranteed.

- Longword: Bits 31 to 0
- Word: Bits 31 to 16
- Byte: Bits 31 to 24

When SPDR is read with the longword-, word-, or byte-access width, the receive data should be read from the following bits. If data is read from the other bits, the data is not guaranteed.

- Longword: Bits 31 to 0
- Word: Bits 31 to 16
- Byte: Bits 31 to 24

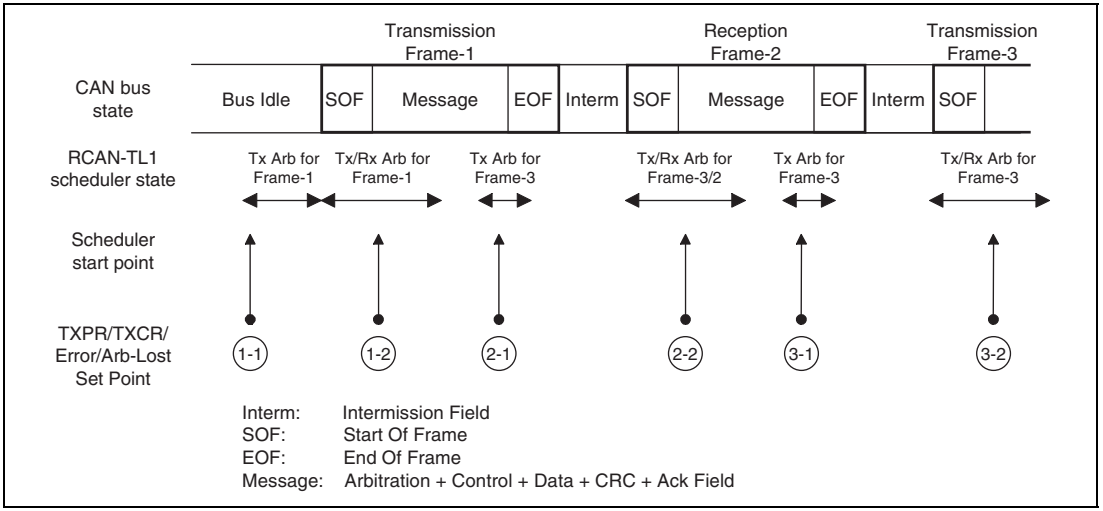


Figure 20.17 Internal Arbitration for transmission

This module has two state machines. One is for transmission, and the other is for reception.

1-1: When a TXPR bit(s) is set while the CAN bus is idle, the internal arbitration starts running immediately and the transmission is started.

1-2: Operations for both transmission and reception starts at SOF. Since there is no reception frame, this module becomes transmitter.

2-1: At crc delimiter, internal arbitration to search next message transmitted starts.

2-2: Operations for both transmission and reception starts at SOF. Because of a reception frame with higher priority, this module becomes receiver. Therefore, Reception is carried out instead of transmitting Frame-3.

3-1: At crc delimiter, internal arbitration to search next message transmitted starts.

3-2: Operations for both transmission and reception starts at SOF. Since a transmission frame has higher priority than reception one, this module becomes transmitter.

Internal arbitration for the next transmission is also performed at the beginning of each error delimiter in case of an error is detected on the CAN Bus. It is also performed at the beginning of error delimiters following overload frame.

As the arbitration for transmission is performed at CRC delimiter, in case a remote frame request is received into a Mailbox with ATX = 1 the answer can join the arbitration for transmission only at the following Bus Idle, CRC delimiter or Error Delimiter.

Depending on the status of the CAN bus, following the assertion of the TXCR, the corresponding Message abortion can be handled with a delay of maximum 1 CAN Frame.

20.7 CAN Bus Interface

A bus transceiver IC is necessary to connect this LSI to a CAN bus. A Renesas HA13721 transceiver IC and its compatible products are recommended. As the CRx and CTx pins use 3 V, an external level shifter is necessary. Figure 20.27 shows a sample connection diagram.

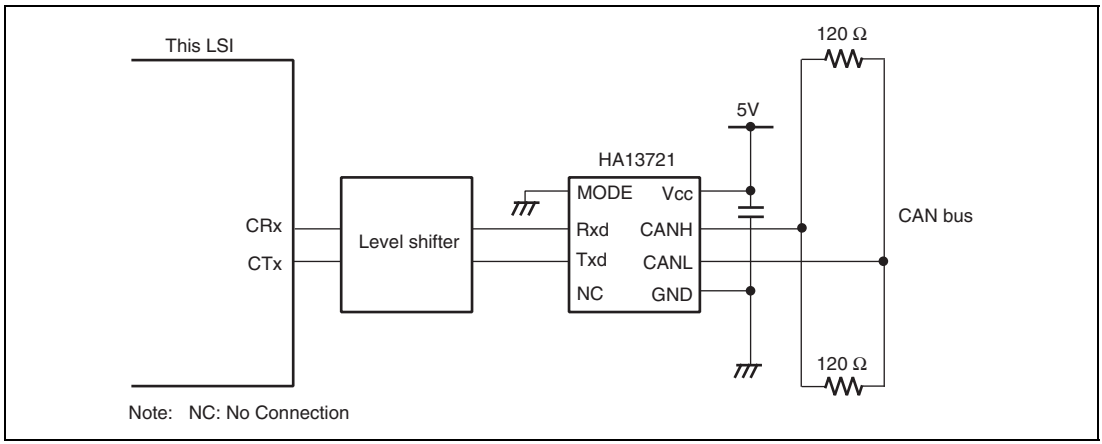


Figure 20.27 High-Speed CAN Interface Using HA13721

21.3.3 IEBus Master Control Register (IEMCR)

IEMCR sets the communication conditions for master communications.

Bit:	7	6	5	4	3	2	1	0
	SS	RN			CTL*1			
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	SS	0	R/W	Broadcast/Normal Communications Select Selects broadcast or normal communications for master communications. 0: Broadcast communications for master communications 1: Normal communications for master communications
6 to 4	RN	000	R/W	Retransmission Counts Set the number of times retransmission is done when arbitration is lost in master communications. If arbitration is lost, the TXEAL flag in IETSR is set and transmission ends. 000: 0 001: 1 010: 2 011: 3 100: 4 101: 5 110: 6 111: 7

Bit	Bit Name	Initial Value	R/W	Description
2	TXETTME	0	R/(W)*	Transmit Timing Error Set to 1 if data is not transmitted at the timing specified by the IEBus protocol during data transmission. This module sets this bit and enters the wait state. [Setting condition] • When a timing error occurs during data transmission [Clearing condition] • When 1 is written
1	TXERO	0	R/(W)*	Overflow of Maximum Number of Transmit Bytes in One Frame Indicates that the maximum number of bytes defined by the communications mode have been transmitted because a NAK has been received from the receive unit and retransmit has been performed, or that transmission has not been completed because the message length value exceeds the maximum number of transmit bytes in one frame. This module sets this bit and enters the wait state. [Setting condition] • When the transmit has not been completed although the maximum number of bytes defined by the communications mode have been transmitted [Clearing condition] • When 1 is written

22.10 Disabling the Module

22.10.1 Transmitter and Receiver Idle

The transmitter or receiver modules can be disabled by writing 0 to the idle bit in the control register (TME for the transmitter and RME for the receiver). The idle state can be detected by polling the idle bit in the status register (TIS and RIS).

22.11 Compressed Mode Data

Compressed mode data is defined in the IEC 61937 specification. This module only detects compressed mode data. This is done by checking the parity flag (V flag) and bit 1 in the channel status data. If both are one then the data is in compressed mode. This is indicated by the setting of the CMD bit in the status register.

Note: Only the receiver detects compressed mode data since the information is not relevant to the transmitter.

22.12 References

IEC60958 Digital Audio Interface

IEC61937 Compressed Mode Digital Audio Interface

24.6 Definitions of A/D Conversion Accuracy

The A/D converter compares an analog value input from an analog input channel with its analog reference value and converts it to 10-bit digital data. The absolute accuracy of this A/D conversion is the deviation between the input analog value and the output digital value. It includes the following errors:

- Offset error
- Full-scale error
- Quantization error
- Nonlinearity error

These four error quantities are explained below with reference to figure 24.7. In the figure, the 10-bit A/D converter is illustrated as the 3-bit A/D converter for explanation. Offset error is the deviation between actual and ideal A/D conversion characteristics when the digital output value changes from the minimum (zero voltage) B'0000000000 (000 in the figure) to B'000000001 (001 in the figure)(figure 24.7, item (1)). Full-scale error is the deviation between actual and ideal A/D conversion characteristics when the digital output value changes from B'1111111110 (110 in the figure) to the maximum B'1111111111 (111 in the figure)(figure 24.7, item (2)). Quantization error is the intrinsic error of the A/D converter and is expressed as 1/2 LSB (figure 24.7, item (3)). Nonlinearity error is the deviation between actual and ideal A/D conversion characteristics between zero voltage and full-scale voltage (figure 24.7, item (4)). Note that it does not include offset, full-scale, or quantization error.

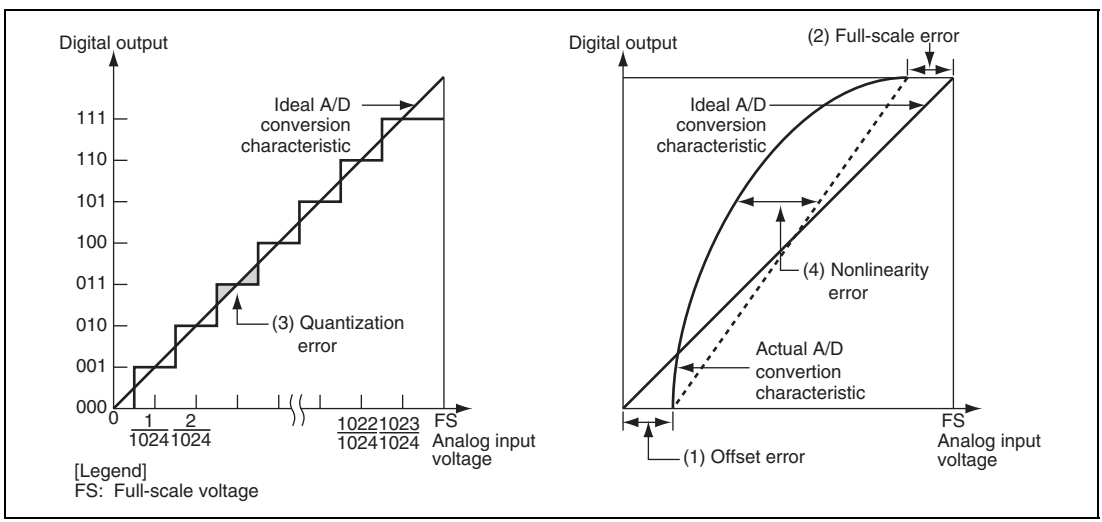


Figure 24.7 Definitions of A/D Conversion Accuracy

26.3.5 Test Mode Register (TESTMODE)

TESTMODE is a register that controls the USB test signal output during high-speed operation.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	UTST[3:0]	0000	R/W	Test Mode This module outputs the USB test signals during the high-speed operation, when these bits are written appropriate value. Table 26.6 shows test mode operation of this module.

- Ports

  Each page of the on-chip high-speed RAM has two independent read and write ports and is connected to the internal DMA bus (ID bus), CPU instruction fetch bus (F bus), and CPU memory access bus (M bus). (Note that the F bus is connected only to the read ports.)

  The F bus and M bus are used for access by the CPU, and the ID bus is used for access by the direct memory access controller.

  Each page of the on-chip large-capacity RAM has one read and write port and is connected to the internal CPU bus (IC bus), internal DMA bus (ID bus) and internal graphic buses 1 to 4 (IV1 to IV4). For 1-Mbyte version, pages 0 and 1 of the on-chip RAM for data retention are included in page 5 of the on-chip large-capacity RAM. Accordingly, pages 0 and 1 of the on-chip RAM for data retention are shared with the read and write port of page 5 of the on-chip large-capacity RAM. On the other hand, since the on-chip RAM for data retention is included in page 0 to 2 for 640-Kbyte version, it is shared with the read and write port of the same pages.

- Priority

  When the same page of the on-chip high-speed RAM is accessed from different buses simultaneously, the access is processed according to the priority. The priority is ID bus > M bus > F bus.

  When the same page of the on-chip large-capacity RAM is accessed from different buses simultaneously, the access is processed according to the priority. The priority is IV1 bus > IV2 bus > IV3 bus > IV4 bus > IC bus (when the IC bus does not have the bus mastership in the preceding bus cycle) > ID bus > IC bus (when the IC bus has the bus mastership in the preceding bus cycle)

- Number of access cycles

  On-chip high-speed RAM: the number of cycles for access to read or write from buses F and I is one cycle of Iϕ. Number of cycles for access from the ID bus depend on the ratio of the CPU clock (Iϕ) to the bus clock (Bϕ). Table 31.6 indicates number of cycles for access from the ID bus.

Section 33 Power-Down Modes

This LSI supports sleep mode, software standby mode, deep standby mode, and module standby mode. In power-down modes, functions of CPU, clocks, on-chip memory, or part of on-chip peripheral modules are halted or the power-supply is turned off, through which low power consumption is achieved. These modes are canceled by a reset or interrupt.

33.1 Features

33.1.1 Power-Down Modes

This LSI has the following power-down modes and function:

1. Sleep mode
2. Software standby mode
3. Deep standby mode
4. Module standby function

Table 33.1 shows the transition conditions for entering the modes from the program execution state, as well as the CPU and peripheral module states in each mode and the procedures for canceling each mode.

Item		Power Supply	Symbol	Typ.	Max.	Unit	Test Conditions
Current consumption in deep standby mode	Ta > 50 °C	Vcc+ PLLVcc+ USBAVcc+ USBDVcc+ USBUVcc	Idstby	7	57	μA	RAM 0 Kbytes retained, RTC_X1 selected
				8.5	64	μA	RAM 16 Kbytes retained, RTC_X1 selected
				19	113	μA	RAM 120 Kbytes retained, RTC_X1 selected
				23	127	μA	RAM 160 Kbytes retained, RTC_X1 selected
				37	197	μA	RAM 320 Kbytes retained, RTC_X1 selected
				14	65	μA	RAM 0 Kbytes retained, EXTAL selected
				15.5	72	μA	RAM 16 Kbytes retained, EXTAL selected
				26	121	μA	RAM 128 Kbytes retained, EXTAL selected
				30	135	μA	RAM 160 Kbytes retained, EXTAL selected
				44	205	μA	RAM 320 Kbytes retained, EXTAL selected
		PVcc+ AVcc+ Avref+ USBAPVcc+ USBDPVcc	PIdstby	1	11	μA	RTC is not operating
				3.5	21	μA	RTC_X1 selected
				1	—	mA	EXTAL selected, small gain*
		VBUS	VIdstby	6.5	7	μA	

2. After the chip has shifted to the power-on reset state from deep standby mode by the input on any of pins NMI, PC8 to PC5, PJ3, and PJ1, the pins retain the state until the IOKEEP bit in the deep standby cancel source flag register (DSFR) is cleared (see section 33, Power-Down Modes).
3. The EBUSKEEPE bit in deep standby control register (DSTCR) (see section 33, Power-Down Modes).
4. This LSI enters the power-on reset state for a certain period after recovery from deep standby control mode (see section 33, Power-Down Modes).
5. Depends on the setting of the RCKSEL bit in the realtime clock control register 5 (RCR5) (see section 14, Realtime Clock).
6. When pins for the connection with a crystal resonator are not used, the input pins (EXTAL, RTC_X1, AUDIO_X1, and USB_X1) must be fixed (pull-up/down resistor, power supply, or ground.) and the output pins (XTAL, RTC_X2, AUDIO_X2, and USB_X2) must be open.
7. Depends on the setting of the CKOEN bit in the frequency control register (FRQCR) of the clock pulse generator (see section 5, Clock Pulse Generator).
8. Depends on the setting of the AXTALE bit in the software reset control register (SWRSTCR) (see section 33, Power-Down Modes).
9. Depends on the setting of the HIZ bit in the standby control register 3 (STBCR3) (see section 33, Power-Down Modes).
10. Depends on the setting of the HIZMEM bit in the common control register (CMNCR) of the bus state controller (see section 9, Bus State Controller).
11. Depends on the setting of the HIZCNT bit in the common control register (CMNCR) of the bus state controller (see section 9, Bus State Controller).
12. Depends on the setting of the corresponding bit in the deep standby cancel source select register (DSSSR) (see section 33, Power-Down Modes).
13. Depends on the setting of the RTCEN bit in the realtime clock control register 2 (RCR2) (see section 14, Realtime Clock).
14. Z when the TAP controller of the user debugging interface is neither the Shift-DR nor Shift-IR state.
15. These are the pin states in product chip mode ($\overline{\text{ASEMD}}$ = H). See the Emulation Manual for the pin states in ASE mode ($\overline{\text{ASEMD}}$ = L).
16. When this is an output, the output is fixed to either the High or Low level. There is no oscillation.