Renesas Electronics America Inc - R5S72645P144FP#UZ Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	SH2A-FPU
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, I²C, SCI, SD, SIO, SPI, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	115
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LFQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5s72645p144fp-uz

Product Classification	Product Code		IEBus Controller	Controller Area Network	Operating Temperature	Package
SH7264 Group	R5S72640W144FPU	1 Mbyte*[1]	Not included	Not included	Regular specifications (-20 to +85 °C)	208-pin QFP
	R5S72641W144FPU		Not included	Included		
	R5S72642W144FPU		Included	Not included		
	R5S72643W144FPU		Included	Included		
	R5S72640P144FPU		Not included	Not included	Wide-range specifications (-40 to +85 °C)	
	R5S72641P144FPU		Not included	Included		
	R5S72642P144FPU		Included	Not included		
	R5S72643P144FPU		Included	Included		
	R5S72644W144FPU	640 Kbyte*[2]	Not included	Not included	Regular specifications (-20 to +85 °C)	
	R5S72645W144FPU		Not included	Included		
	R5S72646W144FPU		Included	Not included		
	R5S72647W144FPU		Included	Included		
	R5S72644P144FPU		Not included	Not included	Wide-range specifications (-40 to +85 °C)	
	R5S72645P144FPU		Not included	Included		
	R5S72646P144FPU		Included	Not included		
	R5S72647P144FPU		Included	Included		

Notes: 1. Hereinafter referred to as "1-Mbyte version" in this manual.
2. Hereinafter referred to as "640-Kbyte version" in this manual.

6.5.3 Interrupt Exception Handling

When an interrupt occurs, its priority level is ascertained by the interrupt controller. NMI is always accepted, but other interrupts are only accepted if they have a priority level higher than the priority level set in the interrupt mask level bits (I3 to I0) of the status register (SR).

When an interrupt is accepted, interrupt exception handling begins. In interrupt exception handling, the CPU fetches the exception service routine start address which corresponds to the accepted interrupt from the exception handling vector table, and saves SR and the program counter (PC) to the stack. In the case of interrupt exception handling other than NMI with usage of the register banks enabled, general registers R0 to R14, control register GBR, system registers MACH, MACL, and PR, and the vector table address offset of the interrupt exception handling to be executed are saved in the register banks. In the case of exception handling due to an address error, NMI interrupt, or instruction, saving is not performed to the register banks. If saving has been performed to all register banks (0 to 14), automatic saving to the stack is performed instead of register bank saving. In this case, an interrupt controller setting must have been made so that register bank overflow exceptions are not accepted (the BOVE bit in IBNR of the interrupt controller is 0). If a setting to accept register bank overflow exceptions has been made (the BOVE bit in IBNR of the interrupt controller is 1), register bank overflow exception occurs. Next, the priority level value of the accepted interrupt is written to the I3 to I0 bits in SR. For NMI, however, the priority level is 16, but the value set in the I3 to I0 bits is H'F (level 15). Then, after jumping to the start address fetched from the exception handling vector table, program execution starts. The jump that occurs is not a delayed branch. See section 7.6, Operation, for further details of interrupt exception handling.

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Interrupt priority register 18	IPR18	R/W	H'0000	H'FFFE0C18	16, 32
Interrupt priority register 19	IPR19	R/W	H'0000	H'FFFE0C1A	16, 32
Interrupt priority register 20	IPR20	R/W	H'0000	H'FFFE0C1C	16, 32
Interrupt priority register 21	IPR21	R/W	H'0000	H'FFFE0C1E	16, 32
Interrupt priority register 22	IPR22	R/W	H'0000	H'FFFE0C20	16, 32

Notes: 1. For 1-Mbyte version, when the NMI pin is high, becomes H'8000; when low, becomes H'0000. For 640-Kbyte version, when the pin is high, becomes H'8001; when low, becomes H'0001.
2. Only 0 can be written after reading 1, to clear the flag.

(b) Free-Running Count Operation and Periodic Count Operation:

Immediately after a reset, the TCNT counters of this module are all designated as free-running counters. When the relevant bit in TSTR is set to 1 the corresponding TCNT counter starts up-count operation as a free-running counter. When TCNT overflows (from H'FFFF to H'0000), the TCFV bit in TSR is set to 1. If the value of the corresponding TCIEV bit in TIER is 1 at this point, this module requests an interrupt. After overflow, TCNT starts counting up again from H'0000.

Figure 11.5 illustrates free-running counter operation.

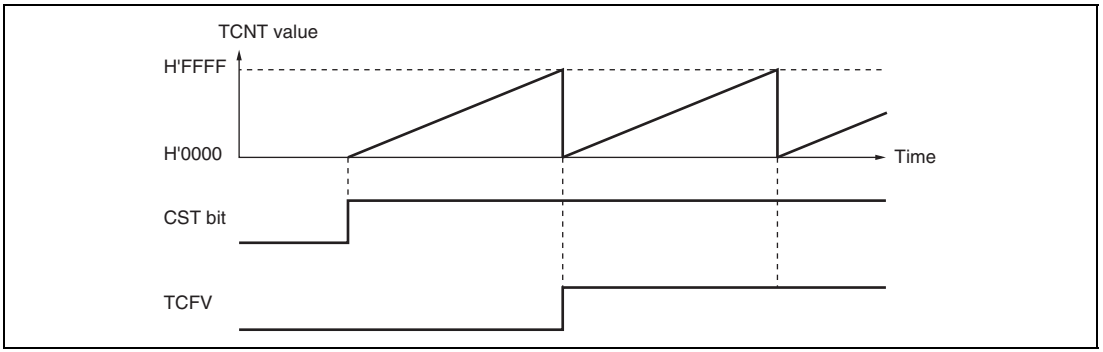


Figure 11.5 Free-Running Counter Operation

When compare match is selected as the TCNT clearing source, the TCNT counter for the relevant channel performs periodic count operation. The TGR register for setting the period is designated as an output compare register, and counter clearing by compare match is selected by means of bits CCLR0 to CCLR2 in TCR. After the settings have been made, TCNT starts up-count operation as a periodic counter when the corresponding bit in TSTR is set to 1. When the count value matches the value in TGR, the TGF bit in TSR is set to 1 and TCNT is cleared to H'0000.

If the value of the corresponding TGIE bit in TIER is 1 at this point, this module requests an interrupt. After a compare match, TCNT starts counting up again from H'0000.

11.7.15 Reset Sync PWM Mode Buffer Operation and Compare Match Flag

When setting buffer operation for reset sync PWM mode, set the BFA and BFB bits of TMDR_4 to 0. The TIOC4C pin will be unable to produce its waveform output if the BFA bit of TMDR_4 is set to 1.

In reset sync PWM mode, the channel 3 and channel 4 buffers operate in accordance with the BFA and BFB bit settings of TMDR_3. For example, if the BFA bit of TMDR_3 is set to 1, TGRC_3 functions as the buffer register for TGRA_3. At the same time, TGRC_4 functions as the buffer register for TGRA_4.

The TGFC bit and TGFD bit of TSR_3 and TSR_4 are not set when TGRC_3 and TGRD_3 are operating as buffer registers.

Figure 11.109 shows an example of operations for TGR_3, TGR_4, TIOC3, and TIOC4, with TMDR_3's BFA and BFB bits set to 1, and TMDR_4's BFA and BFB bits set to 0.

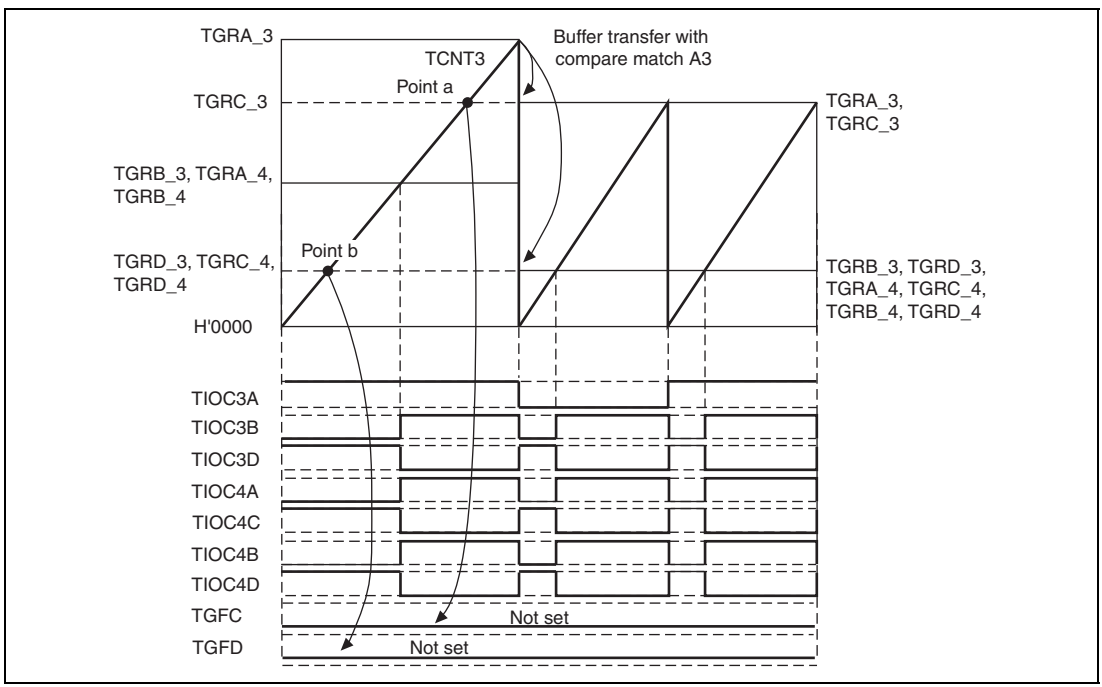


Figure 11.109 Buffer Operation and Compare-Match Flags in Reset Synchronous PWM Mode

Section 19 Serial I/O with FIFO

This LSI includes a clock-synchronized serial I/O module with FIFO.

19.1 Features

- Serial transfer
  - 16-stage 32-bit FIFOs (independent transmission and reception)
  - Supports 8-bit monaural/16-bit monaural/16-bit stereo audio input and output
  - MSB first for data transmission
  - Supports a maximum of 48-kHz sampling rate
  - Synchronization by frame synchronization pulse
  - Connectable to linear, audio, or A-Law or μ-Law CODEC chip
  - Supports both master and slave modes
- Serial clock
  - AUDIO_CLK or AUDIO_X1 can be selected as the clock source.
- Interrupts: One type
- DMA transfer: Two types
  - Transmit FIFO transfer requests and receive FIFO transfer requests

Table 19.8 Conditions to Issue Transmit Request

TFWM2 to TFWM0	Number of Requested Stages	Transmit Request Issued	Used Areas
000	1	There are sixteen stages of empty area.	Smallest
100	4	There are twelve or more stages of empty area.	↕
101	8	There are eight or more stages of empty area.	
110	12	There are four or more stages of empty area.	
111	16	There is one or more stage of empty area.	Largest

Table 19.9 Conditions to Issue Receive Request

RFWM2 to RFWM0	Number of Requested Stages	Receive Request Issued	Used Areas
000	1	There is one or more stage of valid data.	Smallest
100	4	There are four stages of valid data or more.	↕
101	8	There are eight stages of valid data or more.	
110	12	There are twelve stages of valid data or more.	
111	16	There are sixteen stages of valid data.	Largest

The number of stages of the FIFO is sixteen. Accordingly, an overflow error or underflow error occurs if data area or empty area exceeds sixteen FIFO stages. The transfer request is canceled when the above condition is not satisfied even if the FIFO is not empty or full.

(3) Number of FIFOs

The usage state of the transmit FIFO and receive FIFO are indicated by the TFUA and FRUA bits in the FIFO control register as below:

- Transmit FIFO: The number of empty FIFO stages is indicated by the TFUA4 to TFUA0 bits in SIFCTR.
- Receive FIFO: The number of valid data stages is indicated by the RFUA4 to RFUA0 bits in SIFCTR.

The above register contents indicate the possible data numbers that can be transferred by the CPU or direct memory access controller.

(4) Reception in Slave Mode

Figure 19.9 shows an example of reception settings and operation when this module is used as a slave.

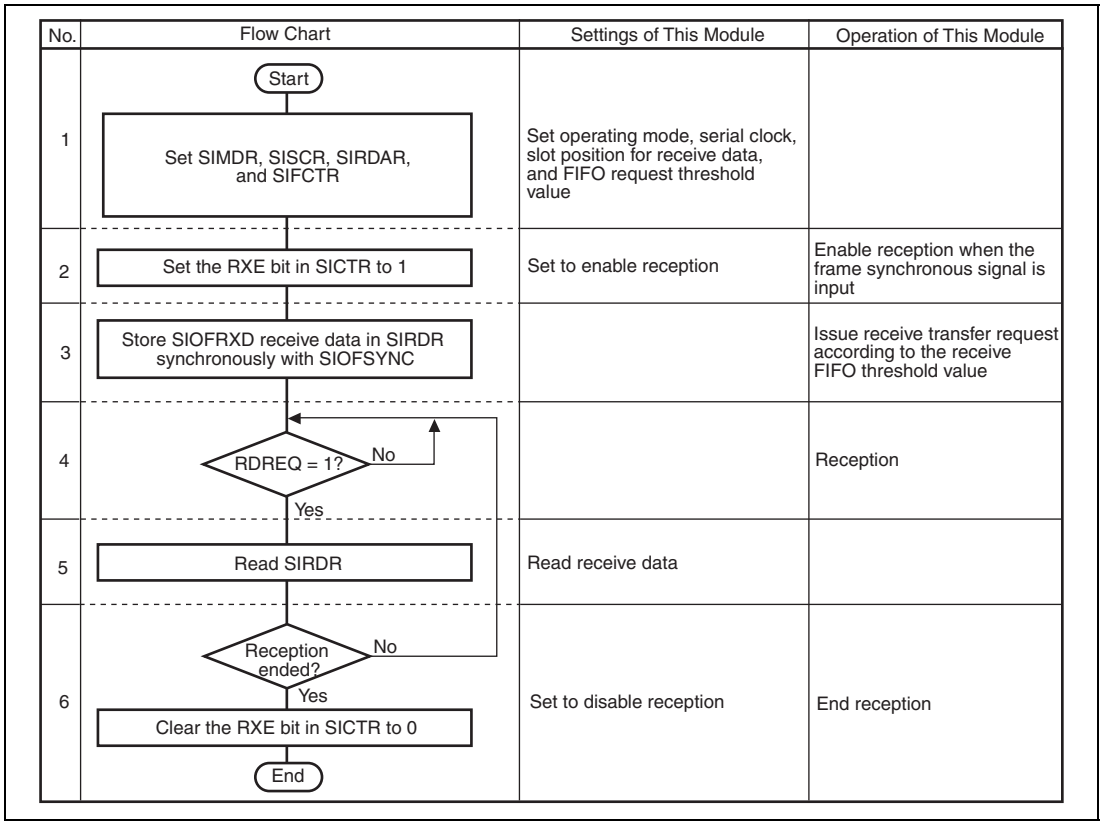


Figure 19.9 Example of Receive Operation in Slave Mode

20.8 Setting I/O Ports

The I/O ports for this module must be specified before or during the configuration mode. For details on the settings of I/O ports, see section 32, General Purpose I/O Ports. Two methods are available using two channels of this module in this LSI.

- Using this module as a 2-channel module (channels 0 and 1)
  Each channel has 32 Mailboxes.
- Using this module as a 1-channel module (channels 0 and 1 functioning as a single channel)

When the second method is used, see section 20.9.1, Notes on Port Setting for Multiple Channels Used as Single Channel.

Figures 20.28 and 20.29 show connection examples for individual port settings.

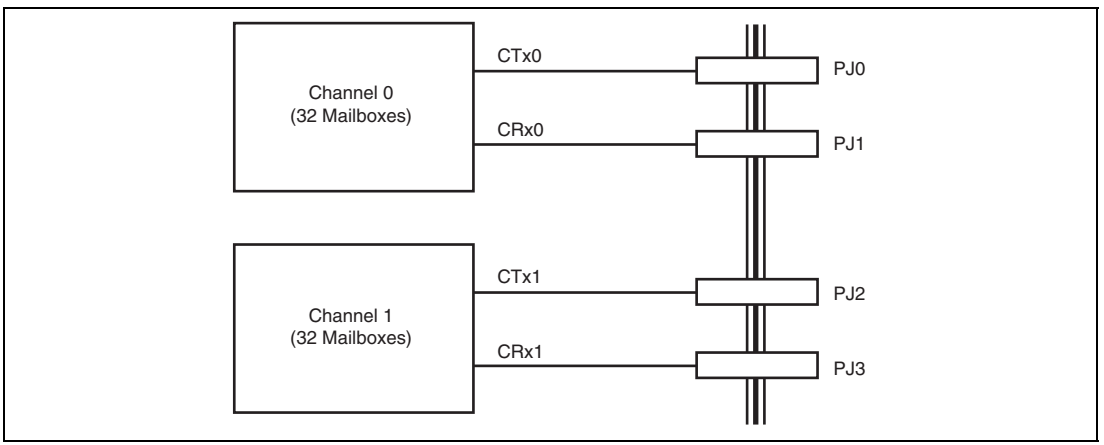
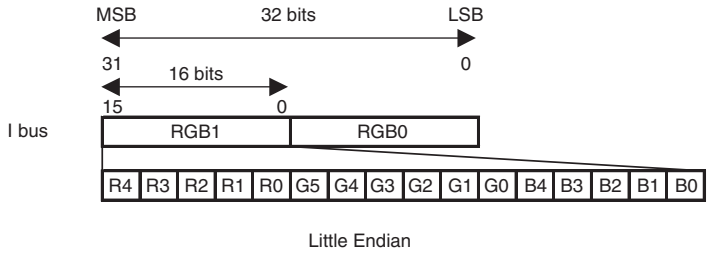


Figure 20.28 Connection Example when Using This Module as 2-Channel Module (32 Mailboxes × 2 Channels)

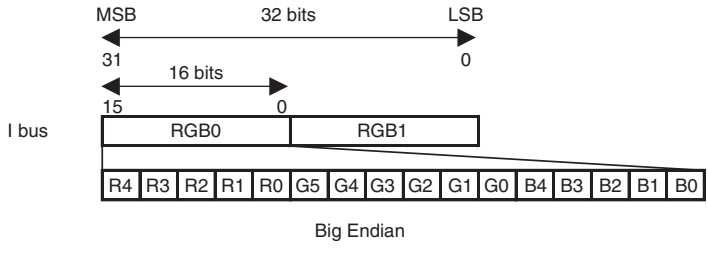
Bit	Bit Name	Initial Value	R/W	Description
23 to 20	CHNO[3:0]	All 0	W	Channel Number 0000: Don't care 0001: A (left channel) 0010: B (right channel) 0011: C
19 to 16	SRCNO[3:0]	All 0	W	Source Number 0000: Don't care 0001: 1 0010: 2 0011: 3
15 to 8	CATCD[7:0]	All 0	W	Category Code (Example) 00000000: 2-channel general format 00000001: 2-channel compact disc (IEC 908) 00000010: 2-channel PCM encoder/decoder 00000011: 2-channel digital audio tape recorder
7, 6	—	All 0	W	Reserved The write value should always be 0.
5 to 1	CTL[4:0]	All 0	W	Control The control bits are copied from the source (see IEC60958 standard).
0	—	0	W	Reserved The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	DBLB	0	R/W	Double Buffer Mode Selects either single or double buffer mode for the FIFO buffer used by the selected pipe. 0: Single buffer 1: Double buffer This bit is valid when PIPE1 to PIPE5 are selected. When this bit has been set to 1, this module assigns two planes of the FIFO buffer size specified by the BUFSIZE bits in PIPEBUF to the selected pipe. Specifically, the following expression determines the FIFO buffer size assigned to the selected pipe by this module. (BUFSIZE + 1) × 64 × (DBLB + 1) [bytes] Modify these bits while CSSTS is 0 and PID is NAK and before the pipe is selected by the CURPIPE bits. To modify these bits after completing USB communication using the selected pipe, write 1 and then 0 to ACLRM continuously to clear the FIFO buffer assigned to the selected pipe while the CSSTS, PID, and CURPIPE bits are in the above-described state. Before modifying these bits after modifying the PID bits for the selected pipe from BUF to NAK, check that CSSTS and PBUSY are 0. However, if the PID bits have been modified to NAK by this module, checking PBUSY is not necessary.

Bit	Bit Name	Initial Value	R/W	Description
13	CSCLR	0	R/W*	C-SPLIT Status Clear Bit When the host controller function is selected, setting this bit to 1 allows this module to clear the CSSTS bit to 0. 0: Writing invalid 1: Clears the CSSTS bit to 0. For the transfer using the split transaction, to restart the next transfer with the S-SPLIT forcibly, set this bit to 1. However, for the normal split transaction, this module automatically clears the CSSTS bit to 0 upon completion of the C-SPLIT; therefore, clearing the CSSTS bit is not necessary. Controlling the CSSTS bit through this bit must be done while UACT is 0 and thus communication is halted or while no transfer is being performed with bus disconnection detected. Setting this bit to 1 while CSSTS is 0 has no effect. When the function controller function is selected, be sure to write 0 to this bit.
12	CSSTS	0	R	CSSTS Status Bit Indicates the C-SPLIT status of the split transaction when the host controller function is selected. 0: START-SPLIT (S-SPLIT) transaction being processed or the transfer not using the split transaction in progress 1: C-SPLIT transaction being processed This module sets this bit to 1 upon start of the C-SPLIT and clears this bit to 0 upon detection of C-SPLIT completion. If the USB device is detached when processing of a C-SPLIT transaction is in progress, the CSSTS bit may remain set to 1. In such a case (DTCH = 1 detected), use the CSCLR bit to clear the CSSTS bit to 0. Indicates the valid value only when the host controller function is selected.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.



Little Endian



Big Endian

Note: The image is displayed in the order of pixels (RGB0 -> RGB1) from left to right.

Figure 27.15 Description of Endian

32.2.30 Port J Control Register 0 to 2 (PJCR0 to PJCR2)

PJCR2 to PJCR0 are 16-bit readable/writable registers that are used to select the functions of the multiplexed pins on port J.

(1) Port J Control Register 2 (PJCR2: Available Only in the SH7264 Group)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	PJ11MD[1:0]		-	-	PJ10MD[1:0]		-	-	PJ9MD[1:0]		-	-	PJ8MD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	PJ11MD[1:0]	00	R/W	PJ11 Mode Select the function of the PJ11. 00: PJ11 10: DACK1 01: PWM2H 11: Setting prohibited
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PJ10MD[1:0]	00	R/W	PJ10 Mode Select the function of the PJ10. 00: PJ10 10: DREQ1 01: PWM2G 11: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	PJ9MD[1:0]	00	R/W	PJ9 Mode Select the function of the PJ9. 00: PJ9 10: TEND1 01: PWM2F 11: AUDIO_XOUT (640-Kbyte version only)
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

33.3.3 Software Standby Mode Application Example

This example describes a transition to software standby mode on the falling edge of the NMI signal, and cancellation on the rising edge of the NMI signal. The timing is shown in figure 33.1.

When the NMI pin is changed from high to low level while the NMI edge select bit (NMIE) in the interrupt control register 0 (ICR0) is set to 0 (falling edge detection), the NMI interrupt is accepted. When the NMIE bit is set to 1 (rising edge detection) by the NMI exception service routine, the STBY and DEEP bits in STBCR1 are set to 1 and 0 respectively, and a SLEEP instruction is executed, software standby mode is entered. Thereafter, software standby mode is canceled when the NMI pin is changed from low to high level.

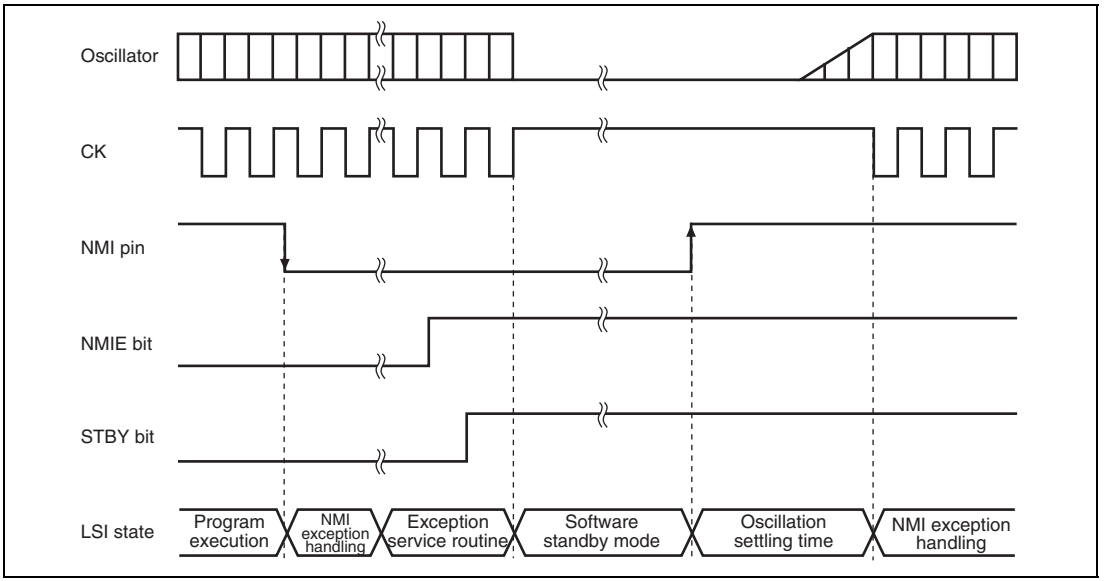


Figure 33.1 NMI Timing in Software Standby Mode (Application Example)

35.5 Operation

35.5.1 PWM Operation

PWM waveforms are output from pins PWM1A to PWM1H and PWM2A to PWM2H as shown in figure 35.7.

(1) Initial Settings

Set the PWM output polarity in PWPR_n; select the clock to be input to PWCNT_n with the CKS2 to CKS0 bits in PWCRn; set the PWM conversion cycle in PWCYR_n; and set the first frame of data in PWBFR_nA, PWBFR_nC, PWBFR_nE, and PWBFR_nG.

(2) Activation

When the CST bit in PWCR_n is set to 1, PWCNT_n starts counting up. On compare match between PWCNT_n and PWCYR_n, data is transferred from the buffer register to the duty register and the CMF bit in PWCR_n is set to 1. At the same time, if the IE bit in PWCR_n has been set to 1, an interrupt can be requested or the direct memory access controller can be activated.

(3) Waveform Output

The PWM outputs selected by the OTS bits in PWDTR_nA, PWDTR_nC, PWDTR_nE, and PWDTR_nG go high when a compare match occurs between PWCNT_n and PWCYR_n. The PWM outputs not selected by the OTS bit are low. When a compare match occurs between PWCNT_n and PWDTR_nA, PWDTR_nC, PWDTR_nE, or PWDTR_nG, the corresponding PWM output goes low. If the corresponding bit in PWPR_n is set to 1, the output is inverted.

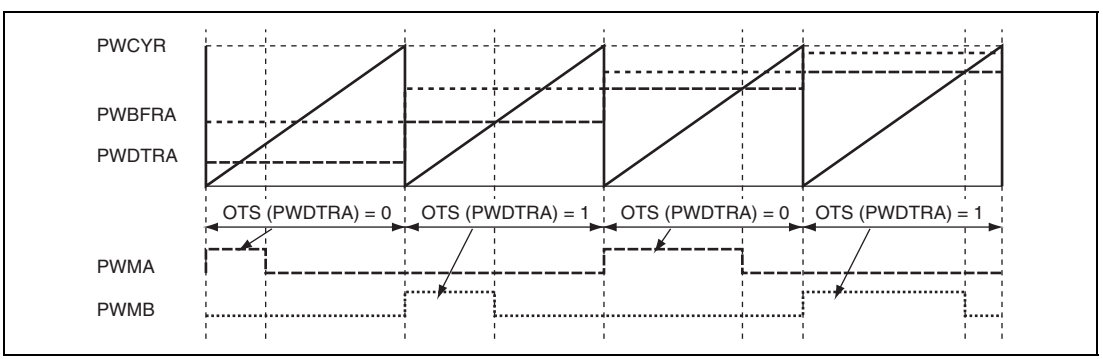


Figure 35.7 PWM Operation

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
I²C bus interface 3	I²C bus interrupt enable register_2	ICIER_2	8	H'FFFEE803	8
	I²C bus status register_2	ICSR_2	8	H'FFFEE804	8
	Slave address register_2	SAR_2	8	H'FFFEE805	8
	I²C bus transmit data register_2	ICDRT_2	8	H'FFFEE806	8
	I²C bus receive data register_2	ICDRR_2	8	H'FFFEE807	8
	NF2CYC register_2	NF2CYC_2	8	H'FFFEE808	8
Serial sound interface	Control register_0	SSICR_0	32	H'FFFF0000	8, 16, 32
	Status register_0	SSISR_0	32	H'FFFF0004	8, 16, 32
	FIFO control register_0	SSIFCR_0	32	H'FFFF0010	8, 16, 32
	FIFO status register_0	SSIFSR_0	32	H'FFFF0014	8, 16, 32
	Transmit FIFO data register 0	SSIFTDR_0	32	H'FFFF0018	32
	Receive FIFO data register 0	SSIFRDR_0	32	H'FFFF001C	8, 16, 32
	Control register_1	SSICR_1	32	H'FFFF0800	8, 16, 32
	Status register_1	SSISR_1	32	H'FFFF0804	8, 16, 32
	FIFO control register_1	SSIFCR_1	32	H'FFFF0810	8, 16, 32
	FIFO status register_1	SSIFSR_1	32	H'FFFF0814	8, 16, 32
	Transmit FIFO data register 1	SSIFTDR_1	32	H'FFFF0818	32
	Receive FIFO data register 1	SSIFRDR_1	32	H'FFFF081C	32
	Control register_2	SSICR_2	32	H'FFFF1000	8, 16, 32
	Status register_2	SSISR_2	32	H'FFFF1004	8, 16, 32
	FIFO control register_2	SSIFCR_2	32	H'FFFF1010	8, 16, 32
	FIFO status register_2	SSIFSR_2	32	H'FFFF1014	8, 16, 32
	Transmit FIFO data register 2	SSIFTDR_2	32	H'FFFF1018	32
	Receive FIFO data register 2	SSIFRDR_2	32	H'FFFF101C	32
	Control register_3	SSICR_3	32	H'FFFF1800	8, 16, 32
	Status register_3	SSISR_3	32	H'FFFF1804	8, 16, 32
	FIFO control register_3	SSIFCR_3	32	H'FFFF1810	8, 16, 32
	FIFO status register_3	SSIFSR_3	32	H'FFFF1814	8, 16, 32
	Transmit FIFO data register 3	SSIFTDR_3	32	H'FFFF1818	32
	Receive FIFO data register 3	SSIFRDR_3	32	H'FFFF181C	32

Module Name	Register Name	Abbreviation	Number of Bits	Address	Access Size
CD-ROM decoder	Pre-ECC correction subheader: channel number (byte 17) data register	SHEAD01	8	H'FFFF901D	8
	Pre-ECC correction subheader: sub-mode (byte 18) data register	SHEAD02	8	H'FFFF901E	8
	Pre-ECC correction subheader: data type (byte 19) data register	SHEAD03	8	H'FFFF901F	8
	Pre-ECC correction subheader: file number (byte 20) data register	SHEAD04	8	H'FFFF9020	8
	Pre-ECC correction subheader: channel number (byte 21) data register	SHEAD05	8	H'FFFF9021	8
	Pre-ECC correction subheader: sub-mode (byte 22) data register	SHEAD06	8	H'FFFF9022	8
	Pre-ECC correction subheader: data type (byte 23) data register	SHEAD07	8	H'FFFF9023	8
	Post-ECC correction header: minutes data register	HEAD20	8	H'FFFF9024	8
	Post-ECC correction header: seconds data register	HEAD21	8	H'FFFF9025	8
	Post-ECC correction header: frames (1/75 second) data register	HEAD22	8	H'FFFF9026	8
	Post-ECC correction header: mode data register	HEAD23	8	H'FFFF9027	8
	Post-ECC correction subheader: file number (byte 16) data register	SHEAD20	8	H'FFFF9028	8
	Post-ECC correction subheader: channel number (byte 17) data register	SHEAD21	8	H'FFFF9029	8
	Post-ECC correction subheader: sub-mode (byte 18) data register	SHEAD22	8	H'FFFF902A	8
	Post-ECC correction subheader: data type (byte 19) data register	SHEAD23	8	H'FFFF902B	8
	Post-ECC correction subheader: file number (byte 20) data register	SHEAD24	8	H'FFFF902C	8
	Post-ECC correction subheader: channel number (byte 21) data register	SHEAD25	8	H'FFFF902D	8

Module Name	Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
Video display controller 3	VIDEO_FIELD_OFFSET	VIDEO_FIELD_OFFSET [31]	VIDEO_FIELD_OFFSET [30]	VIDEO_FIELD_OFFSET [29]	VIDEO_FIELD_OFFSET [28]	VIDEO_FIELD_OFFSET [27]	VIDEO_FIELD_OFFSET [26]	VIDEO_FIELD_OFFSET [25]	VIDEO_FIELD_OFFSET [24]
		VIDEO_FIELD_OFFSET [23]	VIDEO_FIELD_OFFSET [22]	VIDEO_FIELD_OFFSET [21]	VIDEO_FIELD_OFFSET [20]	VIDEO_FIELD_OFFSET [19]	VIDEO_FIELD_OFFSET [18]	VIDEO_FIELD_OFFSET [17]	VIDEO_FIELD_OFFSET [16]
		VIDEO_FIELD_OFFSET [15]	VIDEO_FIELD_OFFSET [14]	VIDEO_FIELD_OFFSET [13]	VIDEO_FIELD_OFFSET [12]	VIDEO_FIELD_OFFSET [11]	VIDEO_FIELD_OFFSET [10]	VIDEO_FIELD_OFFSET[9]	VIDEO_FIELD_OFFSET[8]
		VIDEO_FIELD_OFFSET[7]	VIDEO_FIELD_OFFSET[6]	VIDEO_FIELD_OFFSET[5]	VIDEO_FIELD_OFFSET[4]	VIDEO_FIELD_OFFSET[3]	VIDEO_FIELD_OFFSET[2]	VIDEO_FIELD_OFFSET[1]	VIDEO_FIELD_OFFSET[0]
	VIDEO_LINE BUFF_NUM	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	VIDEO_LINE BUFF_NUM [8]
		VIDEO_LINE BUFF_NUM [7]	VIDEO_LINE BUFF_NUM [6]	VIDEO_LINE BUFF_NUM [5]	VIDEO_LINE BUFF_NUM [4]	VIDEO_LINE BUFF_NUM [3]	VIDEO_LINE BUFF_NUM [2]	VIDEO_LINE BUFF_NUM [1]	VIDEO_LINE BUFF_NUM [0]
	VIDEO_DISP_SIZE	—	—	—	—	—	—	—	VIDEO_DISP_HEIGHT[8]
		VIDEO_DISP_HEIGHT[7]	VIDEO_DISP_HEIGHT[6]	VIDEO_DISP_HEIGHT[5]	VIDEO_DISP_HEIGHT[4]	VIDEO_DISP_HEIGHT[3]	VIDEO_DISP_HEIGHT[2]	VIDEO_DISP_HEIGHT[1]	VIDEO_DISP_HEIGHT[0]
		—	—	—	—	—	—	VIDEO_DISP_WIDTH[9]	VIDEO_DISP_WIDTH[8]
		VIDEO_DISP_WIDTH[7]	VIDEO_DISP_WIDTH[6]	VIDEO_DISP_WIDTH[5]	VIDEO_DISP_WIDTH[4]	VIDEO_DISP_WIDTH[3]	VIDEO_DISP_WIDTH[2]	VIDEO_DISP_WIDTH[1]	VIDEO_DISP_WIDTH[0]
	VIDEO_DISP_HSTART	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—
		—	—	—	—	—	—	VIDEO_DISP_HSTART[9]	VIDEO_DISP_HSTART[8]
		VIDEO_DISP_HSTART[7]	VIDEO_DISP_HSTART[6]	VIDEO_DISP_HSTART[5]	VIDEO_DISP_HSTART[4]	VIDEO_DISP_HSTART[3]	VIDEO_DISP_HSTART[2]	VIDEO_DISP_HSTART[1]	VIDEO_DISP_HSTART[0]

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