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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052c8t6d

Table 2. Ultra-low-power STM32L052x6/x8 device features and peripheral counts (continued)

Peripheral	STM32L052T6	STM32L052K6	STM32L052C6	STM32L052R6	STM32L052T8	STM32L052K8	STM32L052C8	STM32L052R8
Operating temperatures	Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C							
Packages	WLCSP36	LQFP32, UFQFPN32	LQFP48	LQFP64 TFBGA64	WLCSP36	LQFP32, UFQFPN32	LQFP48	LQFP64 TFBGA64

1. 2 SPI interfaces are USARTs operating in SPI master mode.
2. LQFP32 has two GPIOs, less than UFQFPN32 (27).
3. TFBGA64 has one GPIO, one ADC input and one capacitive sensing channel less than LQFP64.

- **Stop mode without RTC**

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are disabled.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB/USART/I2C/LPUART/LPTIMER wakeup events.

- **Standby mode with RTC**

  The Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSE crystal and HSI RC oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby mode without RTC**

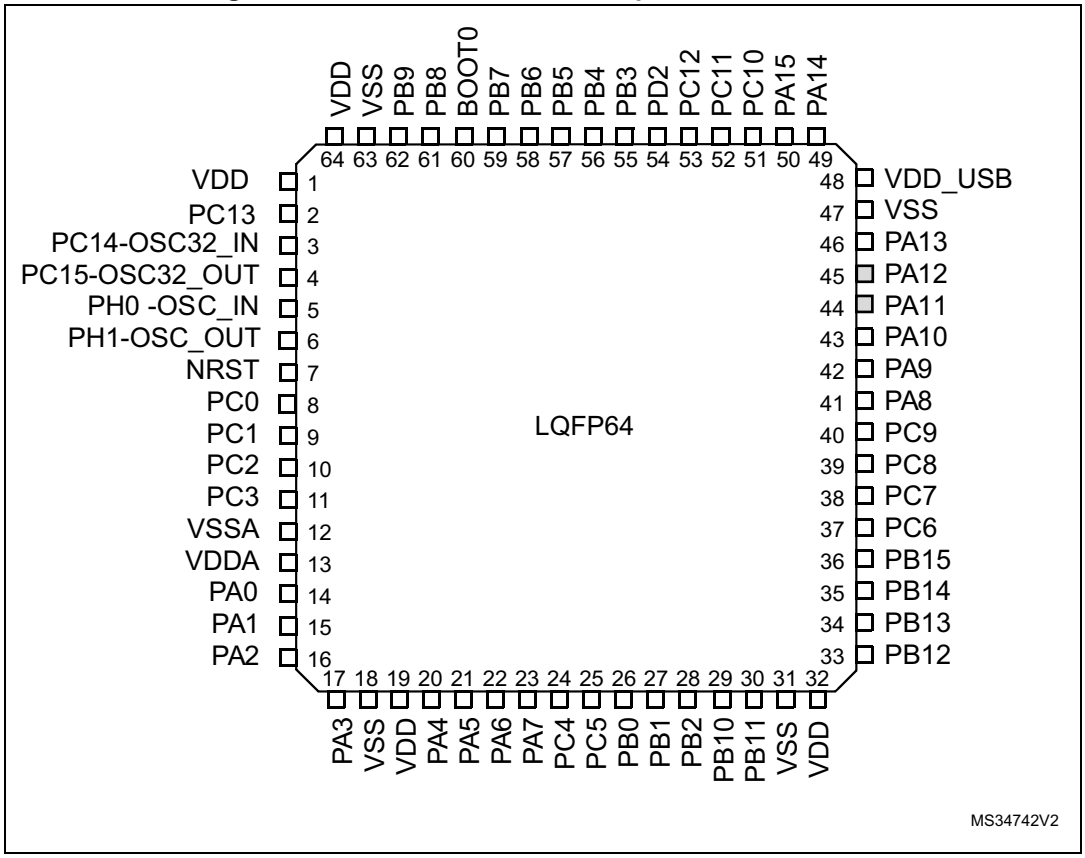
  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32 KHz oscillator, RCC_CSR register).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

4 Pin descriptions

Figure 3. STM32L052x6/8 LQFP64 pinout - 10 x 10 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36[1]	LQFP48	LQFP64	TFBGA64						
-	-	E2	21	29	G7	PB10	I/O	FT	-	TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL	-
-	-	D2	22	30	H7	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA	-
16	-	-	23	31	D6	VSS	S	-	-	-	-
17	17	F1	24	32	E5	VDD	S	-	-	-	-
-	-	-	25	33	H8	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	-
-	-	-	26	34	G8	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
-	-	-	27	35	F8	PB14	I/O	FTf	-	SPI2_MISO/I 2S2_MCK, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
-	-	-	28	36	F7	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, RTC_REFIN	-
-	-	-	-	37	F6	PC6	I/O	FT	-	TIM22_CH1, TSC_G8_IO1	-
-	-	-	-	38	E7	PC7	I/O	FT	-	TIM22_CH2, TSC_G8_IO2	-
-	-	-	-	39	E8	PC8	I/O	FT	-	TIM22_ETR, TSC_G8_IO3	-

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36[1]	LQFP48	LQFP64	TFBGA64						
-	-	-	-	54	B5	PD2	I/O	FT	-	LPUART1_RTS_DE	-
26	26	B3	39	55	A5	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, TSC_G5I_O1, EVENTOUT	COMP2_INN
27	27	A3	40	56	A4	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TSC_G5_IO2, TIM22_CH1	COMP2_INP
28	28	C4	41	57	C4	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
29	29	B4	42	58	D3	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
30	30	A4	43	59	C3	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4	COMP2_INP, PVD_IN
31	31	C5	44	60	B4	BOOT0	B	-	-	-	-
-	32	B5	45	61	B3	PB8	I/O	FTf	-	TSC_SYNC, I2C1_SCL	-
-	-	-	46	62	A3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
32	-	D6	47	63	D4	VSS	S	-	-	-	-
1	1	A5	48	64	E4	VDD	S	-	-	-	-

1. PB9/12/13/14/15, PH0/1 and PC13 GPIOs should be configured as output and driven Low, even if they are not available on this package.
2. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.
3. These pins are powered by VDD_USB. For all characteristics that refer to V_{DD}, V_{DD_USB} must be used instead.

Table 31. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	135	170	µA
				2 MHz	240	270	
				4 MHz	450	480	
			Range 2, V_{CORE}=1.5 ,V, VOS[1:0]=10	4 MHz	0.52	0.6	mA
				8 MHz	1	1.2	
				16 MHz	2	2.3	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4	
				16 MHz	2.45	2.8	
				32 MHz	5.1	5.4	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	34.5	75	µA
				524 kHz	83	120	
				4.2 MHz	485	540	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	2.1	2.3	mA
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	5.1	5.6	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 32. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	450	µA
				CoreMark		575	
				Fibonacci		370	
				while(1)		340	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	5.1	mA
				CoreMark		6.25	
				Fibonacci		4.4	
				while(1)		4.7	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Figure 16. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

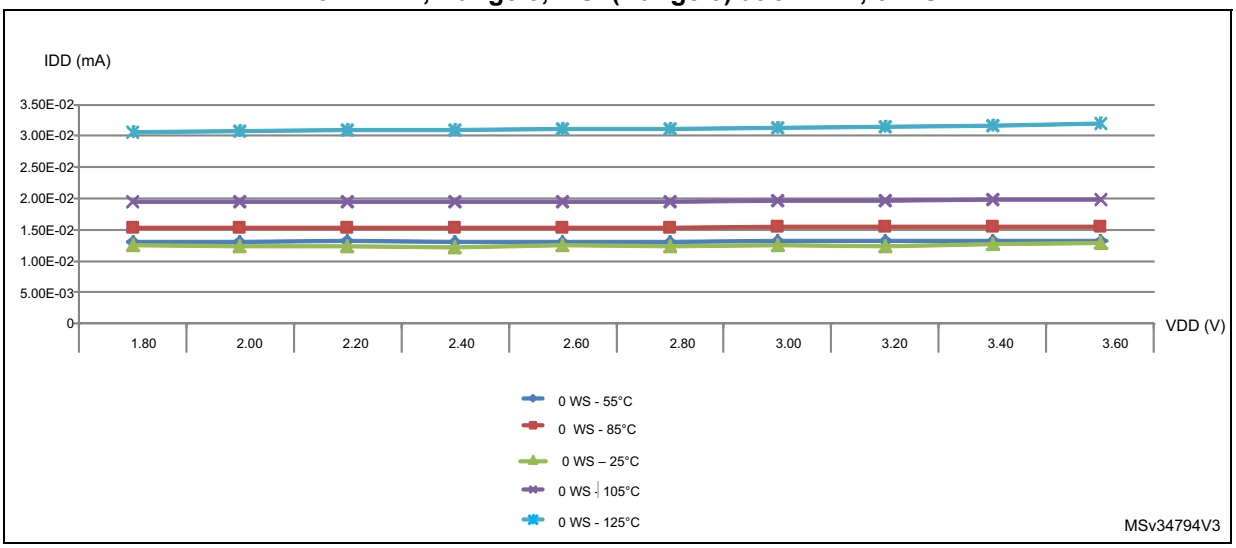


Table 35. Current consumption in Low-power sleep mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK} = 32 kHz, Flash OFF	T_A = − 40 to 25°C	4.7(2)	-	µA
			MSI clock = 65 kHz, f_{HCLK} = 32 kHz, Flash ON	T_A = − 40 to 25°C	17	23	
				T_A = 85 °C	19.5	63	
				T_A = 105 °C	23	69	
				T_A = 125 °C	32.5	90	
			MSI clock =65 kHz, f_{HCLK} = 65 kHz, Flash ON	T_A = − 40 to 25°C	17	23	
				T_A = 85 °C	20	63	
				T_A = 105 °C	23.5	69	
				T_A = 125 °C	32.5	90	
			MSI clock = 131 kHz, f_{HCLK} = 131 kHz, Flash ON	T_A = − 40 to 25°C	19.5	36	
				T_A = 55 °C	20.5	64	
				T_A = 85 °C	22.5	66	
				T_A = 105 °C	26	72	
				T_A = 125 °C	35	95	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. As the CPU is in Sleep mode, the difference between the current consumption with Flash ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

Table 40. Peripheral current consumption in Stop and Standby mode(1)

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	µA
I_{REFINT}	-	-	1.4	
-	LSE Low drive(2)	0,1	0,1	
-	LPTIM1, Input 100 Hz	0,01	0,01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0,2	0,2	
-	RTC	0,3	0,48	

1. LPTIM peripheral cannot operate in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

Table 41. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	7	8	Number of clock cycles
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash memory enabled	7	8	
		f_{HCLK} = 262 kHz Flash memory switched OFF	9	10	

Low-speed external user clock generated from an external source

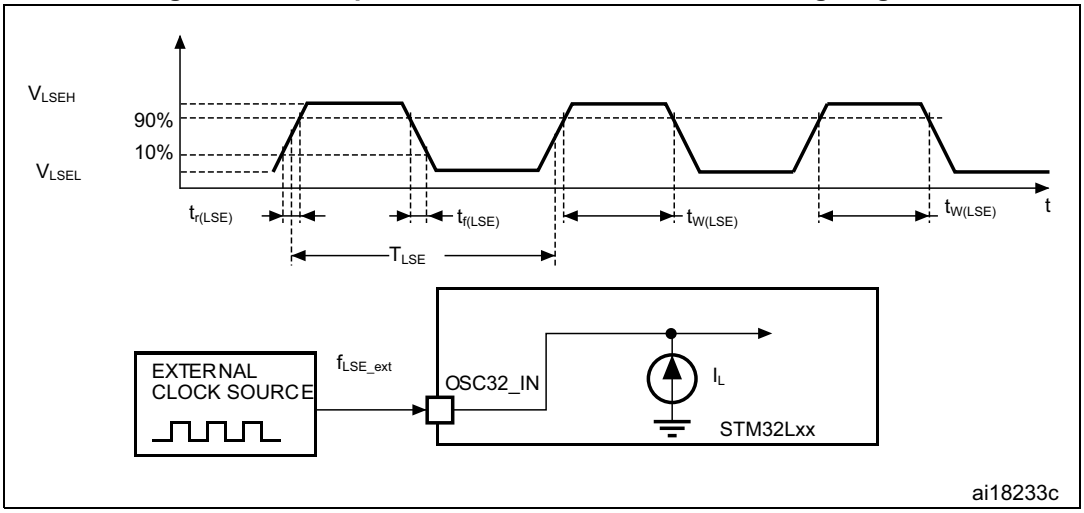
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 25*.

Table 43. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 20. Low-speed external clock source AC timing diagram



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

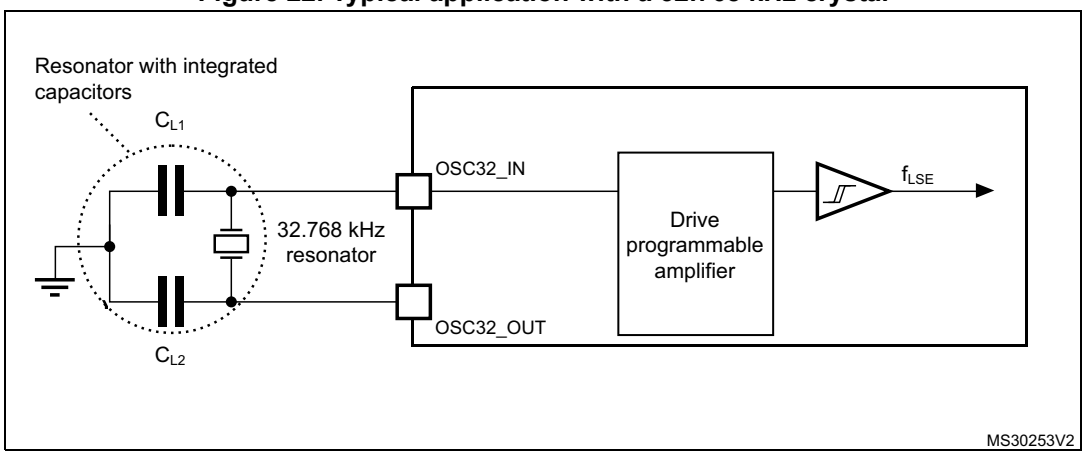
Table 45. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min(2)	Typ	Max	Unit
f_{LSE}	LSE oscillator frequency		-	32.768	-	kHz
G_m	Maximum critical crystal transconductance	LSEDRV[1:0]=00 lower driving capability	-	-	0.5	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	-	-	0.75	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.7	
		LSEDRV[1:0]=11 higher driving capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. Guaranteed by characterization results. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer. To increase speed, address a lower-drive quartz with a high- driver mode.

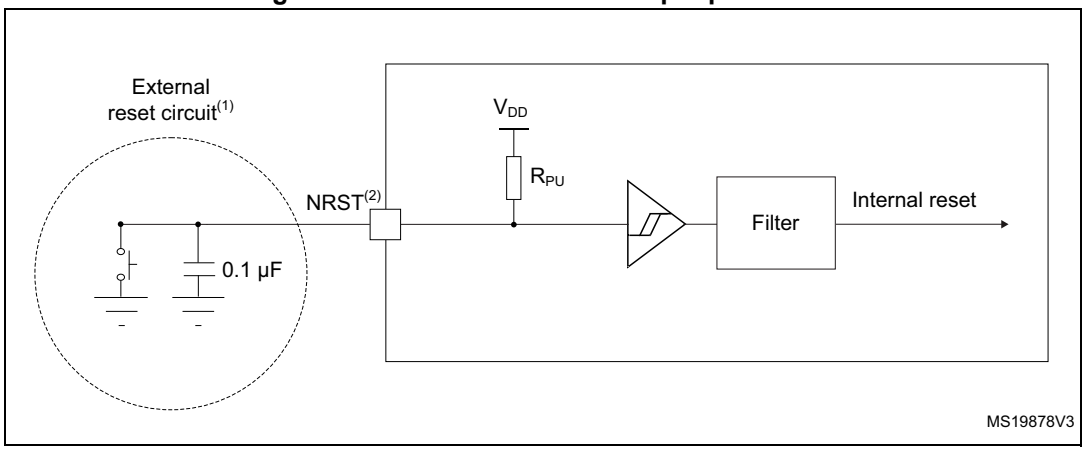
Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 22. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

Figure 27. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 62*. Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 63* are derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 25: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 63. ADC characteristics

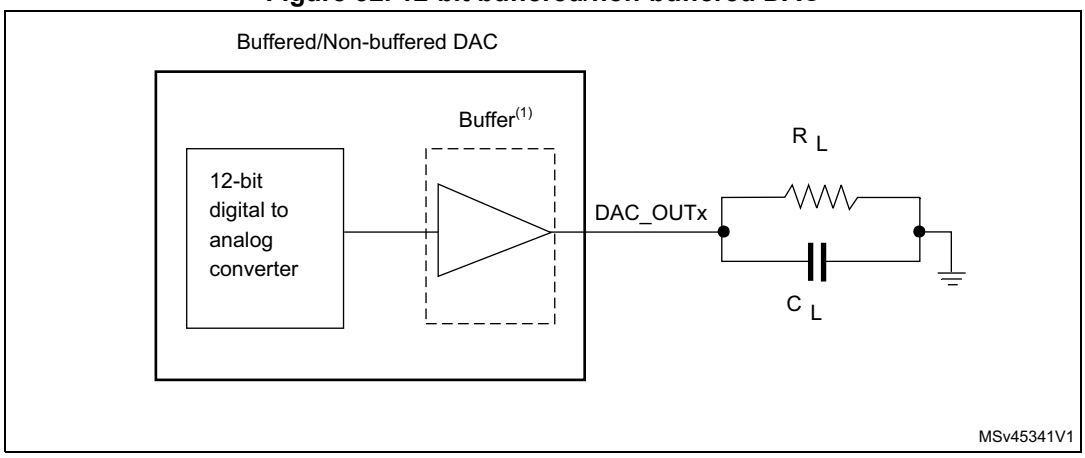
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	Fast channel	1.65	-	3.6	V
		Standard channel	1.75(1)	-	3.6	
$I_{DDA\ (ADC)}$	Current consumption of the ADC on V_{DDA} and V_{REF+}	1.14 Msps	-	200	-	µA
		10 ksps	-	40	-	
	Current consumption of the ADC on V_{DD}(2)	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
f_{ADC}	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
f_S(3)	Sampling rate	12-bit resolution	0.01	-	1.14	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 16 MHz, 12-bit resolution	-	-	941	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-		V
R_{AIN}(3)	External input impedance	See *Equation 1* and *Table 64* for details	-	-	50	kΩ

Table 66. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(9)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Guaranteed by design, not tested in production.
3. Connected between DAC_OUT and V_{SSA}.
4. Difference between two consecutive codes - 1 LSB.
5. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 32. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

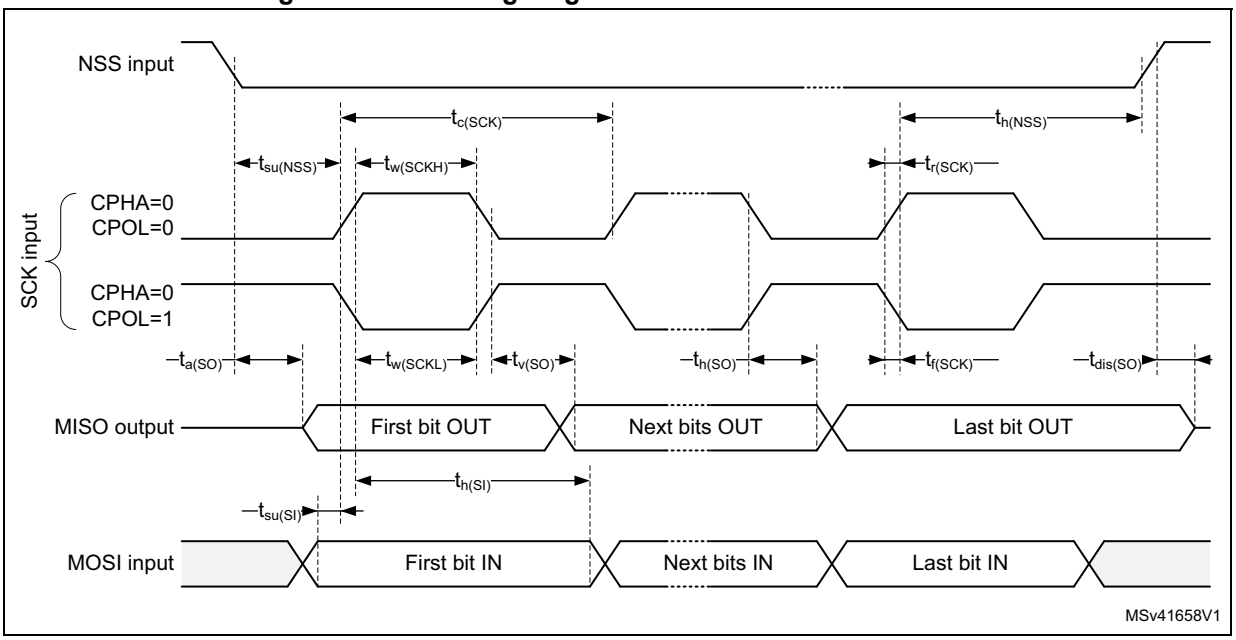
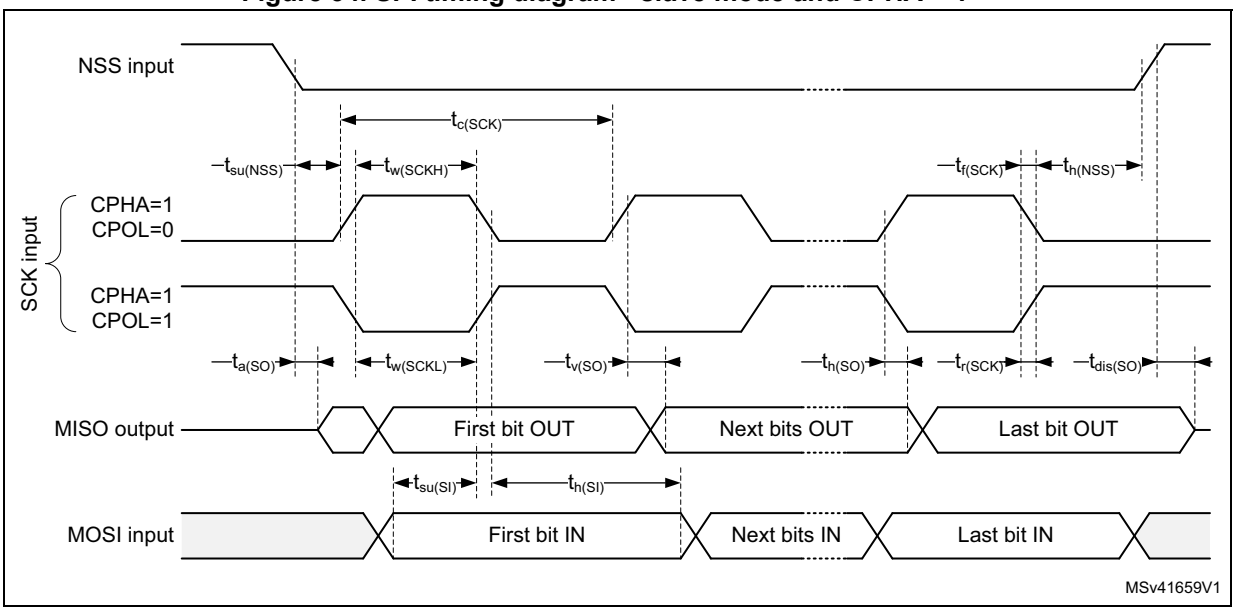


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 80. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

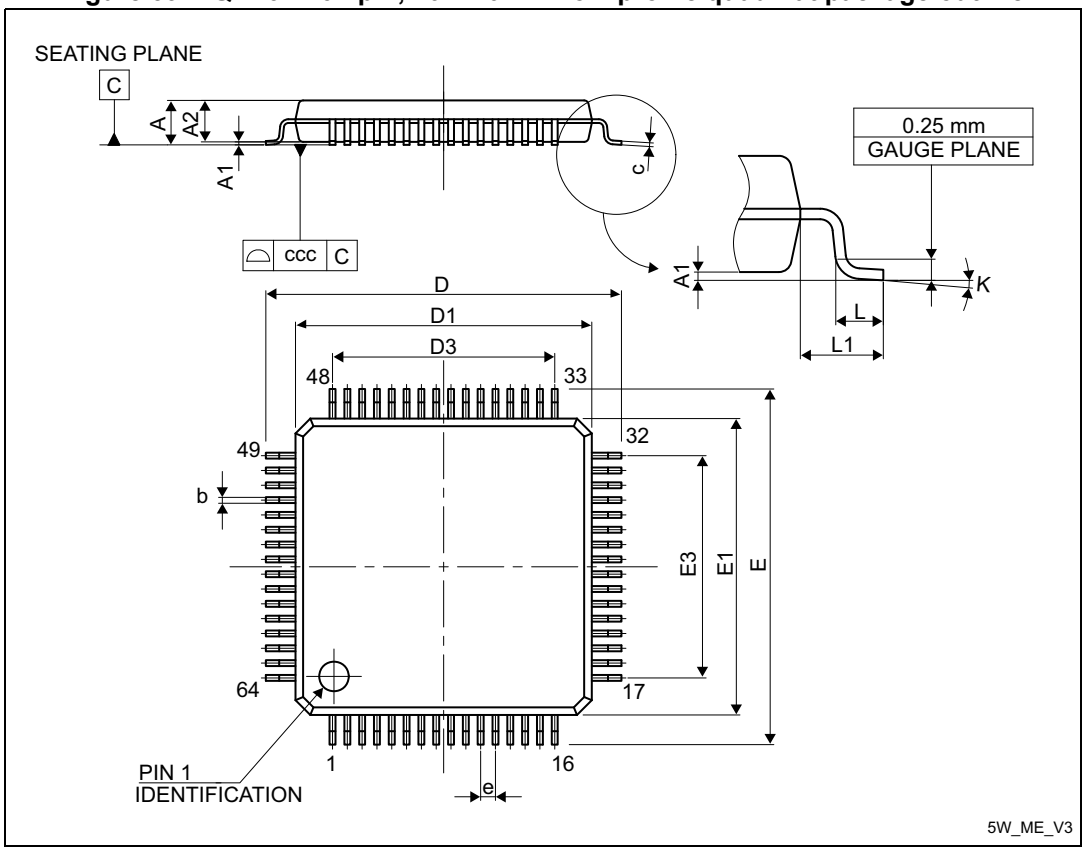
1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



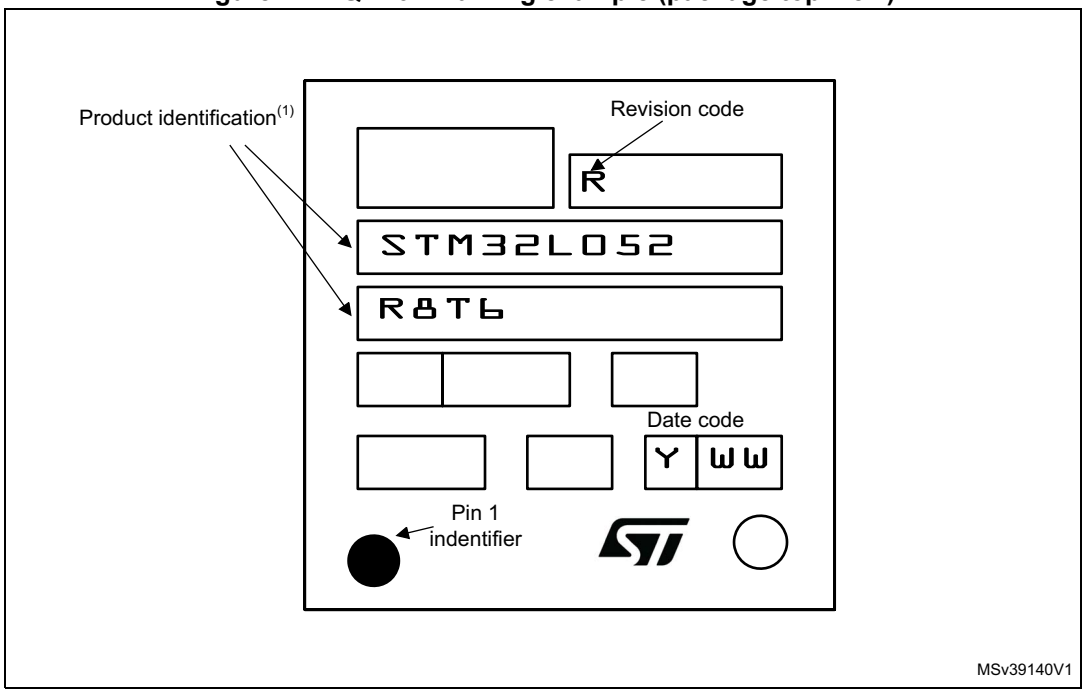
1. Drawing is not to scale.

Device marking for LQFP64

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

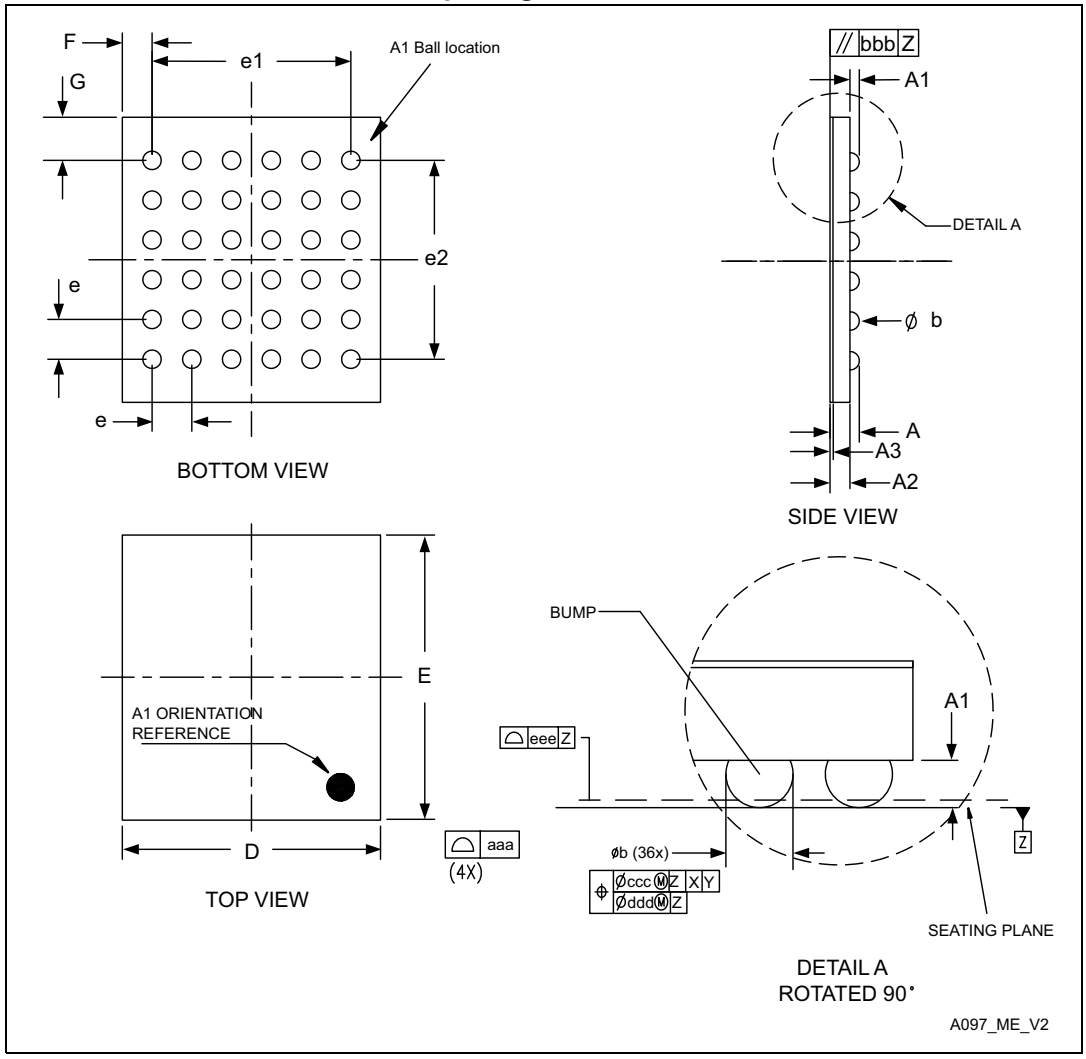
Figure 41. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 Thin WLCSP36 package information

Figure 51. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.
2. b dimensions is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

7.8 Thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max × Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

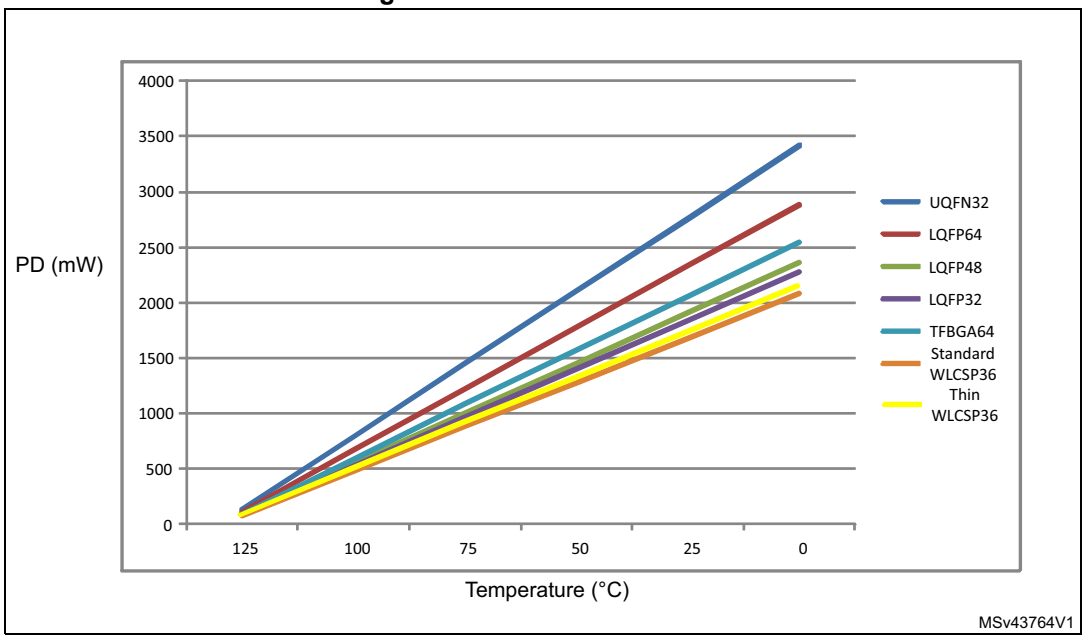
$P_{I/O}$ max = Σ (V_{OL} × I_{OL}) + Σ((V_{DD} – V_{OH}) × I_{OH}),

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 91. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** TFBGA64 - 5 x 5 mm / 0.5 mm pitch	61	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient Standard WLCSP36 - 0.4 mm pitch	63	
	Thermal resistance junction-ambient Thin WLCSP36 - 0.4 mm pitch	59	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	57	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	38	

Figure 59. Thermal resistance



7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 93. Document revision history (continued)

Date	Revision	Changes
05-Sep-2014	4	Extended operating temperature range to 125 °C. Updated minimum ADC operating voltage to 1.65 V. Changed number of I2S interface from 1 to 0 in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Replaced USART3 by LPUART1 in *Table 16: STM32L052x6/8 pin definitions* and LPUART by LPUART1 in *Table 17: Alternate function port A*, *Table 18: Alternate function port B*, *Table 19: Alternate function port C*, *Table 20: Alternate function port D* and *Table 21: Alternate function port H*. Updated PA6 in *Table 17: Alternate function port A*. Updated temperature range in *Section 1: Description*, *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Updated P_D, $T_{A\ and}$ T_J to add range 3 in *Table 25: General operating conditions*. Added range 3 in *Table 53: Flash memory and data EEPROM endurance and retention*, *Table 92: STM32L052x6/8 ordering information scheme*. Update note 1 in *Table 29: Current consumption in Run mode, code with data processing running from Flash*, *Table 31: Current consumption in Run mode, code with data processing running from RAM*, *Table 33: Current consumption in Sleep mode*, *Table 34: Current consumption in Low-power run mode*, *Table 34: Current consumption in Low-power run mode*, *Table 36: Typical and maximum current consumptions in Stop mode*, *Table 37: Typical and maximum current consumptions in Standby mode* and *Table 41: Low-power mode wakeup timings*. Updated *Figure 59: Thermal resistance* and removed note 1. Updated *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive*, *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 37: Typical and maximum current consumptions in Standby mode*. Updated SYSCFG in *Table 39: Peripheral current consumption in Run or Sleep mode*. Updated *Table 40: Peripheral current consumption in Stop and Standby mode* and *Table 43: Low-speed external user clock characteristics*. Updated ACC_{HSI16} temperature conditions in *Table 46: 16 MHz HSI16 oscillator characteristics*. Changed ambient temperature range in note 1 below *Table 47: HSI48 oscillator characteristics*. Updated $V_{F(NRST)}$ and $V_{NF(NRST)}$ in *Table 62: NRST pin characteristics*. Updated *Table 63: ADC characteristics* and *Table 65: ADC accuracy*. Added range 3 in *Table 92: STM32L052x6/8 ordering information scheme*.