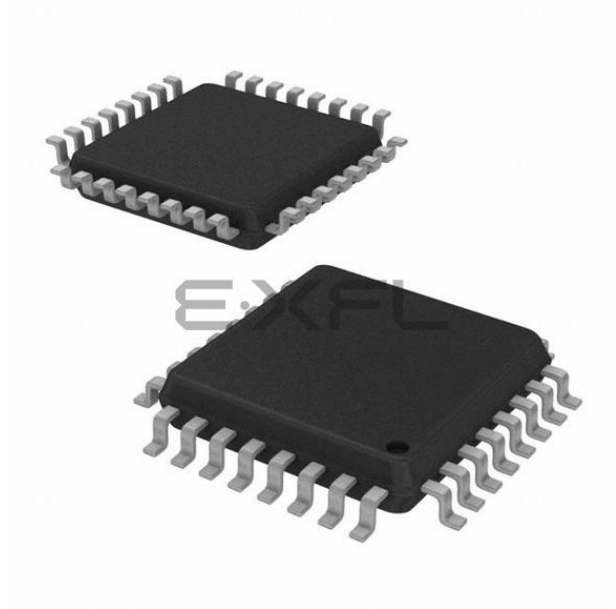

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052k6t6

Table 3. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance	Not functional
V_{DD} = 1.71 to 1.8 V(1)	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. To be USB compliant from the I/O voltage standpoint, the minimum V_{DD_USB} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36[1]	LQFP48	LQFP64	TFBGA64						
-	-	E2	21	29	G7	PB10	I/O	FT	-	TIM2_CH3, TSC_SYNC, LPUART1_TX, SPI2_SCK, I2C2_SCL	-
-	-	D2	22	30	H7	PB11	I/O	FT	-	EVENTOUT, TIM2_CH4, TSC_G6_IO1, LPUART1_RX, I2C2_SDA	-
16	-	-	23	31	D6	VSS	S	-	-	-	-
17	17	F1	24	32	E5	VDD	S	-	-	-	-
-	-	-	25	33	H8	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, LPUART1_RTS_DE, TSC_G6_IO2, I2C2_SMBA, EVENTOUT	-
-	-	-	26	34	G8	PB13	I/O	FTf	-	SPI2_SCK/I2S2_CK, TSC_G6_IO3, LPUART1_CTS, I2C2_SCL, TIM21_CH1	-
-	-	-	27	35	F8	PB14	I/O	FTf	-	SPI2_MISO/I 2S2_MCK, RTC_OUT, TSC_G6_IO4, LPUART1_RTS_DE, I2C2_SDA, TIM21_CH2	-
-	-	-	28	36	F7	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, RTC_REFIN	-
-	-	-	-	37	F6	PC6	I/O	FT	-	TIM22_CH1, TSC_G8_IO1	-
-	-	-	-	38	E7	PC7	I/O	FT	-	TIM22_CH2, TSC_G8_IO2	-
-	-	-	-	39	E8	PC8	I/O	FT	-	TIM22_ETR, TSC_G8_IO3	-

Table 20. Alternate function port D

Port		AF0
		LPUART1
Port D	PD2	LPUART1_RTS_DE

Table 21. Alternate function port H

Port		AF0
		USB
Port H	PH0	USB_CRS_SYNC
	PH1	-

Table 36. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode	T_A = − 40 to 25°C	0.41	1	µA
		T_A = 55°C	0.63	2.1	
		T_A= 85°C	1.7	4.5	
		T_A = 105°C	4	9.6	
		T_A = 125°C	11	24(2)	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Guaranteed by test in production.

Figure 17. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

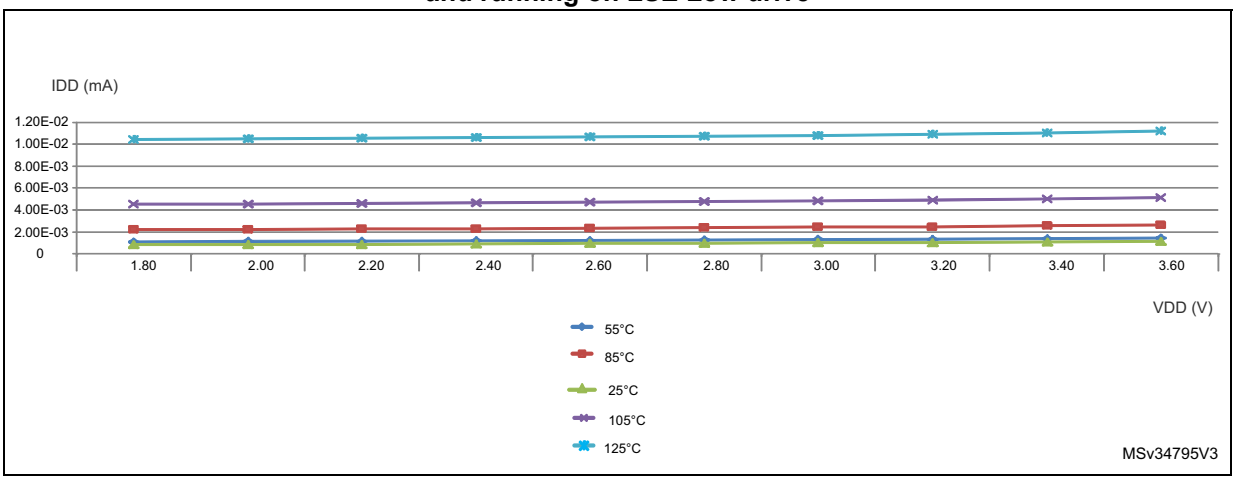


Figure 18. I_{DD} vs V_{DD}, at T_A= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF

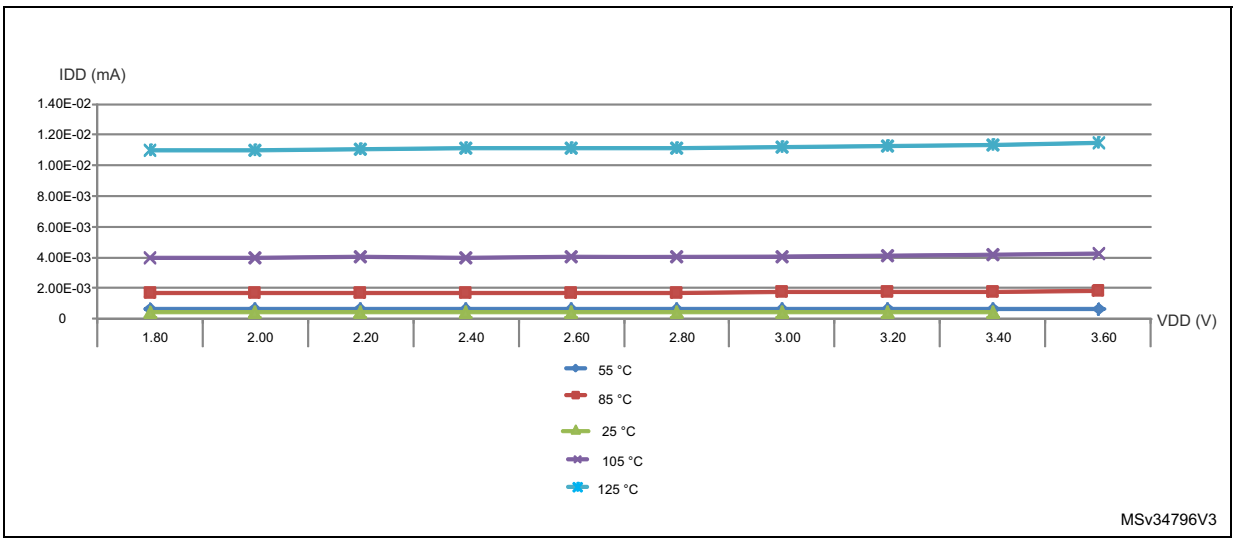


Table 40. Peripheral current consumption in Stop and Standby mode(1)

Symbol	Peripheral	Typical consumption, T_A = 25 °C		Unit
		V_{DD}=1.8 V	V_{DD}=3.0 V	
$I_{DD(PVD / BOR)}$	-	0.7	1.2	µA
I_{REFINT}	-	-	1.4	
-	LSE Low drive(2)	0,1	0,1	
-	LPTIM1, Input 100 Hz	0,01	0,01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0,2	0,2	
-	RTC	0,3	0,48	

1. LPTIM peripheral cannot operate in Standby mode.
2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

Table 41. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	7	8	Number of clock cycles
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash memory enabled	7	8	
		f_{HCLK} = 262 kHz Flash memory switched OFF	9	10	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

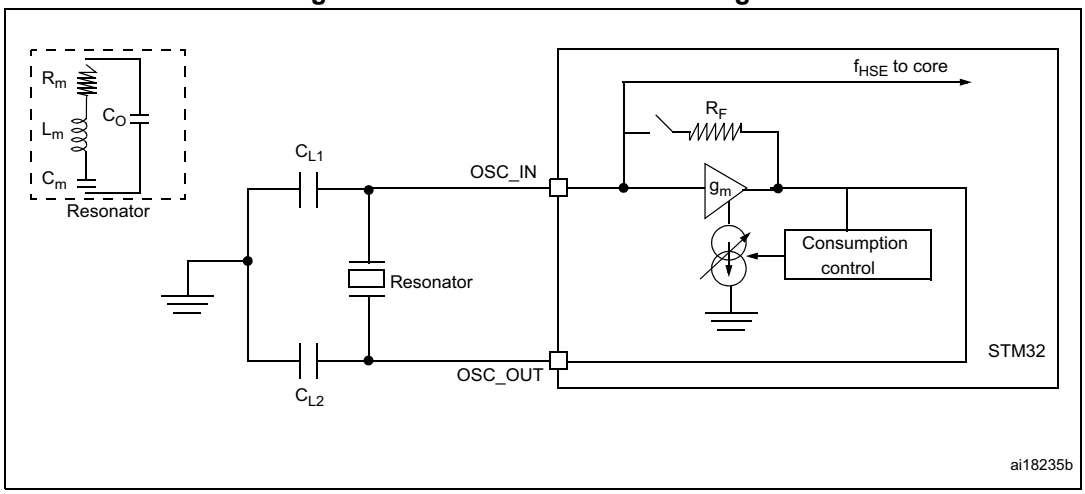
Table 44. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
G_m	Maximum critical crystal transconductance	Startup	-	-	700	µA /V
$t_{SU(HSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 21. HSE oscillator circuit diagram



6.3.9 Memory characteristics

RAM memory

Table 51. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 52. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
V_{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t_{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I_{DD}	Average current during the whole programming / erase operation	T_A = 25 °C, V_{DD} = 3.6 V	-	500	700	µA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 53. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{CYC}(2)	Cycling (erase / write) Program memory	T_A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T_A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 56. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1.	C4	500	

1. Guaranteed by characterization results.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 57. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.13 I/O port characteristics

General input/output characteristics

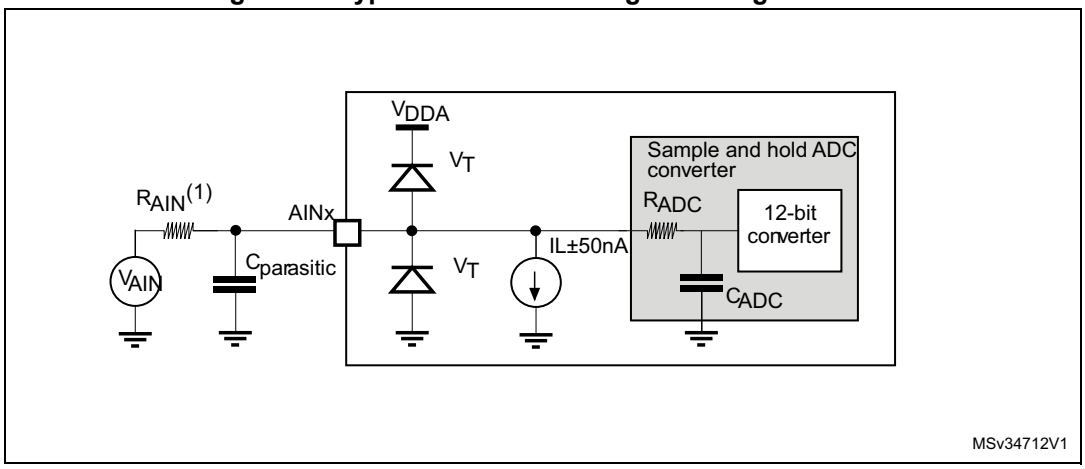
Unless otherwise specified, the parameters given in *Table 59* are derived from tests performed under the conditions summarized in *Table 25*. All I/Os are CMOS and TTL compliant.

Table 59. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TC, FT, FTf, RST I/Os	-	-	$0.3V_{DD}$	V
		BOOT0 pin	-	-	$0.14V_{DD}$ (1)	
V_{IH}	Input high level voltage	All I/Os	$0.7\ V_{DD}$	-	-	
V_{hys}	I/O Schmitt trigger voltage hysteresis (2)	Standard I/Os	-	$10\%\ V_{DD}$ (3)	-	
		BOOT0 pin	-	0.01	-	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	±50	nA
		$V_{SS} \le V_{IN} \le V_{DD}$, PA11 and PA12 I/Os	-	-	-50/+250	
		$V_{SS} \le V_{IN} \le V_{DD}$ FTf I/Os	-	-	±100	
		$V_{DD} \le V_{IN} \le 5$ V All I/Os except for PA11, PA12, BOOT0 and FTf I/Os	-	-	200	nA
		$V_{DD} \le V_{IN} \le 5$ V FTf I/Os	-	-	500	
		$V_{DD} \le V_{IN} \le 5$ V PA11, PA12 and BOOT0	-	-	10	µA
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	45	60	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	45	60	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by characterization.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 200 mV. Guaranteed by characterization results.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 29. Typical connection diagram using the ADC

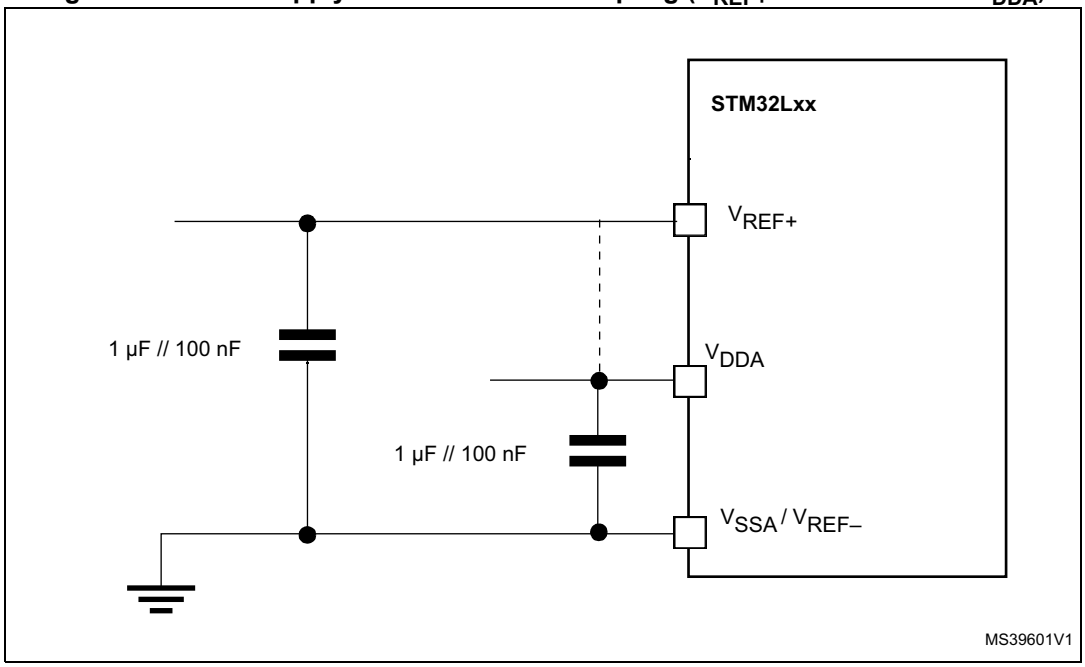


1. Refer to *Table 63: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 30* or *Figure 31*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 30. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



The analog spike filter is compliant with I^2C timings requirements only for the following voltage ranges:

- Fast mode Plus: 2.7 V ≤V_{DD} ≤3.6 V and voltage scaling Range 1
- Fast mode:
  - 2 V ≤V_{DD} ≤3.6 V and voltage scaling Range 1 or Range 2.
  - V_{DD} < 2 V, voltage scaling Range 1 or Range 2, C_{load} < 200 pF.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 72. I2C analog filter characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50(2)	260(3)	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 73. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when the USART/LPUART is clocked by HSI	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	µs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

Figure 33. SPI timing diagram - slave mode and CPHA = 0

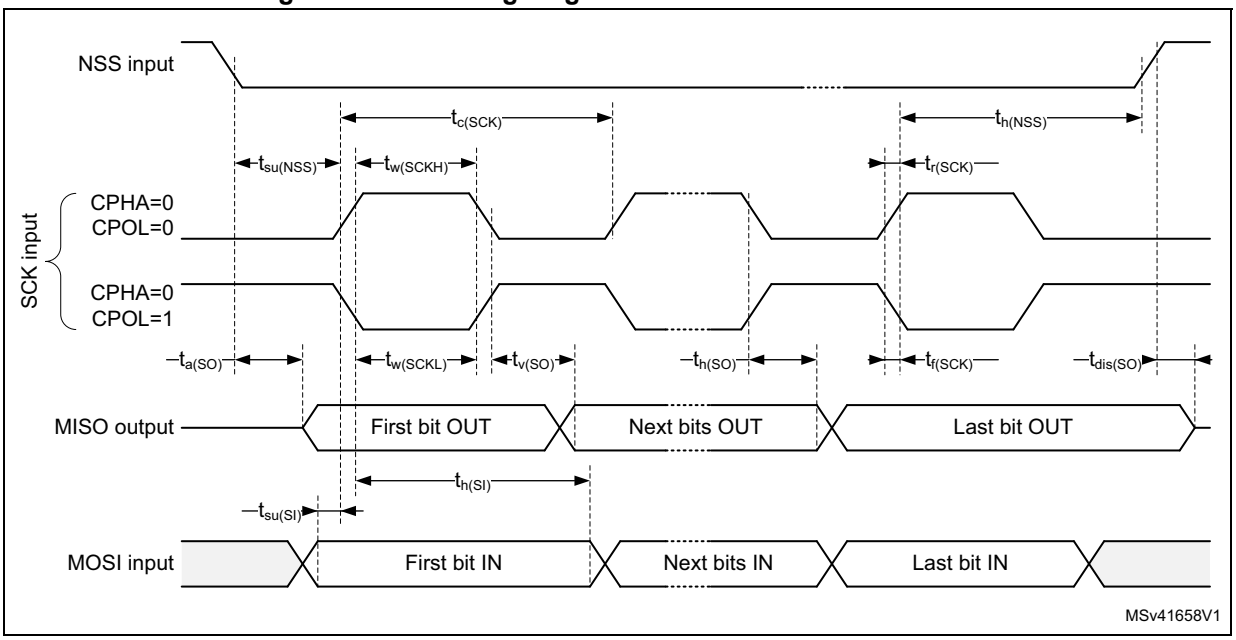
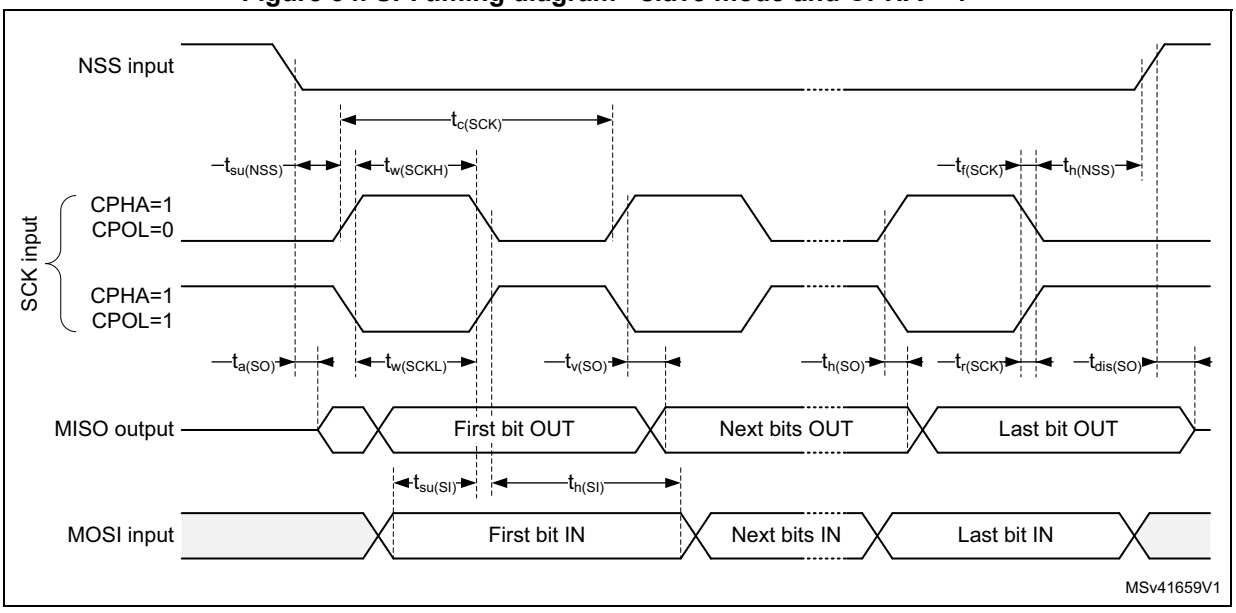


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



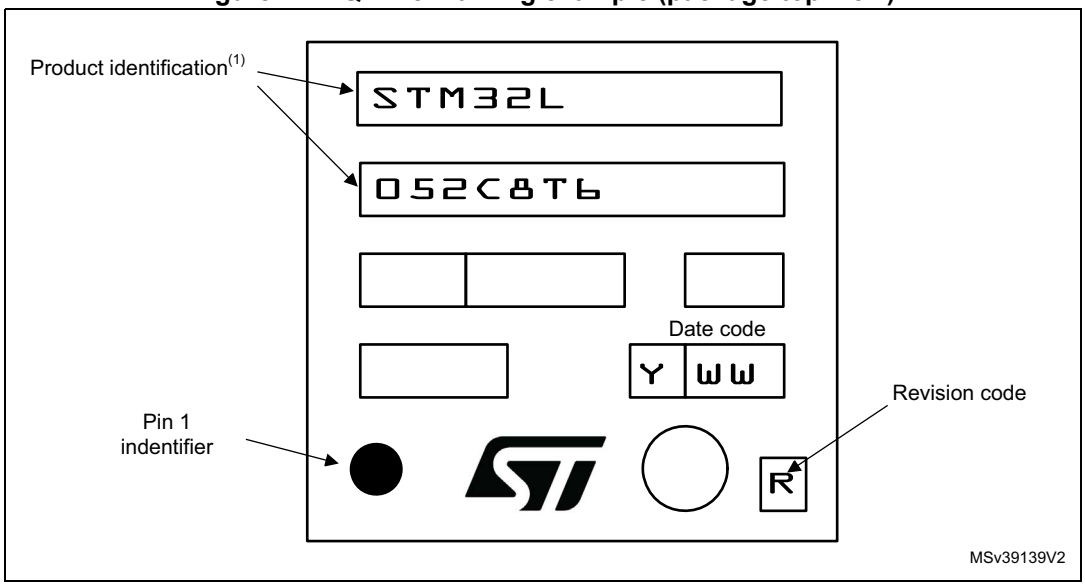
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Device marking for LQFP48

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 47. LQFP48 marking example (package top view)



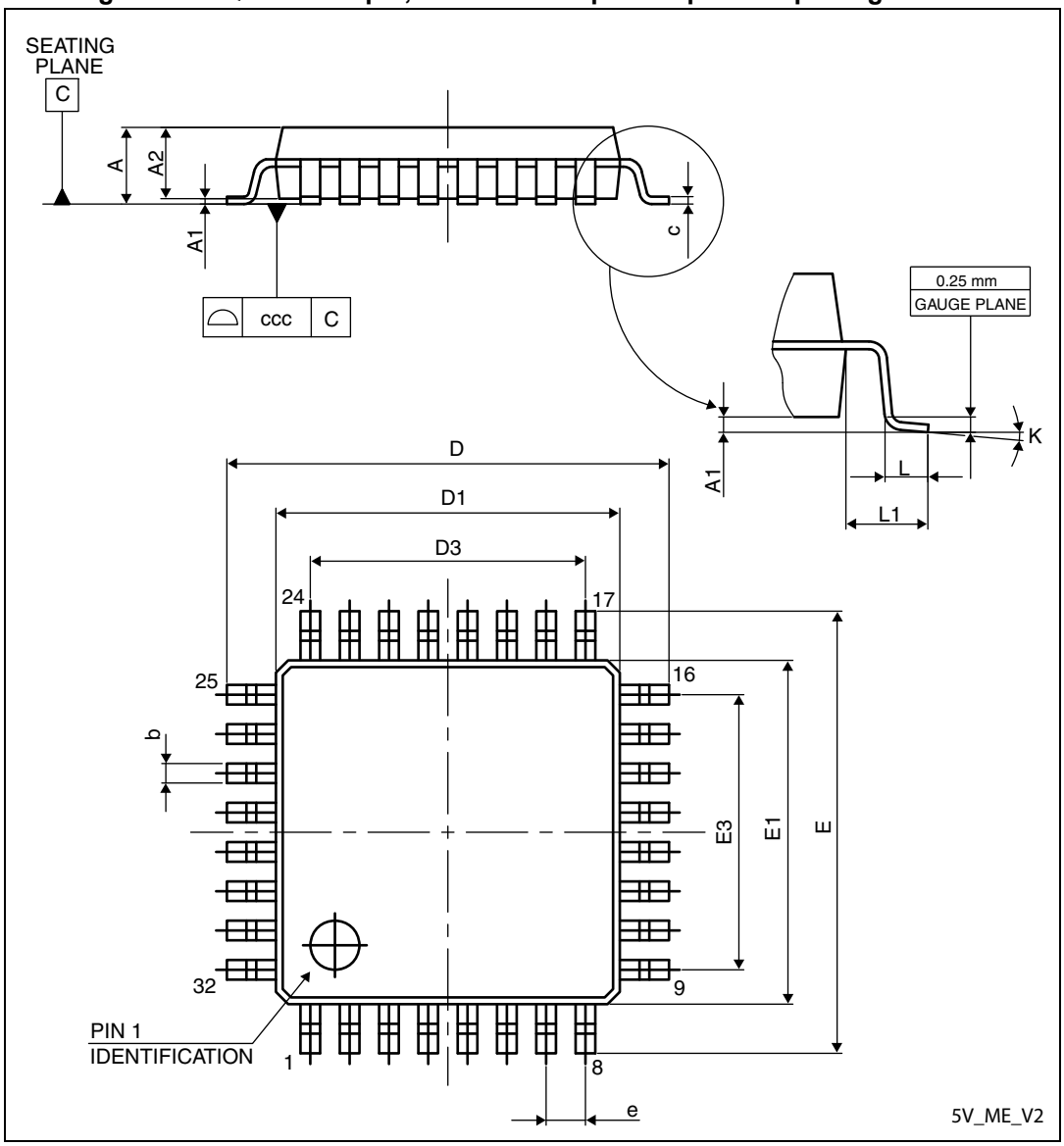
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 88. WLCSP36 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

7.6 LQFP32 package information

Figure 53. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



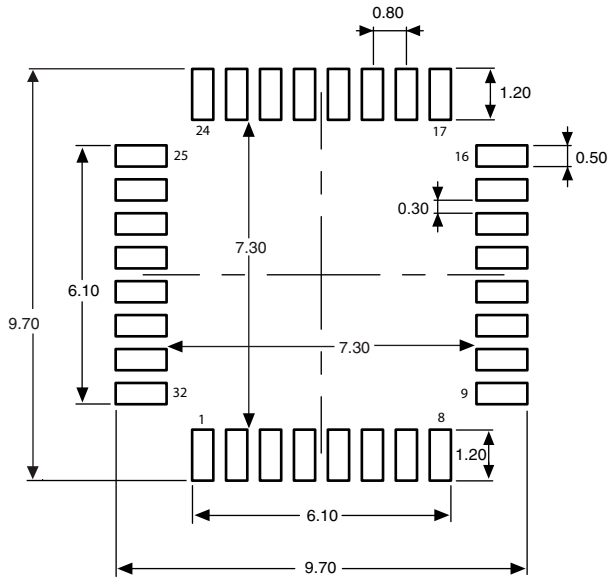
1. Drawing is not to scale.

Table 89. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint



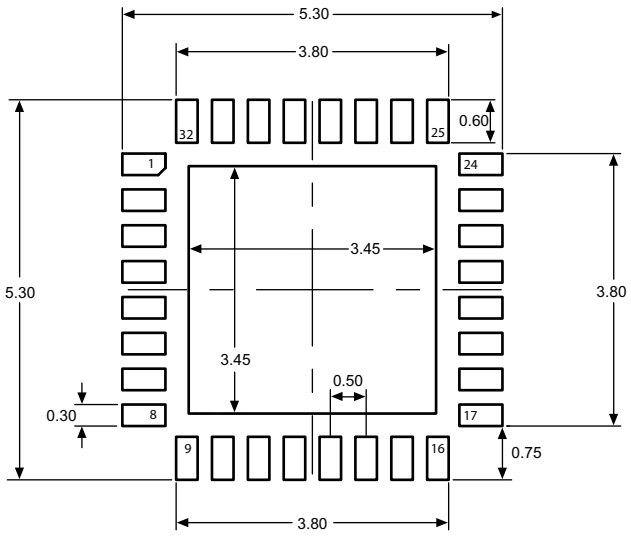
1. Dimensions are expressed in millimeters.

Table 90. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 57. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint



1. Dimensions are expressed in millimeters.

9 Revision history

Table 93. Document revision history

Date	Revision	Changes
27-Feb-2014	1	Initial release.
29-Apr-2014	2	Added WLCSP36 package. Updated *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts* Updated *Figure 4: STM32L052x6/8 TFBGA64 ballout - 5x 5 mm*. Updated *Table 5: Functionalities depending on the working mode (from Run/active down to standby)*. Added *Section 3.2: Interconnect matrix*. Replaced TTa I/O structure by TC, updated PA0/4/5, PC5/14, BOOT0 and NRST I/O structure, and added note 3 in *Table 16: STM32L052x6/8 pin definitions*. Updated *Table 25: General operating conditions*, *Table 22: Voltage characteristics* and *Table 23: Current characteristics*. Modified conditions in *Table 28: Embedded internal reference voltage*. Updated *Table 29: Current consumption in Run mode, code with data processing running from Flash*, *Table 31: Current consumption in Run mode, code with data processing running from RAM*, *Table 33: Current consumption in Sleep mode*, *Table 34: Current consumption in Low-power run mode*, *Table 35: Current consumption in Low-power sleep mode*, and *Table 36: Typical and maximum current consumptions in Stop modeTable 37: Typical and maximum current consumptions in Standby mode*. Added *Figure 14: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS*, *Figure 15: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS*, *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 44: HSE oscillator characteristics* and *Table 45: LSE oscillator characteristics*. Added *Figure 23: HSI16 minimum and maximum value versus temperature*. Updated *Table 56: ESD absolute maximum ratings*, *Table 58: I/O current injection susceptibility* and *Table 59: I/O static characteristics*, and added *Figure 24: VIH/VIL versus VDD (CMOS I/Os)* and *Figure 25: VIH/VIL versus VDD (TTL I/Os)*. Updated *Table 60: Output voltage characteristics*, *Table 61: I/O AC characteristics*, and *Figure 26: I/O AC characteristics definition*. Updated *Table 63: ADC characteristics*, *Table 65: ADC accuracy*, and *Figure 29: Typical connection diagram using the ADC*. Updated *Table 68: Temperature sensor characteristics*. Updated *Table 74: SPI characteristics in voltage Range 1* and *Table 77: I2S characteristics*. Added *Figure 59: Thermal resistance*.

Table 93. Document revision history (continued)

Date	Revision	Changes
11-Mar-2016	6	Updated number of SPIs on cover page and in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Changed minimum comparator supply voltage to 1.65 V on cover page. Added number of fast and standard channels in *Section 3.11: Analog-to-digital converter (ADC)*. Updated *Section 3.18.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.18.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.18.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.18.3: Low-power universal asynchronous receiver transmitter (LPUART)*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated *Table 58: I/O current injection susceptibility*. Updated *Figure 6: STM32L052x6/8 WLCSP36 ballout*, *Figure 8: STM32L052x6/8 UFQFPN32 pinout* removing grey PA11, PA12 pins and removing note 2. Updated *Table 55: EMI characteristics*. Changed temperature condition in *Table 8: Internal voltage reference measured values* and *Table 27: Embedded internal reference voltage calibration values*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 63: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note 1 Added note 4 related to R_{ADC}. Updated f_{TRIG}. Updated t_S and t_{CONV}. – Updated equation 1 description. – Updated *Table 64: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. Updated R_O and added Note 2 in *Table 66: DAC characteristics*. Added *Table 73: USART/LPUART characteristics*. Updated *Figure 47: LQFP48 marking example (package top view)*.

Table 93. Document revision history (continued)

Date	Revision	Changes
07-Mar-2017	7	Added thin WLCSP36 package. Updated number of I2S interfaces and removed I2S for STM32L052T8 in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. In *Section 4: Pin descriptions*, renamed USB_OE into USB_NOE. Added mission profile compliance with JEDEC JESD47 in *Section 6.2: Absolute maximum ratings*. Added note 2. related to the position of the external capacitor below *Figure 27: Recommended NRST pin protection*. Updated R_L in *Table 63: ADC characteristics*. Updated *Figure 32: 12-bit buffered/non-buffered DAC* and added note below figure. Updated t_{AF} maximum value for range 1 in *Table 72: I2C analog filter characteristics*. Updated $t_{WUUSART}$ description in *Table 73: USART/LPUART characteristics*. NSS timing waveforms updated in *Figure 33: SPI timing diagram - slave mode and CPHA = 0* and *Figure 34: SPI timing diagram - slave mode and CPHA = 1(1)*. Previous WLCSP36 package renamed “Standard” WLCSP36; added Note *2.* below *Figure 48: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline* and updated *Table 85: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data*. Added reference to optional marking or inset/upset marks in all package device marking sections.