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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052k6u6

2 Description

The ultra-low-power STM32L052x6/8 microcontrollers incorporate the connectivity power of the universal serial bus (USB 2.0 crystal-less) with the high-performance ARM® Cortex®-M0+ 32-bit RISC core operating at a 32 MHz frequency, a memory protection unit (MPU), high-speed embedded memories (64 Kbytes of Flash program memory, 2 Kbytes of data EEPROM and 8 Kbytes of RAM) plus an extensive range of enhanced I/Os and peripherals.

The STM32L052x6/8 devices provide high power efficiency for a wide range of performance. It is achieved with a large choice of internal and external clock sources, an internal voltage adaptation and several low-power modes.

The STM32L052x6/8 devices offer several analog features, one 12-bit ADC with hardware oversampling, one DAC, two ultra-low-power comparators, several timers, one low-power timer (LPTIM), three general-purpose 16-bit timers and one basic timer, one RTC and one SysTick which can be used as timebases. They also feature two watchdogs, one watchdog with independent clock and window capability and one window watchdog based on bus clock.

Moreover, the STM32L052x6/8 devices embed standard and advanced communication interfaces: up to two I2C, two SPIs, one I2S, two USARTs, a low-power UART (LPUART), and a crystal-less USB. The devices offer up to 24 capacitive sensing channels to simply add touch sensing functionality to any application.

The STM32L052x6/8 also include a real-time clock and a set of backup registers that remain powered in Standby mode.

The ultra-low-power STM32L052x6/8 devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +125 °C temperature range. A comprehensive set of power-saving modes allows the design of low-power applications.



2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L052x6/8 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L052x6/8 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L052x6/8 device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 μ A at 10 kSPS, ~200 μ A at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.12 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

3.17.4 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches '0'.

3.17.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.17.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.18 Communication interfaces

3.18.1 I²C bus

two I²C interface (I2C1, I2C2) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

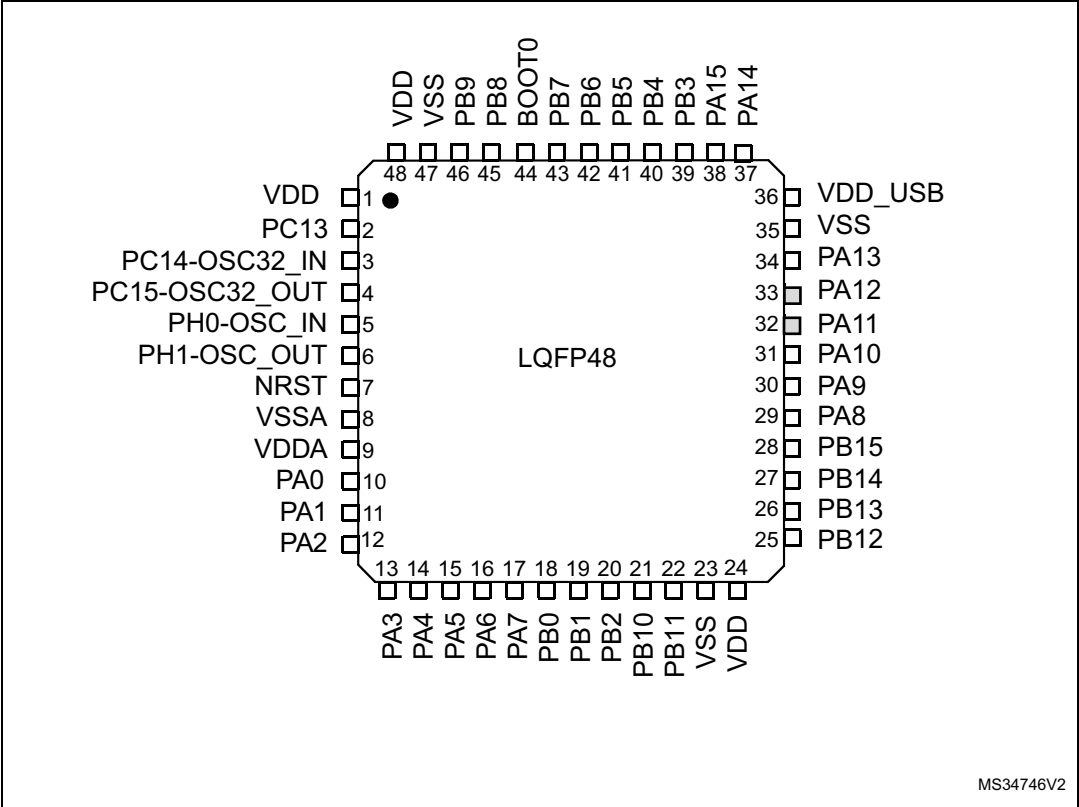
7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 11. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

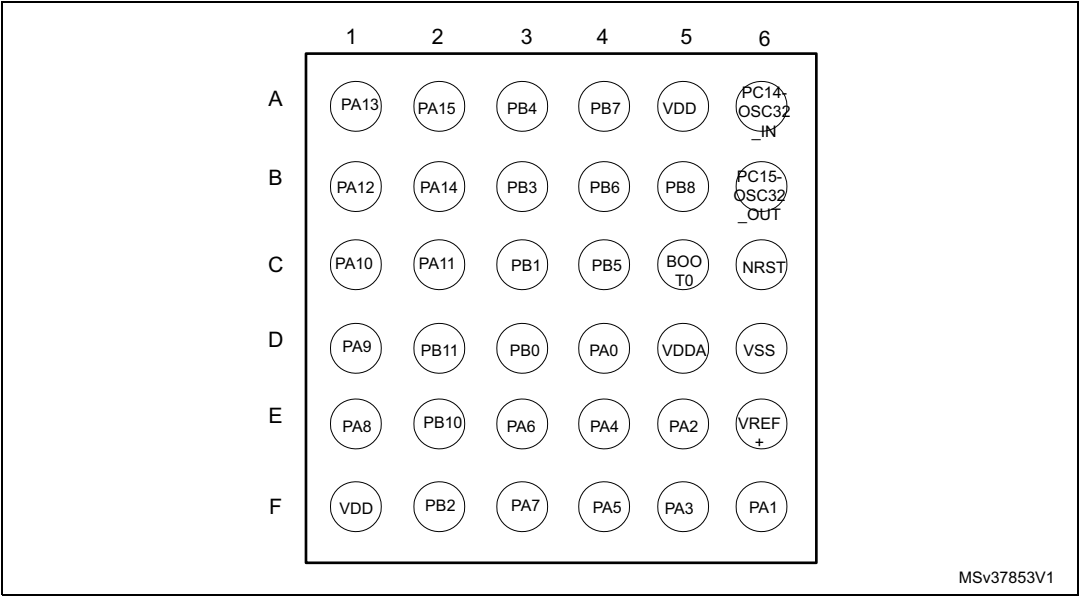
In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

Figure 5. STM32L052x6/8 LQFP48 pinout - 7 x 7 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Figure 6. STM32L052x6/8 WLCSP36 ballout



1. The above figure shows the package top view.

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36 ⁽¹⁾	LQFP48	LQFP64	TFBGA64						
-	-	-	-	40	D8	PC9	I/O	FT	-	TIM21_ETR, USB_NOE, TSC_G8_IO4	-
18	18	E1	29	41	D7	PA8	I/O	FT	-	MCO, USB_CR_S_SYNC, EVENTOUT, USART1_CK	-
19	19	D1	30	42	C7	PA9	I/O	FT	-	MCO, TSC_G4_IO1, USART1_TX	-
20	20	C1	31	43	C6	PA10	I/O	FT	-	TSC_G4_IO2, USART1_RX	-
21	21	C2	32	44	C8	PA11 ⁽³⁾	I/O	FT	-	SPI1_MISO, EVENTOUT, TSC_G4_IO3, USART1_CTS, COMP1_OUT	USB_DM
22	22	B1	33	45	B8	PA12 ⁽³⁾	I/O	FT	-	SPI1_MOSI, EVENTOUT, TSC_G4_IO4, USART1_RTS_DE, COMP2_OUT	USB_DP
23	23	A1	34	46	A8	PA13	I/O	FT	-	SWDIO, USB_NOE	-
-	-	-	35	47	D5	VSS	S	-	-	-	-
-	-	-	36	48	E6	VDD_USB	S	-	-	-	-
24	24	B2	37	49	A7	PA14	I/O	FT	-	SWCLK, USART2_TX	-
25	25	A2	38	50	A6	PA15	I/O	FT	-	SPI1_NSS, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	-
-	-	-	-	51	B7	PC10	I/O	FT	-	LPUART1_TX	-
-	-	-	-	52	B6	PC11	I/O	FT	-	LPUART1_RX	-
-	-	-	-	53	C5	PC12	I/O	FT	-	-	-

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36 ⁽¹⁾	LQFP48	LQFP64	TFBGA64						
-	-	-	-	54	B5	PD2	I/O	FT	-	LPUART1_RTS_DE	-
26	26	B3	39	55	A5	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, TSC_G5I_O1, EVENTOUT	COMP2_INN
27	27	A3	40	56	A4	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TSC_G5_IO2, TIM22_CH1	COMP2_INP
28	28	C4	41	57	C4	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
29	29	B4	42	58	D3	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
30	30	A4	43	59	C3	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4	COMP2_INP, PVD_IN
31	31	C5	44	60	B4	BOOT0	B	-	-	-	-
-	32	B5	45	61	B3	PB8	I/O	FTf	-	TSC_SYNC, I2C1_SCL	-
-	-	-	46	62	A3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
32	-	D6	47	63	D4	VSS	S	-	-	-	-
1	1	A5	48	64	E4	VDD	S	-	-	-	-

1. PB9/12/13/14/15, PH0/1 and PC13 GPIOs should be configured as output and driven Low, even if they are not available on this package.
2. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.
3. These pins are powered by VDD_USB. For all characteristics that refer to V_{DD}, V_{DD_USB} must be used instead.

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 22: Voltage characteristics](#), [Table 23: Current characteristics](#), and [Table 24: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 22. Voltage characteristics

Symbol	Definition	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} , V_{DD_USB} , V_{DD}) ⁽¹⁾	-0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS}-0.3$	$V_{DD}+4.0$	
	Input voltage on TC pins	$V_{SS}-0.3$	4.0	
	Input voltage on BOOT0	V_{SS}	$V_{DD}+4.0$	
	Input voltage on any other pin	$V_{SS}-0.3$	4.0	
$ \Delta V_{DD} $	Variations between different V_{DDx} power pins	-	50	mV
$ V_{DDA}-V_{DDx} $	Variations between any V_{DDx} and V_{DDA} power pins ⁽³⁾	-	300	
$ \Delta V_{SS} $	Variations between all different ground pins	-	50	
$V_{REF+}-V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.11		

1. All main power (V_{DD} , V_{DD_USB} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 23](#) for maximum allowed injected current values.
3. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and device operation. V_{DD_USB} is independent from V_{DD} and V_{DDA} : its value does not need to respect this rule.

Table 29. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f _{HCLK}	Typ	Max ⁽¹⁾	Unit
I _{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽²⁾	Range 3, V _{CORE} =1.2 V VOS[1:0]=11	1 MHz	165	230	μA
				2 MHz	290	360	
				4 MHz	555	630	
			Range 2, V _{CORE} =1.5 V, VOS[1:0]=10,	4 MHz	0.665	0.74	mA
				8 MHz	1.3	1.4	
				16 MHz	2.6	2.8	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	8 MHz	1.55	1.7	
				16 MHz	3.1	3.4	
				32 MHz	6.3	6.8	
		MSI clock	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	65 kHz	36.5	110	μA
				524 kHz	99.5	190	
				4.2 MHz	620	700	
		HSI clock	Range 2, V _{CORE} =1.5 V, VOS[1:0]=10,	16 MHz	2.6	2.9	mA
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	32 MHz	6.25	7	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 30. Current consumption in Run mode vs code type, code with data processing running from Flash

Symbol	Parameter	Conditions			f _{HCLK}	Typ	Unit
I _{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f _{HSE} = f _{HCLK} up to 16 MHz included, f _{HSE} = f _{HCLK} /2 above 16 MHz (PLL ON) ⁽¹⁾	Range 3, V _{CORE} =1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	555	μA
				CoreMark		585	
				Fibonacci		440	
				while(1)		355	
				while(1), prefetch OFF		353	
			Range 1, V _{CORE} =1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6.3	mA
				CoreMark		6.3	
				Fibonacci		6.55	
				while(1)		5.4	
				while(1), prefetch OFF		5.2	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 37. Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
I _{DD} (Standby)	Supply current in Standby mode	Independent watchdog and LSI enabled	T _A = - 40 to 25°C	1.3	1.7
			T _A = 55 °C	-	2.9
			T _A = 85 °C	-	3.3
			T _A = 105 °C	-	4.1
			T _A = 125 °C	-	8.5
		Independent watchdog and LSI OFF	T _A = - 40 to 25°C	0.29	0.6
			T _A = 55 °C	0.32	0.9
			T _A = 85 °C	0.5	2.3
			T _A = 105 °C	0.94	3
			T _A = 125 °C	2.6	7

1. Guaranteed by characterization results at 125 °C, unless otherwise specified

Table 38. Average current consumption during Wakeup

Symbol	parameter	System frequency	Current consumption during wakeup	Unit
I _{DD} (Wakeup from Stop)	Supply current during Wakeup from Stop mode	HSI	1	mA
		HSI/4	0,7	
		MSI clock = 4,2 MHz	0,7	
		MSI clock = 1,05 MHz	0,4	
		MSI clock = 65 KHz	0,1	
I _{DD} (Reset)	Reset pin pulled down	-	0,21	
I _{DD} (Power-up)	BOR ON	-	0,23	
I _{DD} (Wakeup from StandBy)	With Fast wakeup set	MSI clock = 2,1 MHz	0,5	
	With Fast wakeup disabled	MSI clock = 2,1 MHz	0,12	

Table 39. Peripheral current consumption in Run or Sleep mode⁽¹⁾ (continued)

Peripheral		Typical consumption, $V_{DD} = 3.0\text{ V}$, $T_A = 25\text{ °C}$				Unit
		Range 1, $V_{CORE}=1.8\text{ V}$ $VOS[1:0] = 01$	Range 2, $V_{CORE}=1.5\text{ V}$ $VOS[1:0] = 10$	Range 3, $V_{CORE}=1.2\text{ V}$ $VOS[1:0] = 11$	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	$\mu\text{A/MHz}$ (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GIOD	1	0.5	0.5	0.5	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	$\mu\text{A/MHz}$ (f_{HCLK})
	FLASH	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	0 ⁽³⁾	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		283	225	222.5	212.5	$\mu\text{A/MHz}$ (f_{HCLK})
PWR		2.5	2	2	1	$\mu\text{A/MHz}$ (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF and one peripheral with clock enabled, in the following conditions: $f_{HCLK} = 32\text{ MHz}$ (range 1), $f_{HCLK} = 16\text{ MHz}$ (range 2), $f_{HCLK} = 4\text{ MHz}$ (range 3), $f_{HCLK} = 64\text{ kHz}$ (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 μA .

Table 40. Peripheral current consumption in Stop and Standby mode⁽¹⁾

Symbol	Peripheral	Typical consumption, T _A = 25 °C		Unit
		V _{DD} =1.8 V	V _{DD} =3.0 V	
I _{DD} (PVD / BOR)	-	0.7	1.2	μA
I _{REFINT}	-	-	1.4	
-	LSE Low drive ⁽²⁾	0,1	0,1	
-	LPTIM1, Input 100 Hz	0,01	0,01	
-	LPTIM1, Input 1 MHz	6	6	
-	LPUART1	0,2	0,2	
-	RTC	0,3	0,48	

1. LPTIM peripheral cannot operate in Standby mode.

2. LSE Low drive consumption is the difference between an external clock on OSC32_IN and a quartz between OSC32_IN and OSC32_OUT.-

6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI or HSI16 RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is either the MSI oscillator in the range configured before entering Stop mode, the HSI16 or HSI16/4.
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 25](#).

Table 41. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max	Unit
t _{WUSLEEP}	Wakeup from Sleep mode	f _{HCLK} = 32 MHz	7	8	Number of clock cycles
t _{WUSLEEP_LP}	Wakeup from Low-power sleep mode, f _{HCLK} = 262 kHz	f _{HCLK} = 262 kHz Flash memory enabled	7	8	
		f _{HCLK} = 262 kHz Flash memory switched OFF	9	10	

Table 41. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	5.0	8	μs
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	7.3	13	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	13	23	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	28	38	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	51	65	
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	100	120	
		$f_{HCLK} = f_{MSI} = 65 \text{ kHz}$	190	260	
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	7.9	10	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode, FWU bit = 1	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	65	130	μs
	Wakeup from Standby mode, FWU bit = 0	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	2.2	3	ms

6.3.9 Memory characteristics

RAM memory

Table 51. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode ⁽¹⁾	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

Flash memory and data EEPROM

Table 52. Flash memory and data EEPROM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
V _{DD}	Operating voltage Read / Write / Erase	-	1.65	-	3.6	V
t _{prog}	Programming time for word or half-page	Erasing	-	3.28	3.94	ms
		Programming	-	3.28	3.94	
I _{DD}	Average current during the whole programming / erase operation	T _A = 25 °C, V _{DD} = 3.6 V	-	500	700	μA
	Maximum current (peak) during the whole programming / erase operation		-	1.5	2.5	mA

1. Guaranteed by design.

Table 53. Flash memory and data EEPROM endurance and retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N _{CYC} ⁽²⁾	Cycling (erase / write) Program memory	T _A = -40°C to 105 °C	10	kcycles
	Cycling (erase / write) EEPROM data memory		100	
	Cycling (erase / write) Program memory	T _A = -40°C to 125 °C	0.2	
	Cycling (erase / write) EEPROM data memory		2	

Table 63. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ADC}^{(3)(4)}$	Sampling switch resistance	-	-	-	1	k Ω
$C_{ADC}^{(3)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{CAL}^{(3)(5)}$	Calibration time	$f_{ADC} = 16$ MHz	5.2			μ s
		-	83			$1/f_{ADC}$
$W_{LATENCY}^{(6)}$	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
$t_{latr}^{(3)}$	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 16$ MHz	0.266			μ s
		$f_{ADC} = f_{PCLK}/2$	8.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 8$ MHz	0.516			μ s
		$f_{ADC} = f_{PCLK}/4$	16.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16} = 16$ MHz	0.252	-	0.260	μ s
Jitter _{ADC}	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI16}$	-	1	-	$1/f_{HSI16}$
$t_S^{(3)}$	Sampling time	$f_{ADC} = 16$ MHz	0.093	-	10.03	μ s
		-	1.5	-	160.5	$1/f_{ADC}$
$t_{UP_LDO}^{(3)(5)}$	Internal LDO power-up time	-	-	-	10	μ s
$t_{STAB}^{(3)(5)}$	ADC stabilization time	-	14			$1/f_{ADC}$
$t_{ConV}^{(3)}$	Total conversion time (including sampling time)	$f_{ADC} = 16$ MHz, 12-bit resolution	0.875	-	10.81	μ s
		12-bit resolution	14 to 173 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to [Table 64: RAIN max for \$f_{ADC} = 16\$ MHz](#).
2. A current consumption proportional to the APB clock frequency has to be added (see [Table 39: Peripheral current consumption in Run or Sleep mode](#)).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to [Table 64: RAIN max for \$f_{ADC} = 16\$ MHz](#).
5. This parameter only includes the ADC timing. It does not take into account register access latency.
6. This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 78. USB startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB transceiver startup time	1	μs

1. Guaranteed by design.

Table 79. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾	Max. ⁽¹⁾	Unit
Input levels					
V _{DD}	USB operating voltage	-	3.0	3.6	V
V _{DI} ⁽²⁾	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V _{CM} ⁽²⁾	Differential common mode range	Includes V _{DI} range	0.8	2.5	
V _{SE} ⁽²⁾	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V _{OL} ⁽³⁾	Static output level low	R _L of 1.5 kΩ to 3.6 V ⁽⁴⁾	-	0.3	V
V _{OH} ⁽³⁾	Static output level high	R _L of 15 kΩ to V _{SS} ⁽⁴⁾	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_{L} is the load connected on the USB drivers.

Figure 38. USB timings: definition of data signal rise and fall time

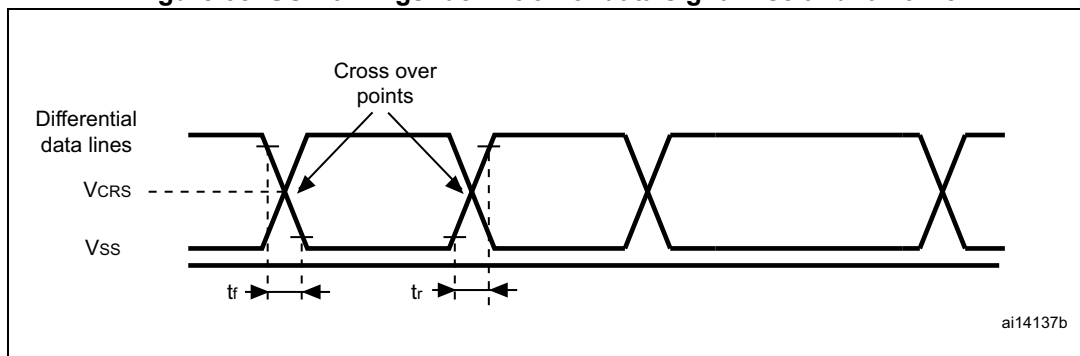
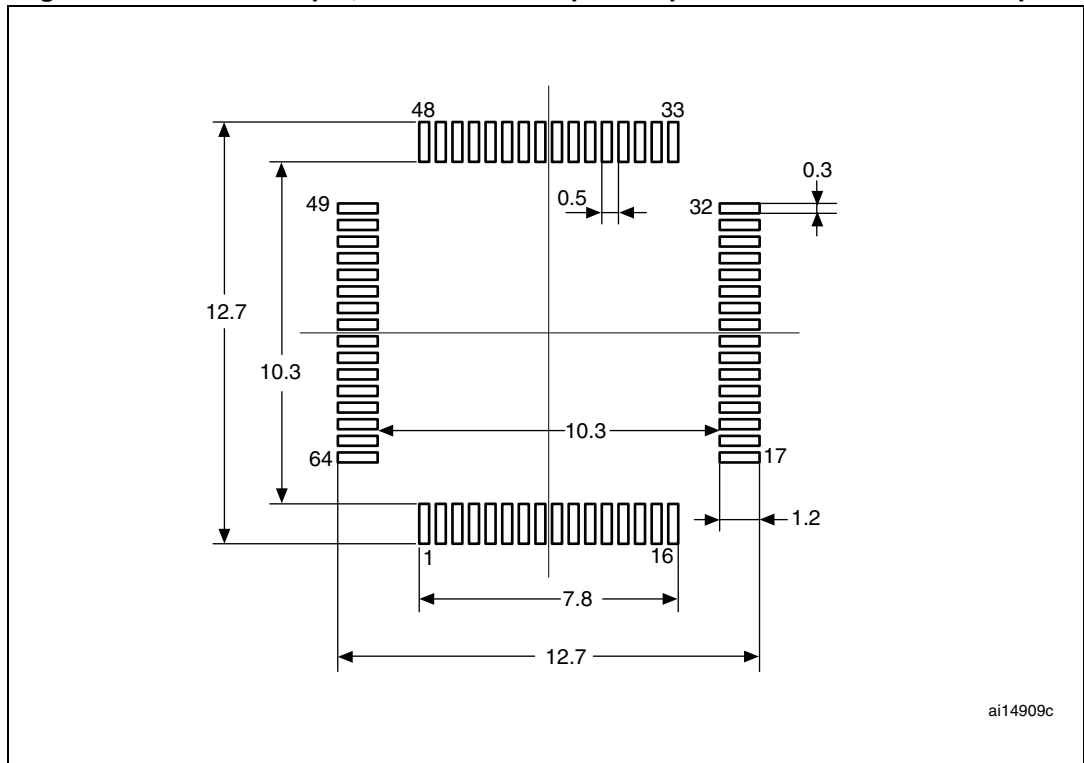
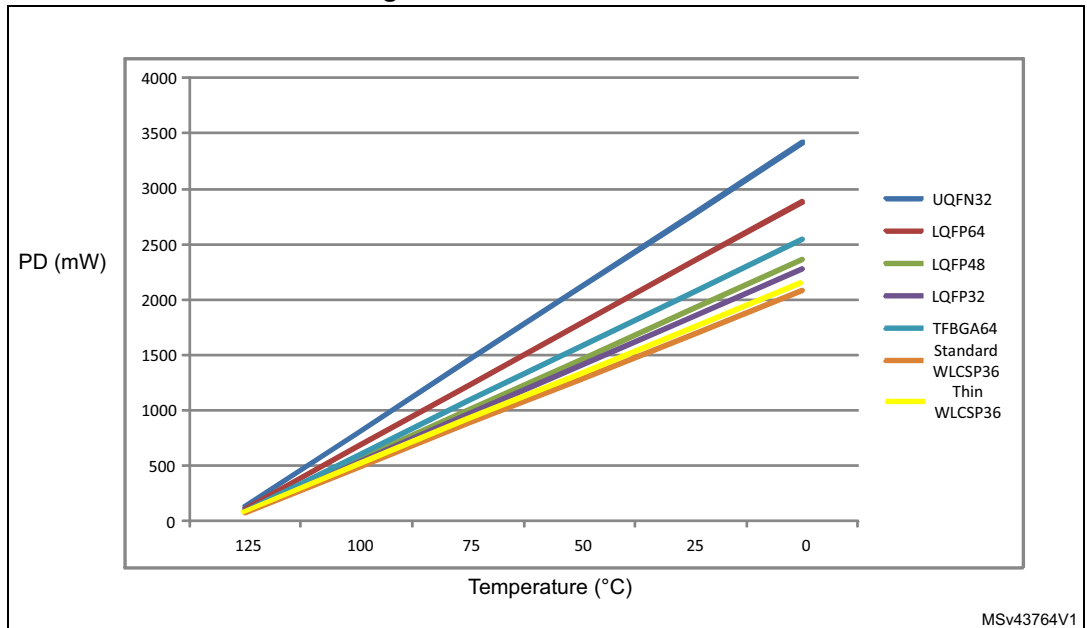


Figure 40. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint

1. Dimensions are expressed in millimeters.

Figure 59. Thermal resistance



7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 93. Document revision history (continued)

Date	Revision	Changes
05-Sep-2014	4	<p>Extended operating temperature range to 125 °C.</p> <p>Updated minimum ADC operating voltage to 1.65 V.</p> <p>Changed number of I2S interface from 1 to 0 in Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts.</p> <p>Replaced USART3 by LPUART1 in Table 16: STM32L052x6/8 pin definitions and LPUART by LPUART1 in Table 17: Alternate function port A, Table 18: Alternate function port B, Table 19: Alternate function port C, Table 20: Alternate function port D and Table 21: Alternate function port H. Updated PA6 in Table 17: Alternate function port A.</p> <p>Updated temperature range in Section 1: Description, Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts.</p> <p>Updated P_D, T_A and T_J to add range 3 in Table 25: General operating conditions. Added range 3 in Table 53: Flash memory and data EEPROM endurance and retention, Table 92: STM32L052x6/8 ordering information scheme. Update note 1 in Table 29: Current consumption in Run mode, code with data processing running from Flash, Table 31: Current consumption in Run mode, code with data processing running from RAM, Table 33: Current consumption in Sleep mode, Table 34: Current consumption in Low-power run mode, Table 34: Current consumption in Low-power run mode, Table 36: Typical and maximum current consumptions in Stop mode, Table 37: Typical and maximum current consumptions in Standby mode and Table 41: Low-power mode wakeup timings. Updated Figure 59: Thermal resistance and removed note 1. Updated Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS, Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive, Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF.</p> <p>Updated Table 37: Typical and maximum current consumptions in Standby mode.</p> <p>Updated SYSCFG in Table 39: Peripheral current consumption in Run or Sleep mode.</p> <p>Updated Table 40: Peripheral current consumption in Stop and Standby mode and Table 43: Low-speed external user clock characteristics.</p> <p>Updated ACC_{HSI16} temperature conditions in Table 46: 16 MHz HSI16 oscillator characteristics. Changed ambient temperature range in note 1 below Table 47: HSI48 oscillator characteristics.</p> <p>Updated $V_{F(NRST)}$ and $V_{NF(NRST)}$ in Table 62: NRST pin characteristics.</p> <p>Updated Table 63: ADC characteristics and Table 65: ADC accuracy.</p> <p>Added range 3 in Table 92: STM32L052x6/8 ordering information scheme.</p>