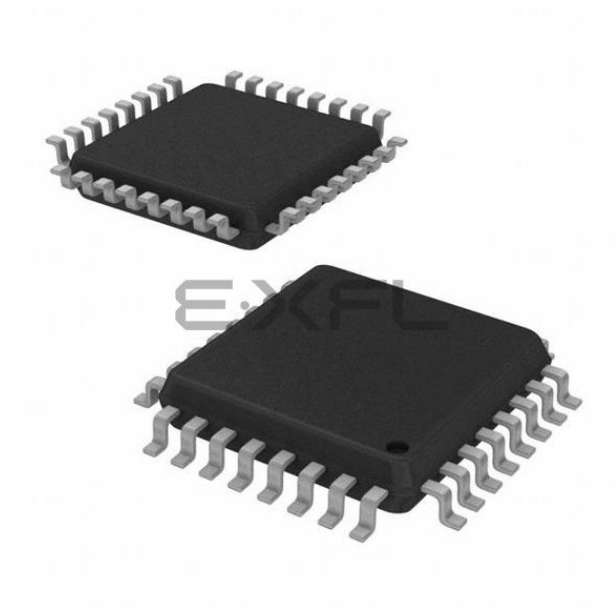

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052k8t6

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L052x6/8 support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

  Stop mode with RTC

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USB/USART/I2C/LPUART/LPTIMER wakeup events.

3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

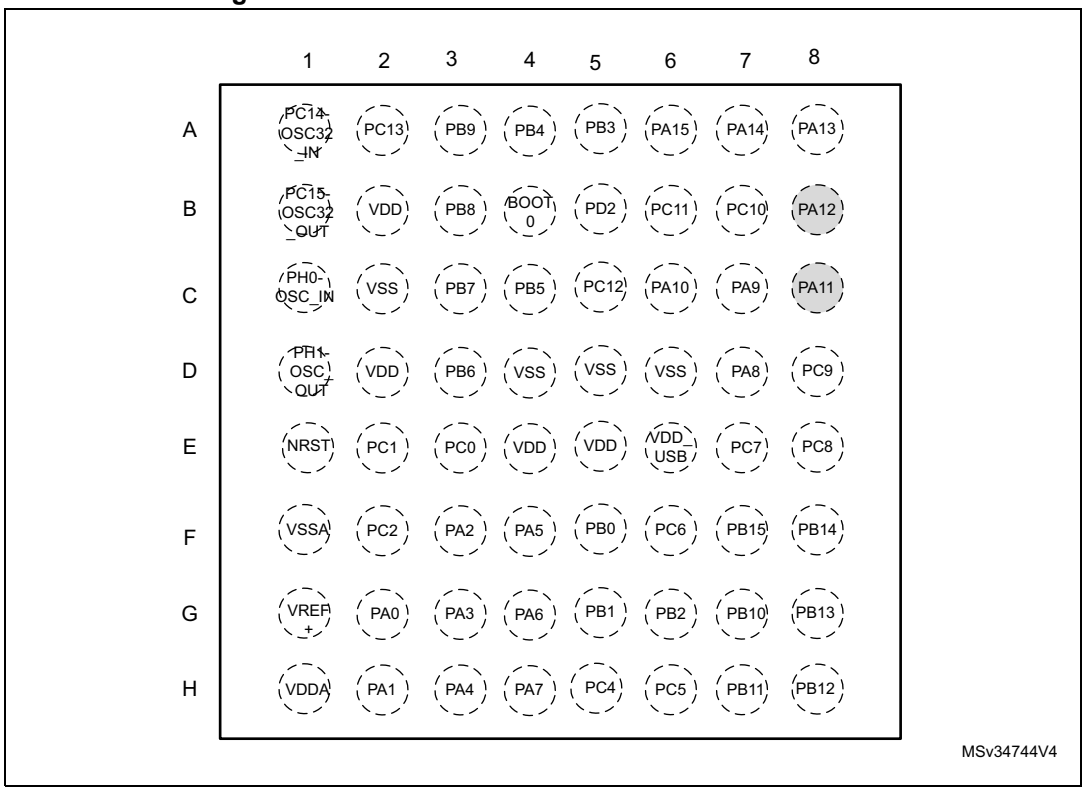
3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USB, USARTs, LPUART, LPTIMER or comparator events.

Figure 4. STM32L052x6/8 TFBGA64 ballout - 5x 5 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 15. Legend/abbreviations used in the pinout table

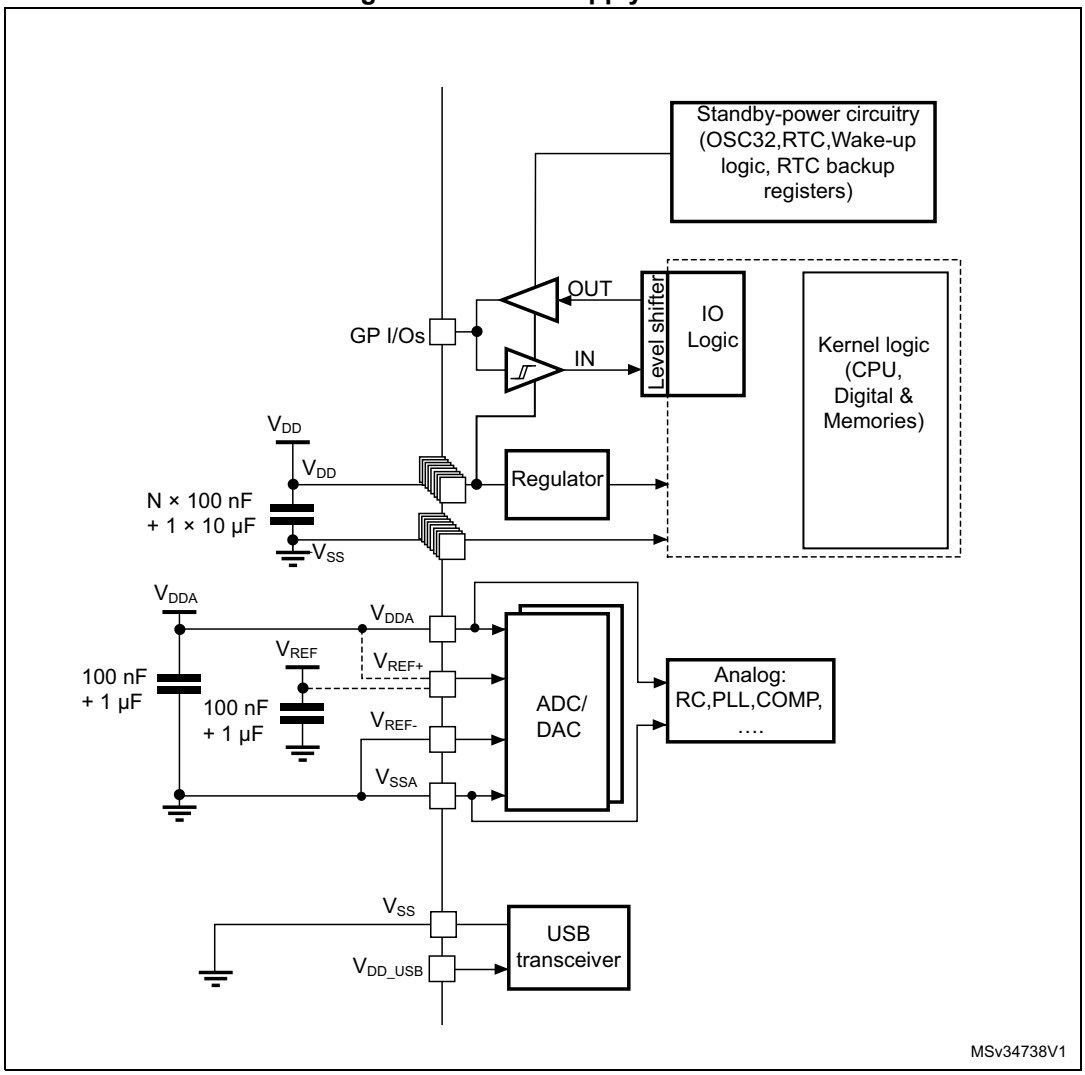
Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 16. STM32L052x6/8 pin definitions

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36[1]	LQFP48	LQFP64	TFBGA64						
-	-	-	1	1	B2	VDD	S	-	-	-	-
-	-	-	2	2	A2	PC13	I/O	FT	-	-	RTC_TAMP1/ RTC_TS/RTC _OUT/WKUP2
2	2	A6	3	3	A1	PC14-OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
3	3	B6	4	4	B1	PC15-OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT

6.1.6 Power supply scheme

Figure 12. Power supply scheme



6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme

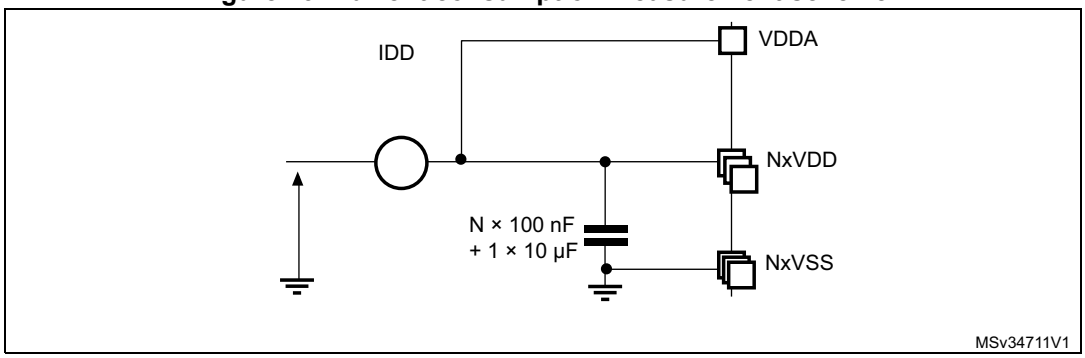


Table 23. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD} (2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS} (2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	
ΣI_{VDD_USB}	Total current into V_{DD_USB} power lines (source)	25	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2)	90	
	Total output current sunk by PA11 and PA12	25	
	Total output current sourced by sum of all IOs and control pins(2)	-90	
$I_{INJ(PIN)}$	Injected current on FT, FTf, RST and B pins	-5/+0(3)	
	Injected current on TC pin	± 5(4)	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 22* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 22: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 24. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 34. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Run)	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched off, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK} = 32 kHz	T_A = − 40 to 25°C	8.5	10	µA
				T_A = 85 °C	11.5	48	
				T_A = 105 °C	15.5	53	
				T_A = 125 °C	27.5	130	
			MSI clock= 65 kHz, f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	10	15	
				T_A = 85 °C	15.5	50	
				T_A = 105 °C	19.5	54	
				T_A = 125 °C	31.5	130	
			MSI clock= 131 kHz, f_{HCLK} = 131 kHz	T_A = − 40 to 25°C	20	25	
				T_A = 55 °C	23	50	
				T_A = 85 °C	25.5	55	
				T_A = 105 °C	29.5	64	
				T_A = 125 °C	40	140	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock= 65 kHz, f_{HCLK} = 32 kHz	T_A = − 40 to 25°C	22	28	
				T_A = 85 °C	26	68	
				T_A = 105 °C	31	75	
				T_A = 125 °C	44	95	
			MSI clock = 65 kHz, f_{HCLK} = 65 kHz	T_A = − 40 to 25°C	27.5	33	
				T_A = 85 °C	31.5	73	
				T_A = 105 °C	36.5	80	
				T_A = 125 °C	49	100	
			MSI clock = 131 kHz, f_{HCLK} = 131 kHz	T_A = − 40 to 25°C	39	46	
				T_A = 55 °C	41	80	
				T_A = 85 °C	44	86	
				T_A = 105 °C	49.5	100	
				T_A = 125 °C	60	120	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Table 63. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ADC}(3)(4)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)(5)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$(6)	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 16 MHz	0.266			µs
		$f_{ADC} = f_{PCLK}/2$	8.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 8 MHz	0.516			µs
		$f_{ADC} = f_{PCLK}/4$	16.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16}$ = 16 MHz	0.252	-	0.260	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI16}$	-	1	-	$1/f_{HSI16}$
t_S(3)	Sampling time	f_{ADC} = 16 MHz	0.093	-	10.03	µs
		-	1.5	-	160.5	$1/f_{ADC}$
t_{UP_LDO}(3)(5)	Internal LDO power-up time	-	-	-	10	µs
t_{STAB}(3)(5)	ADC stabilization time	-	14			$1/f_{ADC}$
t_{ConV}(3)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz, 12-bit resolution	0.875	-	10.81	µs
		12-bit resolution	14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

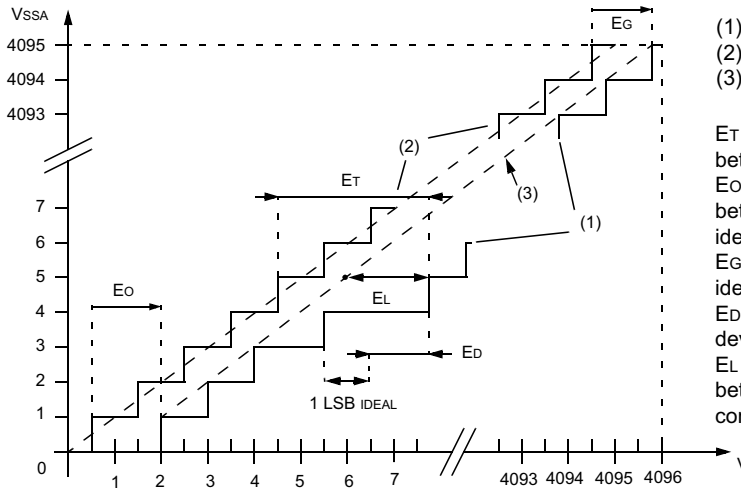
1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to *Table 64: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 39: Peripheral current consumption in Run or Sleep mode*).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 64: RAIN max for fADC = 16 MHz*.
5. This parameter only includes the ADC timing. It does not take into account register access latency.
6. This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

Table 65. ADC accuracy(1)(2)(3) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{REF+} < V_{DDA} < 3.6 V, range 1/2/3	-	2	5	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	3	
ED	Differential linearity error		-	1	2	
ENOB	Effective number of bits		10.0	11.0	-	bits
SINAD	Signal-to-noise distortion		62	69	-	dB
SNR	Signal-to-noise ratio		61	69	-	
THD	Total harmonic distortion		-	-85	-65	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 28. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Table 75. SPI characteristics in voltage Range 2 (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	-	8	MHz
		Slave mode Transmitter $1.65<V_{DD}<3.6V$			8	
		Slave mode Transmitter $2.7<V_{DD}<3.6V$			8(2)	
$Duty_{(SCK)}$	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	4*Tpclk	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	2*Tpclk	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	Tpclk-2	Tpclk	Tpclk+2	
$t_{su(MI)}$	Data input setup time	Master mode	0	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	11	-	-	
$t_{h(SI)}$		Slave mode	4.5	-	-	
$t_{a(SO}$	Data output access time	Slave mode	18	-	52	
$t_{dis(SO)}$	Data output disable time	Slave mode	12	-	42	
$t_{v(SO)}$	Data output valid time	Slave mode	-	20	56.5	
$t_{v(MO)}$		Master mode	-	5	9	
$t_{h(SO)}$	Data output hold time	Slave mode	13	-	-	
$t_{h(MO)}$		Master mode	3	-	-	

1. Guaranteed by characterization results.
2. The maximum SPI clock frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

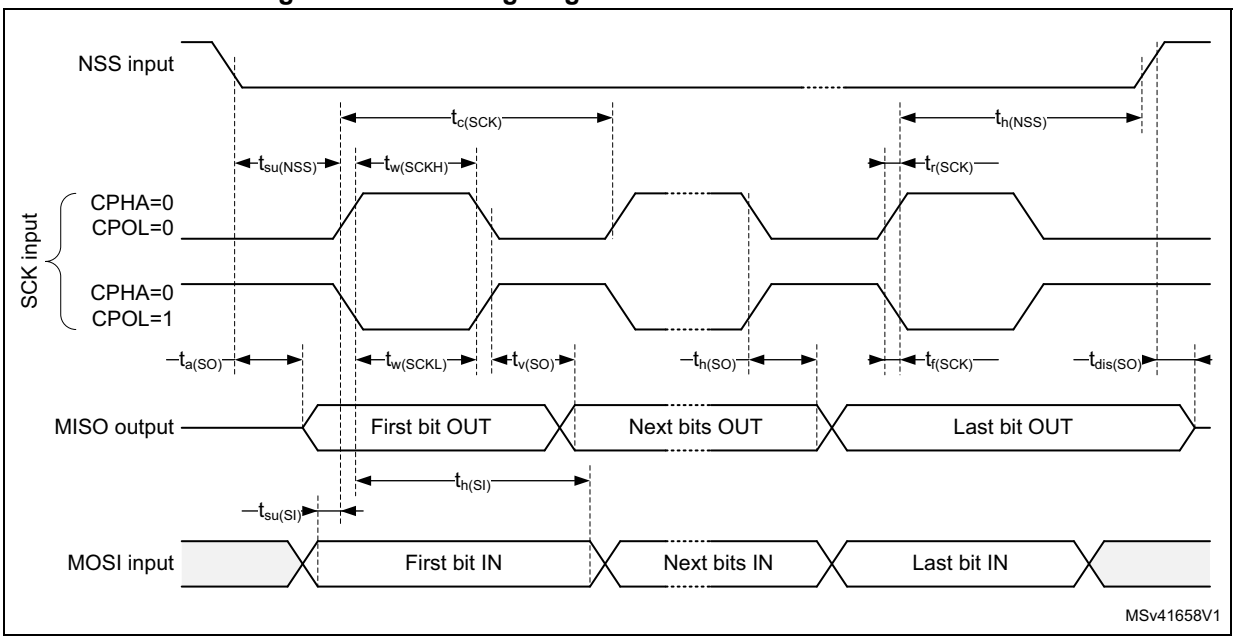
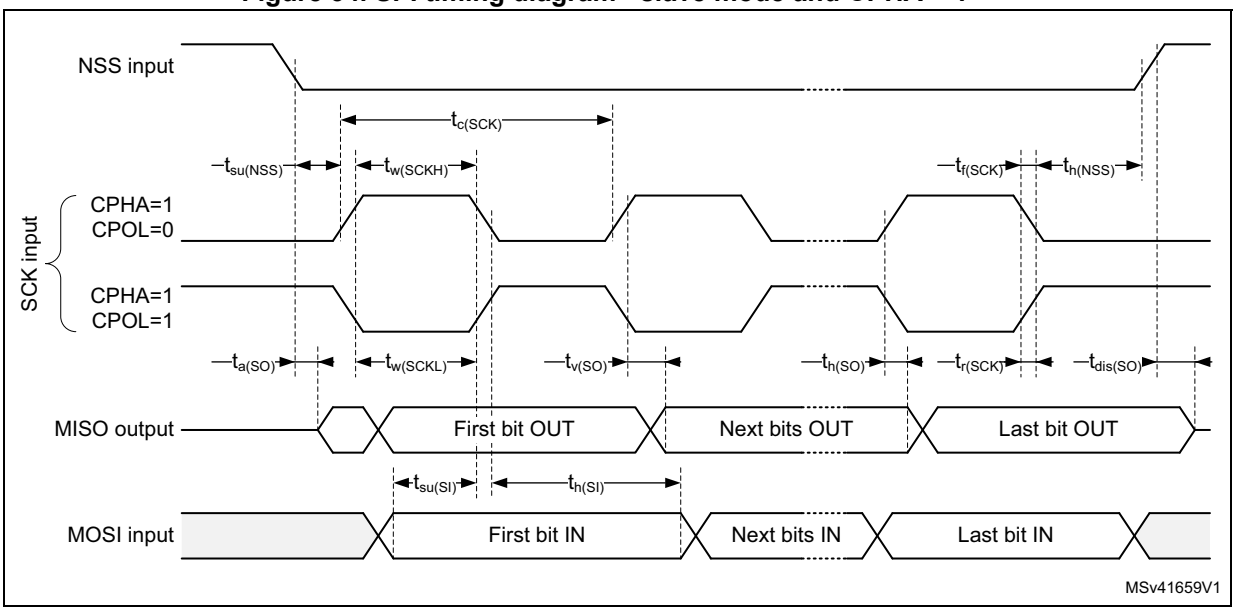


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 78. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

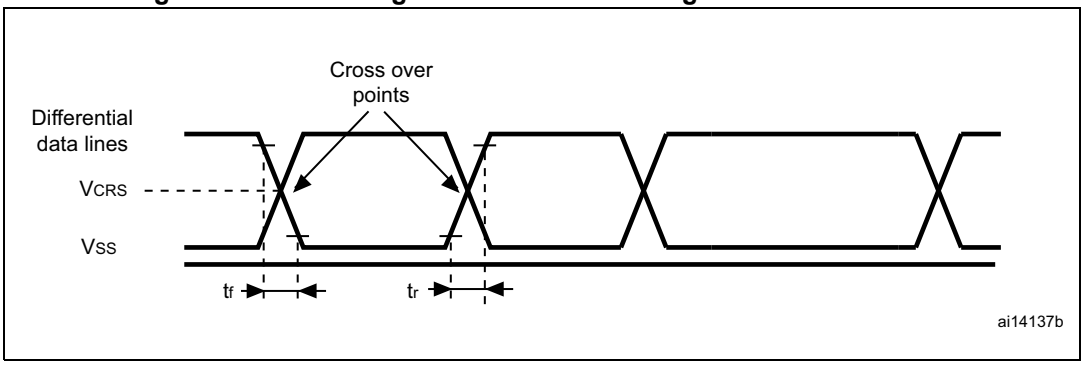
1. Guaranteed by design.

Table 79. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

Figure 38. USB timings: definition of data signal rise and fall time

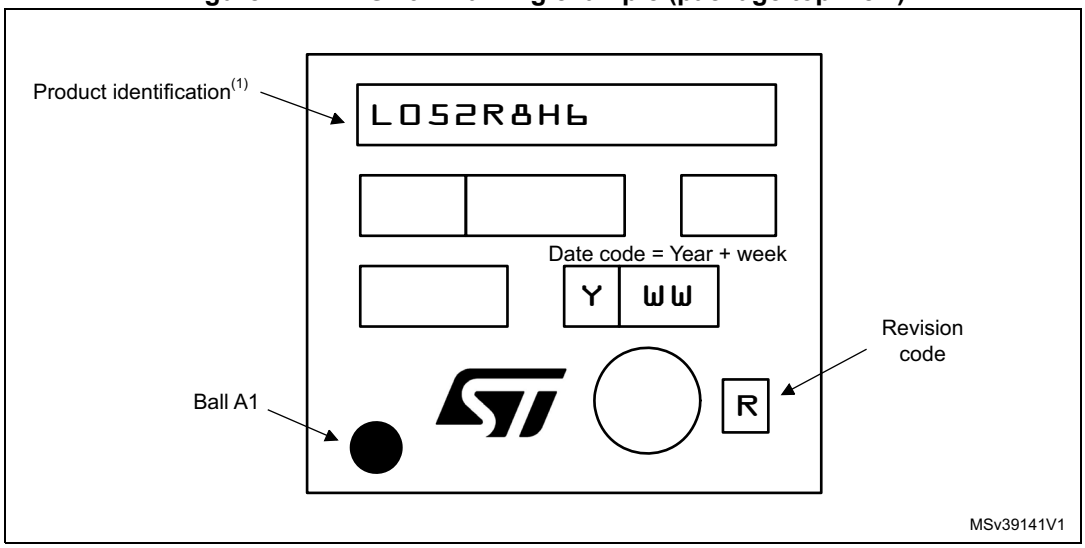


Device marking for TFBGA64

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

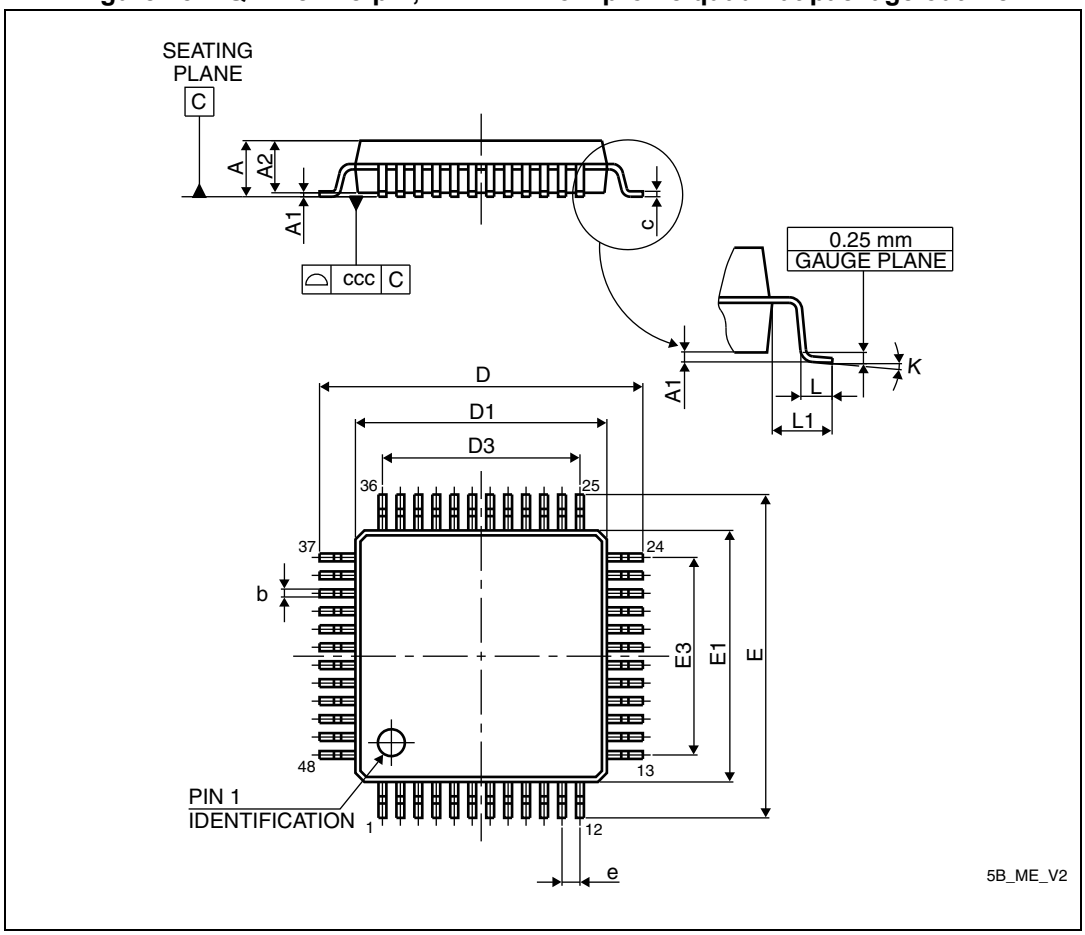
Figure 44. TFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.3 LQFP48 package information

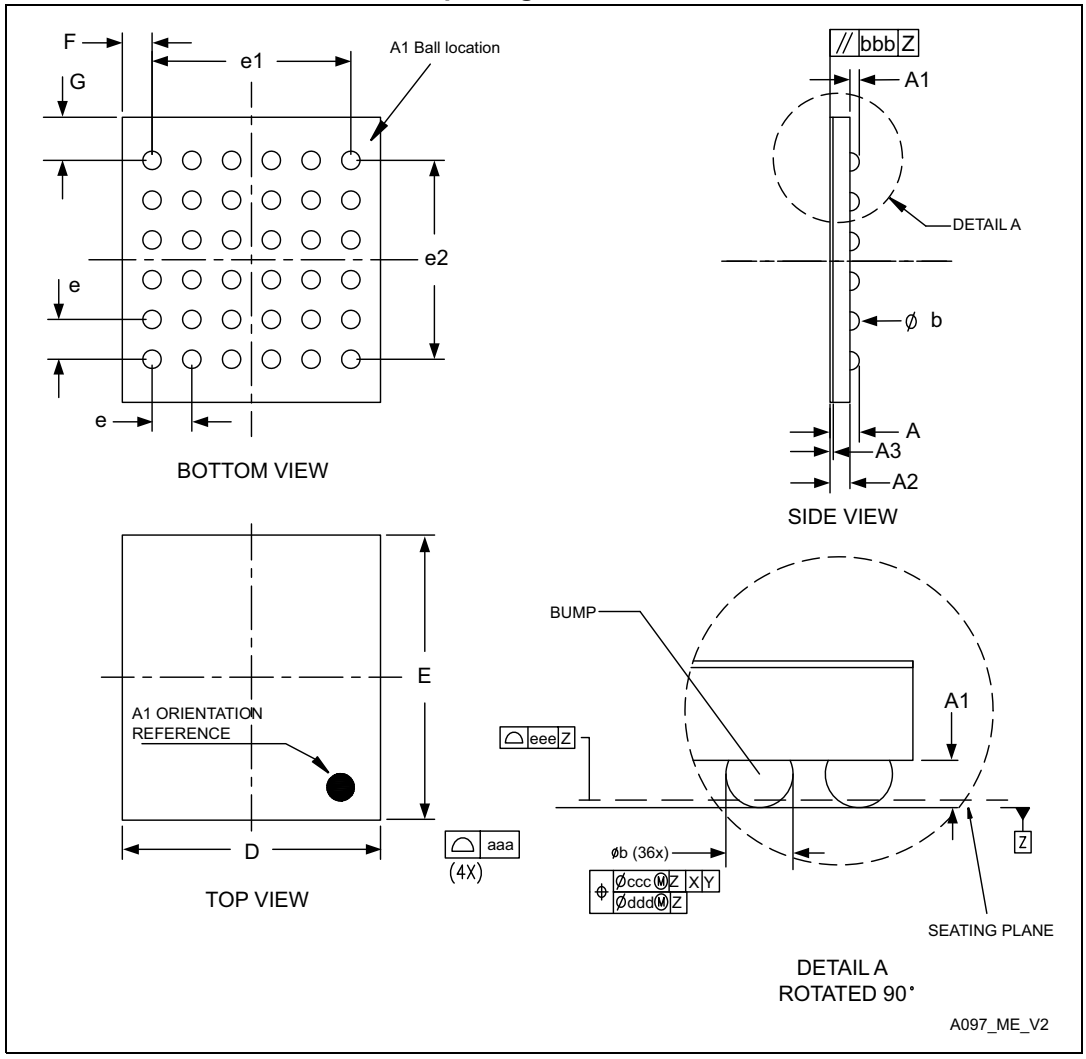
Figure 45. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.5 Thin WLCSP36 package information

Figure 51. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline



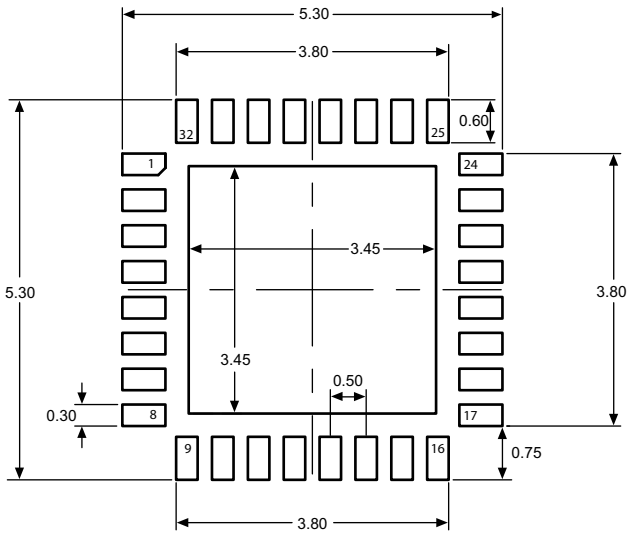
1. Drawing is not to scale.
2. b dimensions is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 90. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 57. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint



1. Dimensions are expressed in millimeters.

9 Revision history

Table 93. Document revision history

Date	Revision	Changes
27-Feb-2014	1	Initial release.
29-Apr-2014	2	Added WLCSP36 package. Updated *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts* Updated *Figure 4: STM32L052x6/8 TFBGA64 ballout - 5x 5 mm*. Updated *Table 5: Functionalities depending on the working mode (from Run/active down to standby)*. Added *Section 3.2: Interconnect matrix*. Replaced TTa I/O structure by TC, updated PA0/4/5, PC5/14, BOOT0 and NRST I/O structure, and added note 3 in *Table 16: STM32L052x6/8 pin definitions*. Updated *Table 25: General operating conditions*, *Table 22: Voltage characteristics* and *Table 23: Current characteristics*. Modified conditions in *Table 28: Embedded internal reference voltage*. Updated *Table 29: Current consumption in Run mode, code with data processing running from Flash*, *Table 31: Current consumption in Run mode, code with data processing running from RAM*, *Table 33: Current consumption in Sleep mode*, *Table 34: Current consumption in Low-power run mode*, *Table 35: Current consumption in Low-power sleep mode*, and *Table 36: Typical and maximum current consumptions in Stop modeTable 37: Typical and maximum current consumptions in Standby mode*. Added *Figure 14: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS*, *Figure 15: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS*, *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 44: HSE oscillator characteristics* and *Table 45: LSE oscillator characteristics*. Added *Figure 23: HSI16 minimum and maximum value versus temperature*. Updated *Table 56: ESD absolute maximum ratings*, *Table 58: I/O current injection susceptibility* and *Table 59: I/O static characteristics*, and added *Figure 24: VIH/VIL versus VDD (CMOS I/Os)* and *Figure 25: VIH/VIL versus VDD (TTL I/Os)*. Updated *Table 60: Output voltage characteristics*, *Table 61: I/O AC characteristics*, and *Figure 26: I/O AC characteristics definition*. Updated *Table 63: ADC characteristics*, *Table 65: ADC accuracy*, and *Figure 29: Typical connection diagram using the ADC*. Updated *Table 68: Temperature sensor characteristics*. Updated *Table 74: SPI characteristics in voltage Range 1* and *Table 77: I2S characteristics*. Added *Figure 59: Thermal resistance*.

Table 93. Document revision history (continued)

Date	Revision	Changes
11-Mar-2016	6	Updated number of SPIs on cover page and in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Changed minimum comparator supply voltage to 1.65 V on cover page. Added number of fast and standard channels in *Section 3.11: Analog-to-digital converter (ADC)*. Updated *Section 3.18.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.18.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.18.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.18.3: Low-power universal asynchronous receiver transmitter (LPUART)*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated *Table 58: I/O current injection susceptibility*. Updated *Figure 6: STM32L052x6/8 WLCSP36 ballout*, *Figure 8: STM32L052x6/8 UFQFPN32 pinout* removing grey PA11, PA12 pins and removing note 2. Updated *Table 55: EMI characteristics*. Changed temperature condition in *Table 8: Internal voltage reference measured values* and *Table 27: Embedded internal reference voltage calibration values*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 63: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note 1 Added note 4 related to R_{ADC}. Updated f_{TRIG}. Updated t_S and t_{CONV}. – Updated equation 1 description. – Updated *Table 64: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. Updated R_O and added Note 2 in *Table 66: DAC characteristics*. Added *Table 73: USART/LPUART characteristics*. Updated *Figure 47: LQFP48 marking example (package top view)*.

Table 93. Document revision history (continued)

Date	Revision	Changes
07-Mar-2017	7	Added thin WLCSP36 package. Updated number of I2S interfaces and removed I2S for STM32L052T8 in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. In *Section 4: Pin descriptions*, renamed USB_OE into USB_NOE. Added mission profile compliance with JEDEC JESD47 in *Section 6.2: Absolute maximum ratings*. Added note 2. related to the position of the external capacitor below *Figure 27: Recommended NRST pin protection*. Updated R_L in *Table 63: ADC characteristics*. Updated *Figure 32: 12-bit buffered/non-buffered DAC* and added note below figure. Updated t_{AF} maximum value for range 1 in *Table 72: I2C analog filter characteristics*. Updated $t_{WUUSART}$ description in *Table 73: USART/LPUART characteristics*. NSS timing waveforms updated in *Figure 33: SPI timing diagram - slave mode and CPHA = 0* and *Figure 34: SPI timing diagram - slave mode and CPHA = 1(1)*. Previous WLCSP36 package renamed “Standard” WLCSP36; added Note *2.* below *Figure 48: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline* and updated *Table 85: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data*. Added reference to optional marking or inset/upset marks in all package device marking sections.