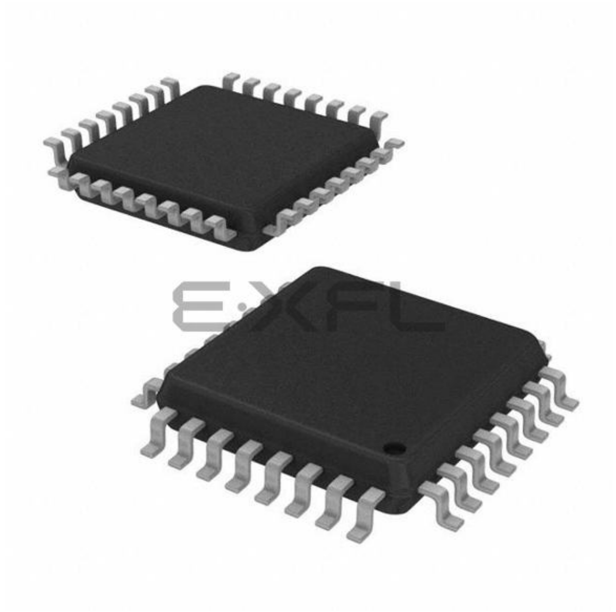
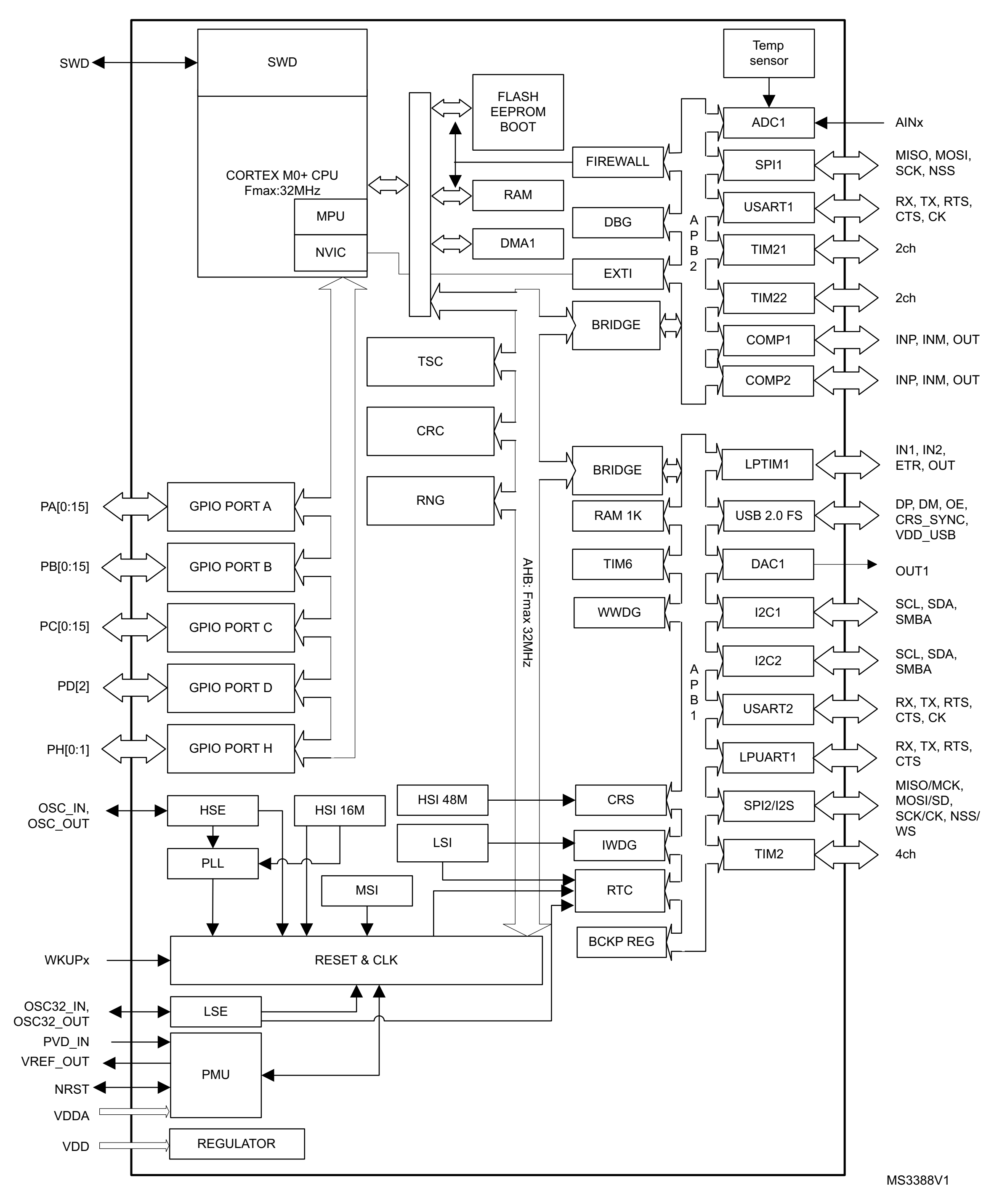


Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052k8t7

Figure 1. STM32L052x6/8 block diagram



3.2 Interconnect matrix

Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 6. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	CRS/HSI48	the clock recovery system trims the HSI48 based on USB SOF	Y	Y	-	-	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC,DAC	Conversion trigger	Y	Y	Y	Y	-

3.4 Reset and supply management

3.4.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, DAC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{DD_USB} = 1.65 to 3.6V: external power supply for USB transceiver, USB_DM (PA11) and USB_DP (PA12). To guarantee a correct voltage level for USB communication V_{DD_USB} must be above 3.0V. If USB is not used this pin must be tied to V_{DD}.

3.4.2 Power supply supervisor

The devices have an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

Two versions are available:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the VDD min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the power ramp-up should guarantee that 1.65 V is reached on V_{DD} at least 1 ms after it exits the POR area.

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Stop mode, it is possible to automatically switch off the internal reference voltage (V_{REFINT}) in Stop mode. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for any external reset circuit.

Note: The start-up time at power-on is typically 3.3 ms when BOR is active at power-up, the start-up time at power-on can be decreased down to 1 ms typically for devices with BOR inactive at power-up.

The devices feature an embedded programmable voltage detector (PVD) that monitors the $V_{DD/VDDA}$ power supply and compares it to the V_{PVD} threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD/VDDA}$ drops below the V_{PVD} threshold and/or when $V_{DD/VDDA}$ is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.10 Direct memory access (DMA)

The flexible 7-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, LPUART, general-purpose timers, DAC, and ADC.

3.11 Analog-to-digital converter (ADC)

A native 12-bit, extended to 16-bit through hardware oversampling, analog-to-digital converter is embedded into STM32L052x6/8 device. It has up to 16 external channels and 3 internal channels (temperature sensor, voltage reference). Three channels, PA0, PA4 and PA5, are fast channels, while the others are standard channels.

The ADC performs conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC frequency is independent from the CPU frequency, allowing maximum sampling rate of 1.14 MSPS even with a low CPU speed. The ADC consumption is low at all frequencies (~25 µA at 10 kSPS, ~200 µA at 1MSPS). An auto-shutdown function guarantees that the ADC is powered off except during the active conversion phase.

The ADC can be served by the DMA controller. It can operate from a supply voltage down to 1.65 V.

The ADC features a hardware oversampler up to 256 samples, this improves the resolution to 16 bits (see AN2668).

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.12 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

Table 9. Capacitive sensing GPIOs available on STM32L052x6/8 devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	5	TSC_G5_IO1	PB3
	TSC_G1_IO2	PA1		TSC_G5_IO2	PB4
	TSC_G1_IO3	PA2		TSC_G5_IO3	PB6
	TSC_G1_IO4	PA3		TSC_G5_IO4	PB7
2	TSC_G2_IO1	PA4(1)	6	TSC_G6_IO1	PB11
	TSC_G2_IO2	PA5		TSC_G6_IO2	PB12
	TSC_G2_IO3	PA6		TSC_G6_IO3	PB13
	TSC_G2_IO4	PA7		TSC_G6_IO4	PB14
3	TSC_G3_IO1	PC5	7	TSC_G7_IO1	PC0
	TSC_G3_IO2	PB0		TSC_G7_IO2	PC1
	TSC_G3_IO3	PB1		TSC_G7_IO3	PC2
	TSC_G3_IO4	PB2		TSC_G7_IO4	PC3
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PC6
	TSC_G4_IO2	PA10		TSC_G8_IO2	PC7
	TSC_G4_IO3	PA11		TSC_G8_IO3	PC8
	TSC_G4_IO4	PA12		TSC_G8_IO4	PC9

1. This GPIO offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

3.17 Timers and watchdogs

The ultra-low-power STM32L052x6/8 devices include three general-purpose timers, one low- power timer (LPTIM), one basic timer, two watchdog timers and the SysTick timer.

Table 10 compares the features of the general-purpose and basic timers.

Table 10. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM21, TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Each I2C interface can be served by the DMA controller.

Refer to *Table 12* for an overview of I2C interface features.

Table 12. STM32L052x6/8 I^{2}C implementation

I2C features[(1)]	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X[(2)]
Independent clock	X	-
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.
2. See for the list of I/Os that feature Fast Mode Plus capability

3.18.2 Universal synchronous/asynchronous receiver transmitter (USART)

The two USART interfaces (USART1, USART2) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. They also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

Table 13 for the supported modes and features of USART interfaces.

Table 13. USART implementation

USART modes/features[(1)]	USART1 and USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode[(2)]	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X

Table 18. Alternate function port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6
		SPI1/SPI2/I2S2/ USART1/ EVENTOUT/	**I2C1**	**LPUART1/LPTIM /TIM2/SYS_AF/ EVENTOUT**	**I2C1/TSC**	**I2C1/TIM22/ EVENTOUT/ LPUART1**	**SPI2/I2S2/I2C2**	**I2C2/TIM21/ EVENTOUT**
Port B	PB0	EVENTOUT	-	-	TSC_G3_IO2	-	-	-
	PB1	-	-	-	TSC_G3_IO3	LPUART1_RTS_ DE	-	-
	PB2	-	-	LPTIM1_OUT	TSC_G3_IO4	-	-	-
	PB3	SPI1_SCK	-	TIM2_CH2	TSC_G5I_O1	EVENTOUT	-	-
	PB4	SPI1_MISO	-	EVENTOUT	TSC_G5_IO2	TIM22_CH1	-	-
	PB5	SPI1_MOSI	-	LPTIM1_IN1	I2C1_SMBA	TIM22_CH2	-	-
	PB6	USART1_TX	I2C1_SCL	LPTIM1_ETR	TSC_G5_IO3	-	-	-
	PB7	USART1_RX	I2C1_SDA	LPTIM1_IN2	TSC_G5_IO4	-	-	-
	PB8	-	-	-	TSC_SYNC	I2C1_SCL	-	-
	PB9	-	-	EVENTOUT	-	I2C1_SDA	SPI2_NSS/I2S2_ WS	-
	PB10	-	-	TIM2_CH3	TSC_SYNC	LPUART1_TX	SPI2_SCK	I2C2_SCL
	PB11	EVENTOUT	-	TIM2_CH4	TSC_G6_IO1	LPUART1_RX		I2C2_SDA
	PB12	SPI2_NSS/I2S2_WS	-	LPUART1_RTS_ DE	TSC_G6_IO2	-	I2C2_SMBA	EVENTOUT
	PB13	SPI2_SCK/I2S2_CK	-	-	TSC_G6_IO3	LPUART1_CTS	I2C2_SCL	TIM21_CH1
	PB14	SPI2_MISO/I2S2_MCK	-	RTC_OUT	TSC_G6_IO4	LPUART1_RTS_ DE	I2C2_SDA	TIM21_CH2
	PB15	SPI2_MOSI/I2S2_SD	-	RTC_REFIN	-	-	-	-

Table 19. Alternate function port C

Port		AF0	AF1	AF2	AF3
		LPUART1/LPTIM/ TIM21/12/ EVENTOUT/	-	SPI2/I2S2/USB/ LPUART1/ EVENTOUT	TSC
Port C	PC0	LPTIM1_IN1	-	EVENTOUT	TSC_G7_IO1
	PC1	LPTIM1_OUT	-	EVENTOUT	TSC_G7_IO2
	PC2	LPTIM1_IN2	-	SPI2_MISO/I2S2_MCK	TSC_G7_IO3
	PC3	LPTIM1_ETR	-	SPI2_MOSI/I2S2_SD	TSC_G7_IO4
	PC4	EVENTOUT	-	LPUART1_TX	-
	PC5	-	-	LPUART1_RX	TSC_G3_IO1
	PC6	TIM22_CH1	-	-	TSC_G8_IO1
	PC7	TIM22_CH2	-	-	TSC_G8_IO2
	PC8	TIM22_ETR	-	-	TSC_G8_IO3
	PC9	TIM21_ETR	-	USB_NOE	TSC_G8_IO4
	PC10	LPUART1_TX	-	-	-
	PC11	LPUART1_RX	-	-	-
	PC12	-	-	-	-
	PC13	-	-	-	-
	PC14	-	-	-	-
	PC15	-	-	-	-

5 Memory mapping

Figure 9. Memory map

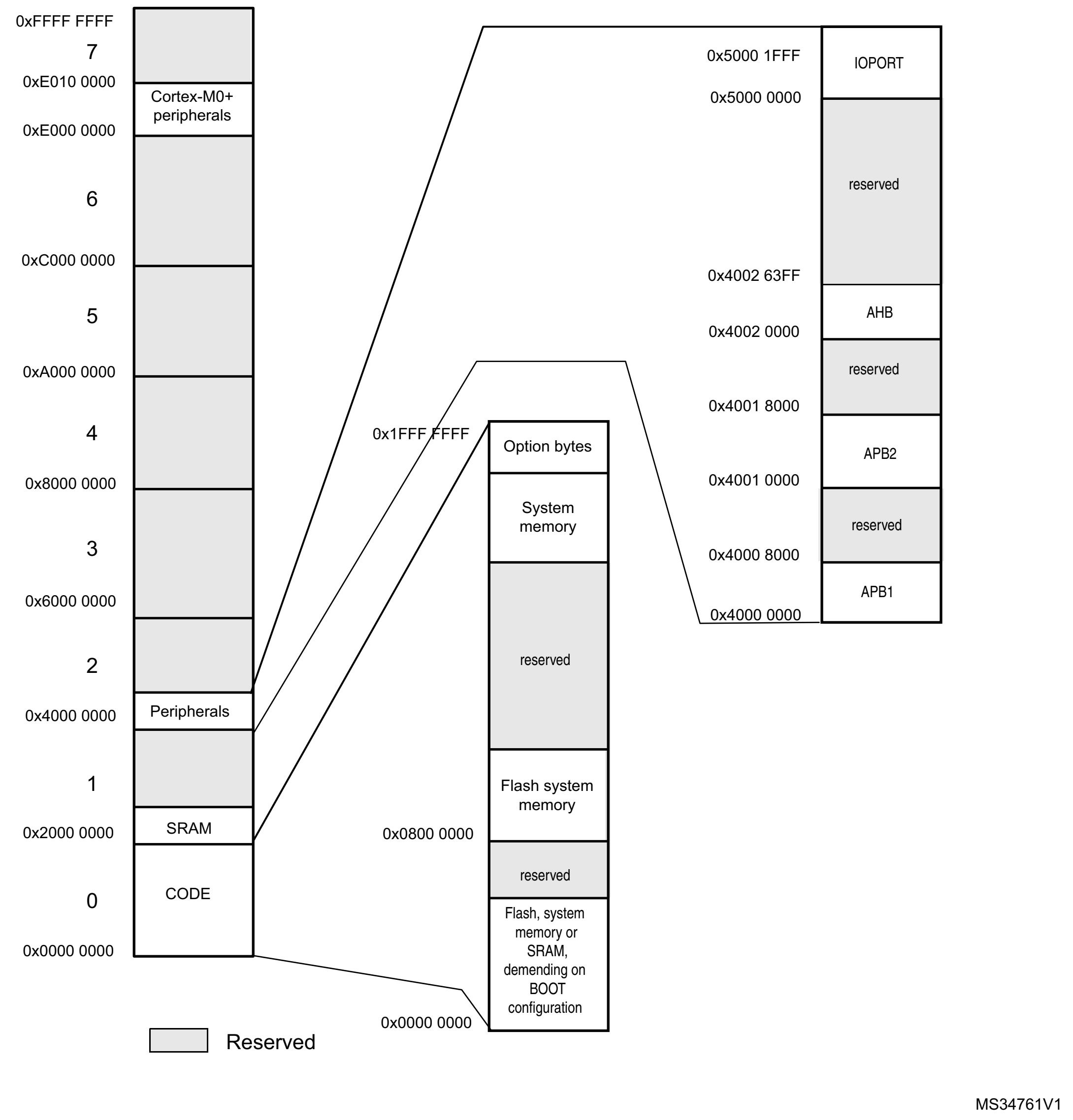


Table 26. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.
2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in *Table 28* are based on characterization results, unless otherwise specified.

Table 27. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA}= 3 V	0x1FF8 0078 - 0x1FF8 0079

Table 28. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{REFINT out}}$(2)	Internal reference voltage	$-40\ °C < T_J < +125\ °C$	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value(3)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(4)	Temperature coefficient	$-40\ °C < T_J < +125\ °C$	-	25	100	ppm/°C
A_{Coeff}(4)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(4)	Voltage coefficient	$3.0\ V < V_{DDA} < 3.6\ V$	-	-	2000	ppm/V
$T_{S\_vrefint}$(4)(5)	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
T_{ADC_BUF}(4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(4)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(4)	VREF_OUT output current(6)	-	-	-	1	µA
C_{VREF_OUT}(4)	VREF_OUT output load	-	-	-	50	pF

Table 29. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max[1]	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)[2]	Range 3, V_{CORE}=1.2 V VOS[1:0]=11	1 MHz	165	230	µA
				2 MHz	290	360	
				4 MHz	555	630	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	4 MHz	0.665	0.74	mA
				8 MHz	1.3	1.4	
				16 MHz	2.6	2.8	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.55	1.7	
				16 MHz	3.1	3.4	
				32 MHz	6.3	6.8	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	36.5	110	µA
				524 kHz	99.5	190	
				4.2 MHz	620	700	
		HSI clock	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	16 MHz	2.6	2.9	mA
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	6.25	7	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 30. Current consumption in Run mode vs code type, code with data processing running from Flash

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)[1]	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	555	µA
				CoreMark		585	
				Fibonacci		440	
				while(1)		355	
				while(1), prefetch OFF		353	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6.3	mA
				CoreMark		6.3	
				Fibonacci		6.55	
				while(1)		5.4	
				while(1), prefetch OFF		5.2	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 39. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		283	225	222.5	212.5	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), f_{APB1} = f_{HCLK}, f_{APB2} = f_{HCLK}, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 µA.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 1 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

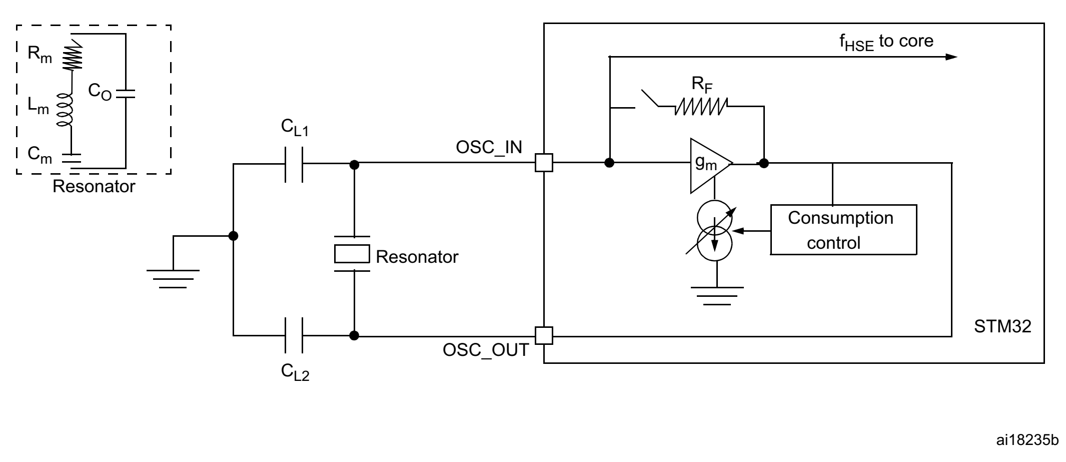
Table 44. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		25	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
G_m	Maximum critical crystal transconductance	Startup	-	-	700	µA /V
$t_{SU(HSE)}$(2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Guaranteed by characterization results. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 21. HSE oscillator circuit diagram



High-speed internal 48 MHz (HSI48) RC oscillator

Table 47. HSI48 oscillator characteristics[(1)]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency		-	48	-	MHz
TRIM	HSI48 user-trimming step		0.09[(2)]	0.14	0.2[(2)]	%
$DuCy_{(HSI48)}$	Duty cycle		45[(2)]	-	55[(2)]	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator (factory calibrated before CRS calibration)	T_A = 25 °C	-4[(3)]	-	4[(3)]	%
$t_{su(HSI48)}$	HSI48 oscillator startup time		-	-	6[(2)]	µs
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption		-	330	380[(2)]	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 48. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}[(1)]	LSI frequency	26	38	56	kHz
D_{LSI}[(2)]	LSI oscillator frequency drift 0°C ≤T_A ≤ 85°C	-10	-	4	%
$t_{su(LSI)}$[(3)]	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}$[(3)]	LSI oscillator power consumption	-	400	510	nA

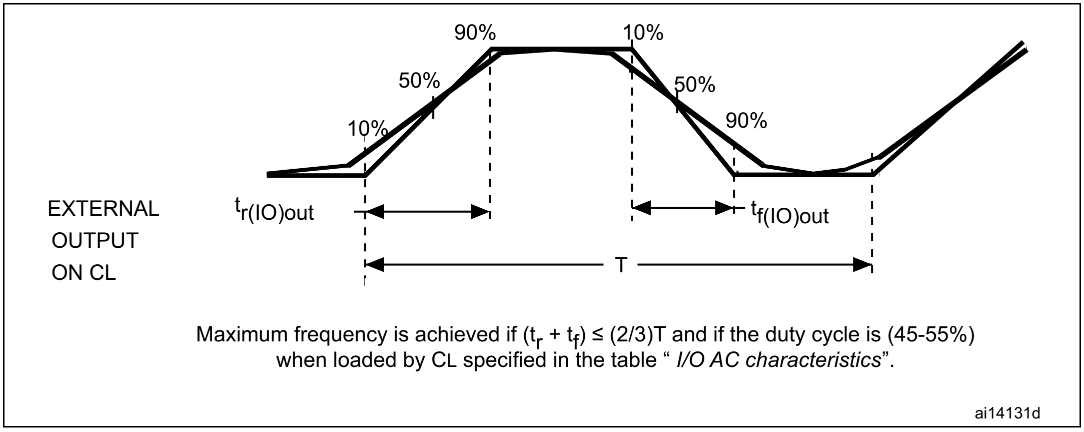
1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Multi-speed internal (MSI) RC oscillator

Table 49. MSI oscillator characteristics

Symbol	Parameter	Condition	Typ	Max	Unit
f_{MSI}	Frequency after factory calibration, done at V_{DD}= 3.3 V and T_A = 25 °C	MSI range 0	65.5	-	kHz
		MSI range 1	131	-	
		MSI range 2	262	-	
		MSI range 3	524	-	
		MSI range 4	1.05	-	MHz
		MSI range 5	2.1	-	
		MSI range 6	4.2	-	

Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table “ *I/O AC characteristics*”.

6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} , except when it is internally driven low (see *Table 62*).

Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

Table 62. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST input not filtered pulse	-	350	-	-	ns

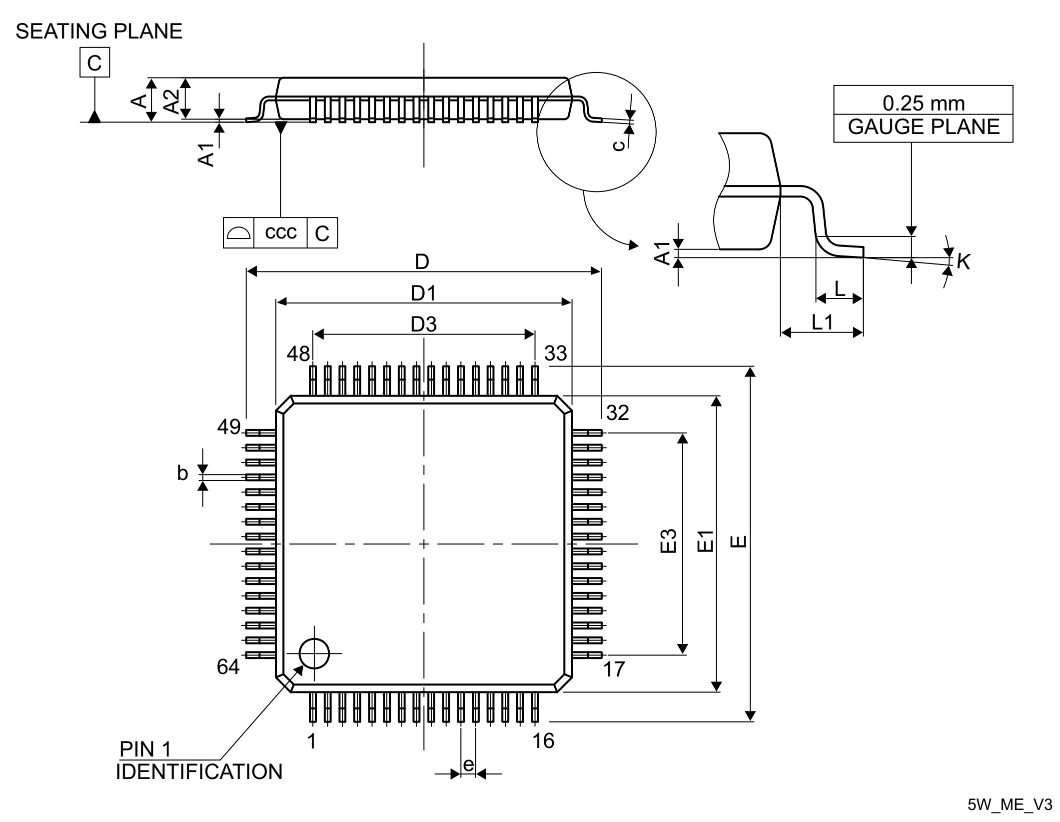
1. Guaranteed by design.
2. 200 mV minimum value
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 85. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.305[3]	-	-	0.012	-
G	-	0.440[3]	-	-	0.017	-
aaa	-	-	0.100	-	-	0.004
bbb	-	-	0.100	-	-	0.004
ccc	-	-	0.100	-	-	0.004
ddd	-	-	0.050	-	-	0.002
eee	-	-	0.050	-	-	0.002

1. Values in inches are converted from mm and rounded to the 3rd decimal place.
2. Nominal dimension rounded to the 3rd decimal place results from process capability.
3. Calculated dimensions are rounded to the 3rd decimal place.

Figure 49. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale recommended footprint

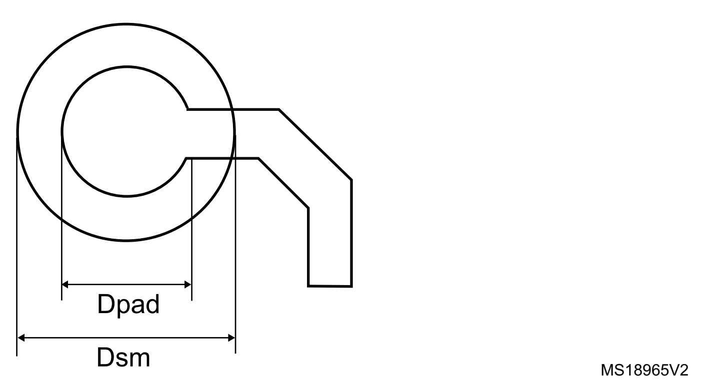


Table 86. Standard WLCSP36 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Table 93. Document revision history (continued)

Date	Revision	Changes
25-Jun-2014	3	Cover page: changed LQFP32 size, updated core speed, added minimum supply voltage for ADC, DAC and comparators. ADC now guaranteed down to 1.65 V. Updated list of applications in *Section 1: Introduction*. Changed number of I2S interfaces to one in *Section 1: Description*. Updated *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Updated RTC/TIM21 in *Table 6: STM32L0xx peripherals interconnect matrix*. Updated *Table 3: Functionalities depending on the operating power supply range*. Split LQFP32/UFQFPN32 pinout schematics into two distinct figures: *Figure 7* and *Figure 8*. Added note related to WLCSP36 package in *Table 16: STM32L052x6/8 pin definitions*. Updated *Section 3.4.1: Power supply schemes*. Updated V_{DDA} in *Table 25: General operating conditions*. Splitted Table *Current consumption in Run mode, code with data processing running from Flash* into *Table 29* and *Table 30* and content updated. Split Table *Current consumption in Run mode, code with data processing running from RAM* into *Table 31* and *Table 32* and content updated. Updated *Table 33: Current consumption in Sleep mode*, *Table 34: Current consumption in Low-power run mode*, *Table 35: Current consumption in Low-power sleep mode*, *Table 36: Typical and maximum current consumptions in Stop mode*, *Table 37: Typical and maximum current consumptions in Standby mode*, and added *Table 38: Average current consumption during Wakeup*. Updated *Table 39: Peripheral current consumption in Run or Sleep mode* and added *Table 40: Peripheral current consumption in Stop and Standby mode*. Updated *Table 47: HSI48 oscillator characteristics*. Removed note 1 below *Figure 21: HSE oscillator circuit diagram*. Updated t_{LOCK} in *Table 50: PLL characteristics*. Updated *Table 52: Flash memory and data EEPROM characteristics* and *Table 53: Flash memory and data EEPROM endurance and retention*. Updated *Table 61: I/O AC characteristics*. Updated *Table 63: ADC characteristics*. Updated *Figure 59: Thermal resistance* and added note 1.