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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

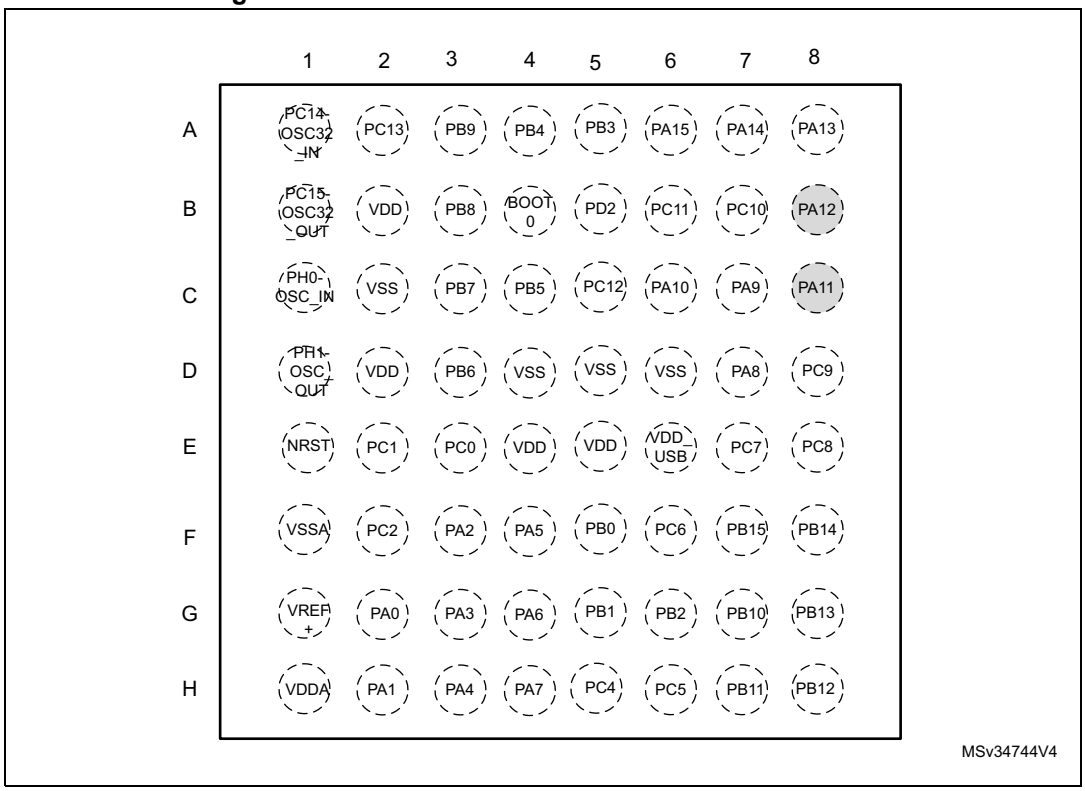
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052r6t6

Table 5. Functionalities depending on the working mode (from Run/active down to standby) (1)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	(2)		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
USB	O	O	--	--	--	O	--	
USART	O	O	O	O	O(3)	O	--	
LPUART	O	O	O	O	O(3)	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O(4)	O	--	
ADC	O	O	--	--	--		--	
DAC	O	O	O	O	O		--	

Figure 4. STM32L052x6/8 TFBGA64 ballout - 5x 5 mm



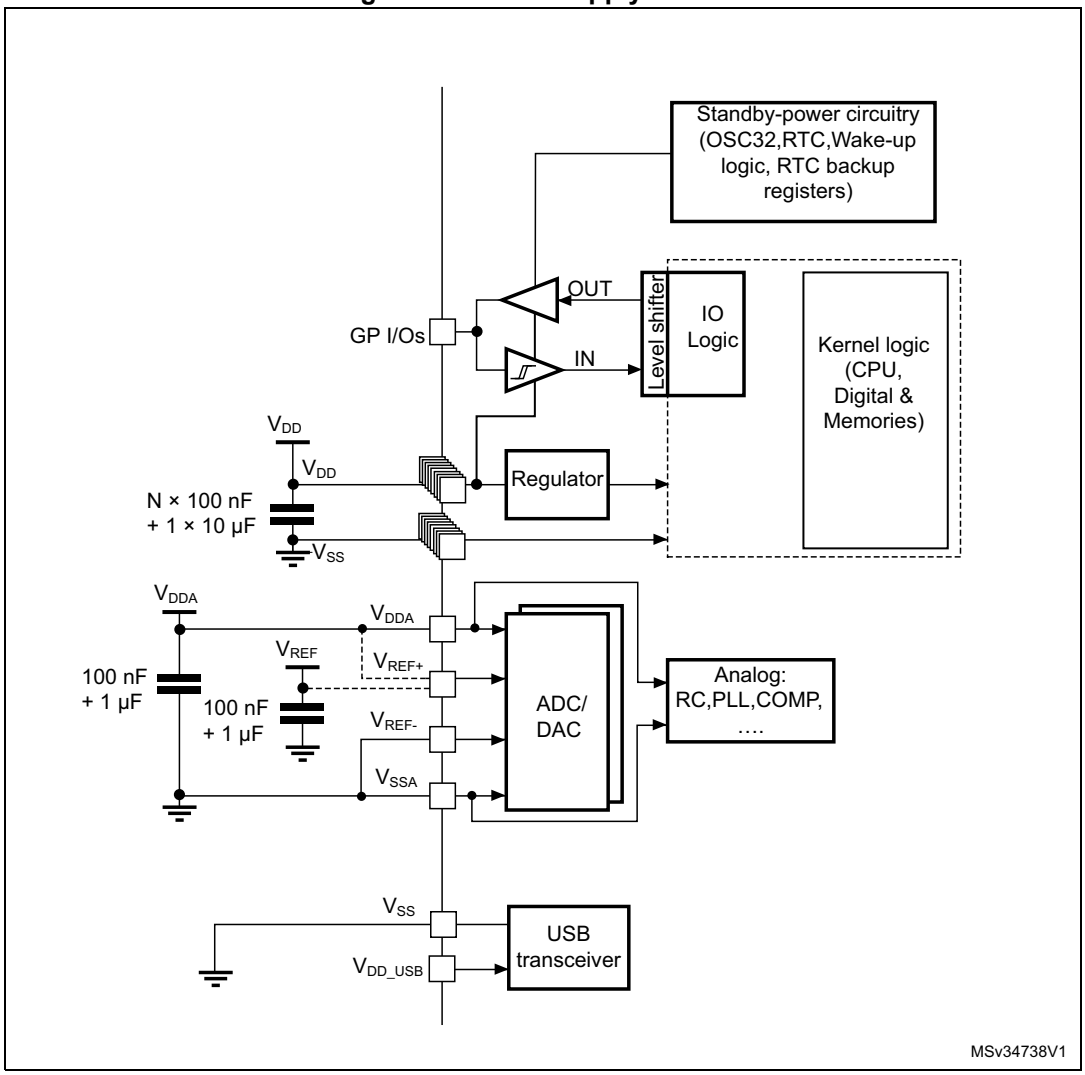
1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 19. Alternate function port C

Port		AF0	AF1	AF2	AF3
		LPUART1/LPTIM/ TIM21/12/ EVENTOUT/	-	SPI2/I2S2/USB/ LPUART1/ EVENTOUT	TSC
Port C	PC0	LPTIM1_IN1	-	EVENTOUT	TSC_G7_IO1
	PC1	LPTIM1_OUT	-	EVENTOUT	TSC_G7_IO2
	PC2	LPTIM1_IN2	-	SPI2_MISO/I2S2_MCK	TSC_G7_IO3
	PC3	LPTIM1_ETR	-	SPI2_MOSI/I2S2_SD	TSC_G7_IO4
	PC4	EVENTOUT	-	LPUART1_TX	-
	PC5	-	-	LPUART1_RX	TSC_G3_IO1
	PC6	TIM22_CH1	-	-	TSC_G8_IO1
	PC7	TIM22_CH2	-	-	TSC_G8_IO2
	PC8	TIM22_ETR	-	-	TSC_G8_IO3
	PC9	TIM21_ETR	-	USB_NOE	TSC_G8_IO4
	PC10	LPUART1_TX	-	-	-
	PC11	LPUART1_RX	-	-	-
	PC12	-	-	-	-
	PC13	-	-	-	-
	PC14	-	-	-	-
	PC15	-	-	-	-

6.1.6 Power supply scheme

Figure 12. Power supply scheme



6.1.7 Current consumption measurement

Figure 13. Current consumption measurement scheme

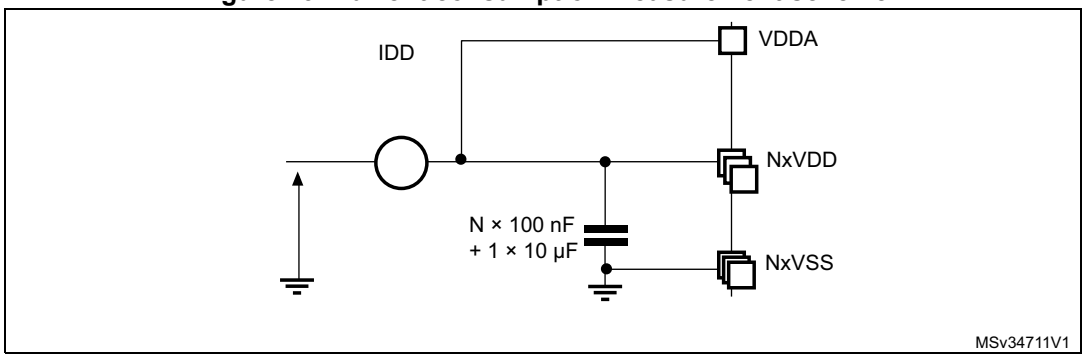


Table 31. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	135	170	µA
				2 MHz	240	270	
				4 MHz	450	480	
			Range 2, V_{CORE}=1.5 ,V, VOS[1:0]=10	4 MHz	0.52	0.6	mA
				8 MHz	1	1.2	
				16 MHz	2	2.3	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4	
				16 MHz	2.45	2.8	
				32 MHz	5.1	5.4	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	34.5	75	µA
				524 kHz	83	120	
				4.2 MHz	485	540	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	2.1	2.3	mA
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	5.1	5.6	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 32. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	450	µA
				CoreMark		575	
				Fibonacci		370	
				while(1)		340	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	5.1	mA
				CoreMark		6.25	
				Fibonacci		4.4	
				while(1)		4.7	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 41. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	5.0	8	µs
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	7.3	13	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	13	23	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	28	38	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	51	65	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	100	120	
		f_{HCLK} = MSI = 65 kHz	190	260	
		$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI}$ = 16 MHz	4.9	7	
		$f_{HCLK} = f_{HSI}/4$ = 4 MHz	7.9	10	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode, FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	65	130	µs
	Wakeup from Standby mode, FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.2	3	ms

Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 25*.

Table 43. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 20. Low-speed external clock source AC timing diagram

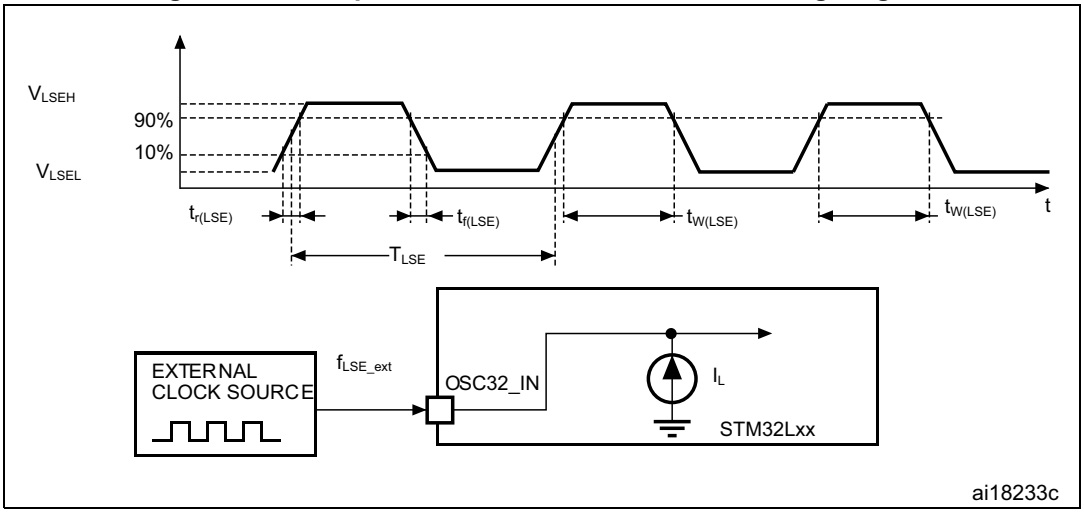


Table 49. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤T_A ≤110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. f_{osc}/f_{CPU}			Unit
				8 MHz/ 4 MHz	8 MHz/ 16 MHz	8 MHz/ 32 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, compliant with IEC 61967-2	0.1 to 30 MHz	-21	-15	-12	dBµV
			30 to 130 MHz	-14	-12	-1	
			130 MHz to 1GHz	-10	-11	-7	
			EMI Level	1	1	1	-

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 26* and *Table 61*, respectively.

Unless otherwise specified, the parameters given in *Table 61* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 25*.

Table 61. I/O AC characteristics(1)

OSPEEDRx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	100	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	320	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	0.6	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	65	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	13	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	28	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	35	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	10	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	6	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	17	
Fm+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.5 V to 3.6 V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	10	ns
	$t_{r(IO)out}$	Output rise time		-	30	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 1.65 V to 3.6 V	-	350	KHz
	$t_{f(IO)out}$	Output fall time		-	15	ns
	$t_{r(IO)out}$	Output rise time		-	60	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 26*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the line reference manual for a detailed description of Fm+ I/O configuration.

Table 63. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ADC}(3)(4)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)(5)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$(6)	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 16 MHz	0.266			µs
		$f_{ADC} = f_{PCLK}/2$	8.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 8 MHz	0.516			µs
		$f_{ADC} = f_{PCLK}/4$	16.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16}$ = 16 MHz	0.252	-	0.260	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI16}$	-	1	-	$1/f_{HSI16}$
t_S(3)	Sampling time	f_{ADC} = 16 MHz	0.093	-	10.03	µs
		-	1.5	-	160.5	$1/f_{ADC}$
t_{UP_LDO}(3)(5)	Internal LDO power-up time	-	-	-	10	µs
t_{STAB}(3)(5)	ADC stabilization time	-	14			$1/f_{ADC}$
t_{ConV}(3)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz, 12-bit resolution	0.875	-	10.81	µs
		12-bit resolution	14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to *Table 64: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 39: Peripheral current consumption in Run or Sleep mode*).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 64: RAIN max for fADC = 16 MHz*.
5. This parameter only includes the ADC timing. It does not take into account register access latency.
6. This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

Table 66. DAC characteristics (continued)

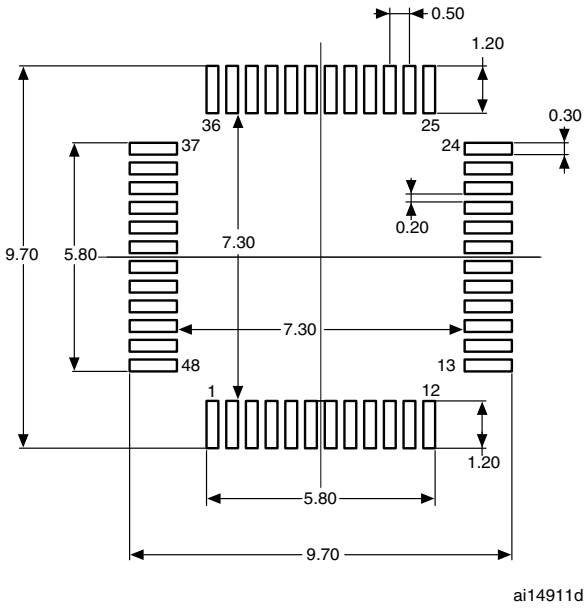
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL(2)	Differential non linearity(4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	1.5	3	
INL(2)	Integral non linearity(5)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	2	4	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	2	4	
Offset(2)	Offset error at code 0x800 (6)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	±10	±25	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	±5	±8	
Offset1(2)	Offset error at code 0x001(7)	No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	±1.5	±5	
dOffset/dT(2)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(2)	Gain error(8)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(2)	Gain error temperature coefficient	V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(2)	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	

Table 84. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

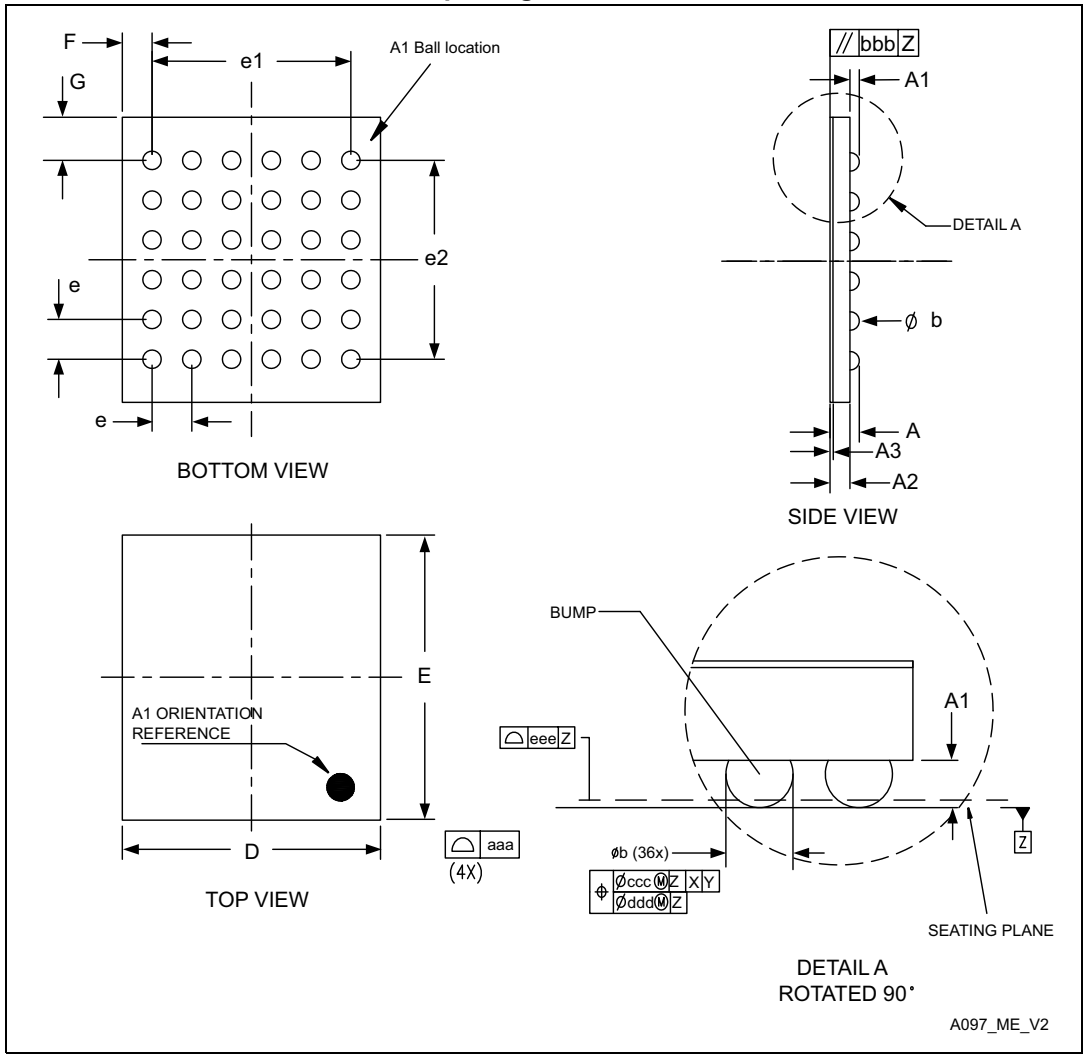
Figure 46. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat recommended footprint



1. Dimensions are expressed in millimeters.

7.5 Thin WLCSP36 package information

Figure 51. Thin WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline



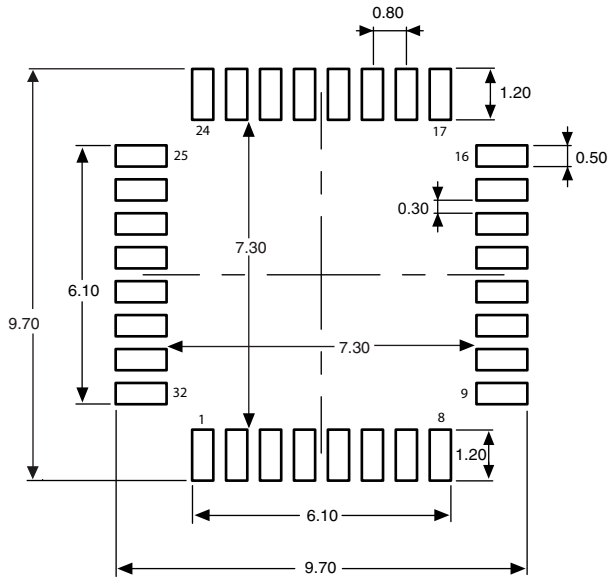
1. Drawing is not to scale.
2. b dimensions is measured at the maximum bump diameter parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
4. Bump position designation per JESD 95-1, SPP-010.

Table 89. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 54. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat recommended footprint



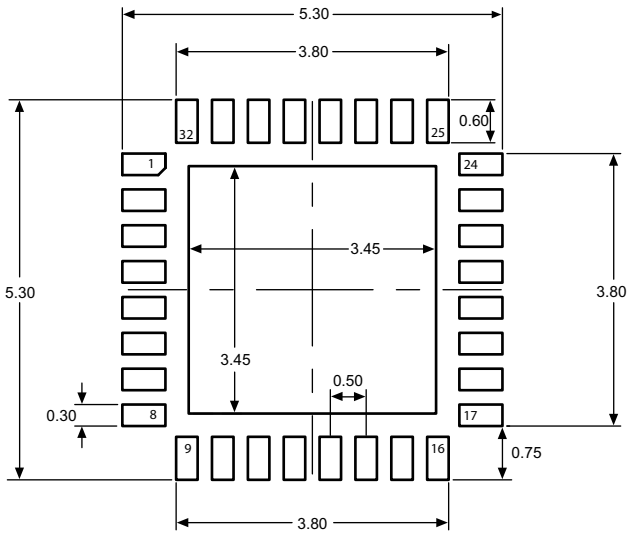
1. Dimensions are expressed in millimeters.

Table 90. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 57. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat recommended footprint



1. Dimensions are expressed in millimeters.

Table 93. Document revision history (continued)

Date	Revision	Changes
25-Jun-2014	3	Cover page: changed LQFP32 size, updated core speed, added minimum supply voltage for ADC, DAC and comparators. ADC now guaranteed down to 1.65 V. Updated list of applications in *Section 1: Introduction*. Changed number of I2S interfaces to one in *Section 1: Description*. Updated *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Updated RTC/TIM21 in *Table 6: STM32L0xx peripherals interconnect matrix*. Updated *Table 3: Functionalities depending on the operating power supply range*. Split LQFP32/UFQFPN32 pinout schematics into two distinct figures: *Figure 7* and *Figure 8*. Added note related to WLCSP36 package in *Table 16: STM32L052x6/8 pin definitions*. Updated *Section 3.4.1: Power supply schemes*. Updated V_{DDA} in *Table 25: General operating conditions*. Splitted Table *Current consumption in Run mode, code with data processing running from Flash* into *Table 29* and *Table 30* and content updated. Split Table *Current consumption in Run mode, code with data processing running from RAM* into *Table 31* and *Table 32* and content updated. Updated *Table 33: Current consumption in Sleep mode*, *Table 34: Current consumption in Low-power run mode*, *Table 35: Current consumption in Low-power sleep mode*, *Table 36: Typical and maximum current consumptions in Stop mode*, *Table 37: Typical and maximum current consumptions in Standby mode*, and added *Table 38: Average current consumption during Wakeup*. Updated *Table 39: Peripheral current consumption in Run or Sleep mode* and added *Table 40: Peripheral current consumption in Stop and Standby mode*. Updated *Table 47: HSI48 oscillator characteristics*. Removed note 1 below *Figure 21: HSE oscillator circuit diagram*. Updated t_{LOCK} in *Table 50: PLL characteristics*. Updated *Table 52: Flash memory and data EEPROM characteristics* and *Table 53: Flash memory and data EEPROM endurance and retention*. Updated *Table 61: I/O AC characteristics*. Updated *Table 63: ADC characteristics*. Updated *Figure 59: Thermal resistance* and added note 1.

Table 93. Document revision history (continued)

Date	Revision	Changes
05-Sep-2014	4	Extended operating temperature range to 125 °C. Updated minimum ADC operating voltage to 1.65 V. Changed number of I2S interface from 1 to 0 in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Replaced USART3 by LPUART1 in *Table 16: STM32L052x6/8 pin definitions* and LPUART by LPUART1 in *Table 17: Alternate function port A*, *Table 18: Alternate function port B*, *Table 19: Alternate function port C*, *Table 20: Alternate function port D* and *Table 21: Alternate function port H*. Updated PA6 in *Table 17: Alternate function port A*. Updated temperature range in *Section 1: Description*, *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Updated P_D, $T_{A\ and}$ T_J to add range 3 in *Table 25: General operating conditions*. Added range 3 in *Table 53: Flash memory and data EEPROM endurance and retention*, *Table 92: STM32L052x6/8 ordering information scheme*. Update note 1 in *Table 29: Current consumption in Run mode, code with data processing running from Flash*, *Table 31: Current consumption in Run mode, code with data processing running from RAM*, *Table 33: Current consumption in Sleep mode*, *Table 34: Current consumption in Low-power run mode*, *Table 34: Current consumption in Low-power run mode*, *Table 36: Typical and maximum current consumptions in Stop mode*, *Table 37: Typical and maximum current consumptions in Standby mode* and *Table 41: Low-power mode wakeup timings*. Updated *Figure 59: Thermal resistance* and removed note 1. Updated *Figure 16: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 17: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive*, *Figure 18: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 37: Typical and maximum current consumptions in Standby mode*. Updated SYSCFG in *Table 39: Peripheral current consumption in Run or Sleep mode*. Updated *Table 40: Peripheral current consumption in Stop and Standby mode* and *Table 43: Low-speed external user clock characteristics*. Updated ACC_{HSI16} temperature conditions in *Table 46: 16 MHz HSI16 oscillator characteristics*. Changed ambient temperature range in note 1 below *Table 47: HSI48 oscillator characteristics*. Updated $V_{F(NRST)}$ and $V_{NF(NRST)}$ in *Table 62: NRST pin characteristics*. Updated *Table 63: ADC characteristics* and *Table 65: ADC accuracy*. Added range 3 in *Table 92: STM32L052x6/8 ordering information scheme*.

Table 93. Document revision history (continued)

Date	Revision	Changes
11-Mar-2016	6	Updated number of SPIs on cover page and in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. Changed minimum comparator supply voltage to 1.65 V on cover page. Added number of fast and standard channels in *Section 3.11: Analog-to-digital converter (ADC)*. Updated *Section 3.18.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.18.4: Serial peripheral interface (SPI)/Inter-integrated sound (I2S)* to mention the fact that USARTs with synchronous mode feature can be used as SPI master interfaces. Added baudrate allowing to wake up the MCU from Stop mode in *Section 3.18.2: Universal synchronous/asynchronous receiver transmitter (USART)* and *Section 3.18.3: Low-power universal asynchronous receiver transmitter (LPUART)*. In *Section 6: Electrical characteristics*, updated notes related to values guaranteed by characterization. Updated *Table 58: I/O current injection susceptibility*. Updated *Figure 6: STM32L052x6/8 WLCSP36 ballout*, *Figure 8: STM32L052x6/8 UFQFPN32 pinout* removing grey PA11, PA12 pins and removing note 2. Updated *Table 55: EMI characteristics*. Changed temperature condition in *Table 8: Internal voltage reference measured values* and *Table 27: Embedded internal reference voltage calibration values*. *Section 6.3.15: 12-bit ADC characteristics*: – *Table 63: ADC characteristics*: Distinction made between V_{DDA} for fast and standard channels; added note 1 Added note 4 related to R_{ADC}. Updated f_{TRIG}. Updated t_S and t_{CONV}. – Updated equation 1 description. – Updated *Table 64: RAIN max for fADC = 16 MHz* for f_{ADC} = 16 MHz and distinction made between fast and standard channels. Updated R_O and added Note 2 in *Table 66: DAC characteristics*. Added *Table 73: USART/LPUART characteristics*. Updated *Figure 47: LQFP48 marking example (package top view)*.

Table 93. Document revision history (continued)

Date	Revision	Changes
07-Mar-2017	7	Added thin WLCSP36 package. Updated number of I2S interfaces and removed I2S for STM32L052T8 in *Table 2: Ultra-low-power STM32L052x6/x8 device features and peripheral counts*. In *Section 4: Pin descriptions*, renamed USB_OE into USB_NOE. Added mission profile compliance with JEDEC JESD47 in *Section 6.2: Absolute maximum ratings*. Added note 2. related to the position of the external capacitor below *Figure 27: Recommended NRST pin protection*. Updated R_L in *Table 63: ADC characteristics*. Updated *Figure 32: 12-bit buffered/non-buffered DAC* and added note below figure. Updated t_{AF} maximum value for range 1 in *Table 72: I2C analog filter characteristics*. Updated $t_{WUUSART}$ description in *Table 73: USART/LPUART characteristics*. NSS timing waveforms updated in *Figure 33: SPI timing diagram - slave mode and CPHA = 0* and *Figure 34: SPI timing diagram - slave mode and CPHA = 1(1)*. Previous WLCSP36 package renamed “Standard” WLCSP36; added Note *2.* below *Figure 48: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline* and updated *Table 85: Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data*. Added reference to optional marking or inset/upset marks in all package device marking sections.