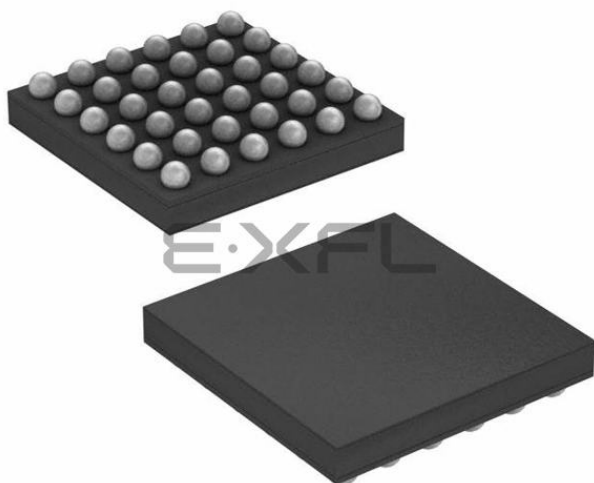




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	29
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l052t8y6tr

3.17.5	Independent watchdog (IWDG)	34
3.17.6	Window watchdog (WWDG)	34
3.18	Communication interfaces	34
3.18.1	I2C bus	34
3.18.2	Universal synchronous/asynchronous receiver transmitter (USART)	35
3.18.3	Low-power universal asynchronous receiver transmitter (LPUART)	36
3.18.4	Serial peripheral interface (SPI)/Inter-integrated sound (I2S)	36
3.18.5	Universal serial bus (USB)	37
3.19	Clock recovery system (CRS)	37
3.20	Cyclic redundancy check (CRC) calculation unit	37
3.21	Serial wire debug port (SW-DP)	37
4	Pin descriptions	38
5	Memory mapping	52
6	Electrical characteristics	53
6.1	Parameter conditions	53
6.1.1	Minimum and maximum values	53
6.1.2	Typical values	53
6.1.3	Typical curves	53
6.1.4	Loading capacitor	53
6.1.5	Pin input voltage	53
6.1.6	Power supply scheme	54
6.1.7	Current consumption measurement	54
6.2	Absolute maximum ratings	55
6.3	Operating conditions	57
6.3.1	General operating conditions	57
6.3.2	Embedded reset and power control block characteristics	59
6.3.3	Embedded internal reference voltage	60
6.3.4	Supply current characteristics	61
6.3.5	Wakeup time from low-power mode	72
6.3.6	External clock source characteristics	74
6.3.7	Internal clock source characteristics	78
6.3.8	PLL characteristics	81
6.3.9	Memory characteristics	82
6.3.10	EMC characteristics	83

2.1 Device overview

Table 2. Ultra-low-power STM32L052x6/x8 device features and peripheral counts

Peripheral		STM32L052T6	STM32L052K6	STM32L052C6	STM32L052R6	STM32L052T8	STM32L052K8	STM32L052C8	STM32L052R8
Flash (Kbytes)		32				64			
Data EEPROM (Kbytes)		2				2			
RAM (Kbytes)		8				8			
Timers	General-purpose	3				3			
	Basic	1				1			
	LPTIMER	1				1			
RTC/SYSTICK/IWDG/WWDG		1/1/1/1				1/1/1/1			
Communication interfaces	SPI/I2S	3(2) ⁽¹⁾ /0	3(2) ⁽¹⁾ /0	4(2) ⁽¹⁾ /1	3(2) ⁽¹⁾ /0	3(2) ⁽¹⁾ /0		4(2) ⁽¹⁾ /1	
	I ² C	2	1	2		2	1	2	
	USART	2				2			
	LPUART	1	0	1		1	0	1	
	USB/(VDD_USB)	1/(0)		1/(1)		1/(0)		1/(1)	
GPIOs		29	27 ⁽²⁾	37	51 ⁽³⁾	29	27 ⁽²⁾	37	51 ⁽³⁾
Clocks: HSE/LSE/HSI/MSI/LSI		0/1/1/1/1	0/1/1/1/1	1/1/1/1/1	1/1/1/1/1	0/1/1/1/1	0/1/1/1/1	1/1/1/1/1	1/1/1/1/1
12-bit synchronized ADC Number of channels		1 10	1 10	1 10	1 16 ⁽³⁾	1 10	1 10	1 10	1 16 ⁽³⁾
12-bit DAC Number of channels		1 1				1 1			
Comparators		2							
Capacitive sensing channels		14		17	24 ⁽³⁾	14		17	24 ⁽³⁾
Max. CPU frequency		32 MHz							
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option							

**Table 5. Functionalities depending on the working mode
(from Run/active down to standby) ⁽¹⁾**

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--		--	
Flash memory	O	O	O	O	--		--	
RAM	Y	Y	Y	Y	Y		--	
Backup registers	Y	Y	Y	Y	Y		Y	
EEPROM	O	O	O	O	--		--	
Brown-out reset (BOR)	O	O	O	O	O	O	O	O
DMA	O	O	O	O	--		--	
Programmable Voltage Detector (PVD)	O	O	O	O	O	O	-	
Power-on/down reset (POR/PDR)	Y	Y	Y	Y	Y	Y	Y	Y
High Speed Internal (HSI)	O	O	--	--	⁽²⁾		--	
High Speed External (HSE)	O	O	O	O	--		--	
Low Speed Internal (LSI)	O	O	O	O	O		O	
Low Speed External (LSE)	O	O	O	O	O		O	
Multi-Speed Internal (MSI)	O	O	Y	Y	--		--	
Inter-Connect Controller	Y	Y	Y	Y	Y		--	
RTC	O	O	O	O	O	O	O	
RTC Tamper	O	O	O	O	O	O	O	O
Auto WakeUp (AWU)	O	O	O	O	O	O	O	O
USB	O	O	--	--	--	O	--	
USART	O	O	O	O	O ⁽³⁾	O	--	
LPUART	O	O	O	O	O ⁽³⁾	O	--	
SPI	O	O	O	O	--		--	
I2C	O	O	O	O	O ⁽⁴⁾	O	--	
ADC	O	O	--	--	--		--	
DAC	O	O	O	O	O		--	

Table 14. SPI/I2S implementation

SPI features ⁽¹⁾	SPI1	SPI2
Hardware CRC calculation	X	X
I2S mode	-	X
TI mode	X	X

1. X = supported.

3.18.5 Universal serial bus (USB)

The STM32L052x6/8 embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.19 Clock recovery system (CRS)

The STM32L052x6/8 embed a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.20 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at linktime and stored at a given memory location.

3.21 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 15. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 16. STM32L052x6/8 pin definitions

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36 ⁽¹⁾	LQFP48	LQFP64	TFBGA64						
-	-	-	1	1	B2	VDD	S	-	-	-	-
-	-	-	2	2	A2	PC13	I/O	FT	-	-	RTC_TAMP1/ RTC_TS/RTC _OUT/WKUP2
2	2	A6	3	3	A1	PC14- OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
3	3	B6	4	4	B1	PC15- OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36 ⁽¹⁾	LQFP48	LQFP64	TFBGA64						
9	9	F5	13	17	G3	PA3	I/O	FT	-	TIM21_CH2, TIM2_CH4, TSC_G1_IO4, USART2_RX	COMP2_INP, ADC_IN3
-	-	-	-	18	C2	VSS	S	-	-	-	-
-	-	-	-	19	D2	VDD	S	-	-	-	-
10	10	E4	14	20	H3	PA4	I/O	TC	(2)	SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR	COMP1_INM4 , COMP2_INM4 , ADC_IN4, DAC_OUT
11	11	F4	15	21	F4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1	COMP1_INM5 , COMP2_INM5 , ADC_IN5
12	12	E3	16	22	G4	PA6	I/O	FT	-	SPI1_MISO, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
13	13	F3	17	23	H4	PA7	I/O	FT	-	SPI1_MOSI, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	-	-	-	24	H5	PC4	I/O	FT	-	EVENTOUT, LPUART1_TX	ADC_IN14
-	-	-	-	25	H6	PC5	I/O	FT	-	LPUART1_RX, TSC_G3_IO1	ADC_IN15
14	14	D3	18	26	F5	PB0	I/O	FT	-	EVENTOUT, TSC_G3_IO2	ADC_IN8, VREF_OUT
15	15	C3	19	27	G5	PB1	I/O	FT	-	TSC_G3_IO3, LPUART1_RTS_DE	ADC_IN9, VREF_OUT
-	16	F2	20	28	G6	PB2	I/O	FT	-	LPTIM1_OUT, TSC_G3_IO4	-

Table 16. STM32L052x6/8 pin definitions (continued)

Pin Number						Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP32	UFQFN32	WLCSP36 ⁽¹⁾	LQFP48	LQFP64	TFBGA64						
-	-	-	-	54	B5	PD2	I/O	FT	-	LPUART1_RTS_DE	-
26	26	B3	39	55	A5	PB3	I/O	FT	-	SPI1_SCK, TIM2_CH2, TSC_G5I_O1, EVENTOUT	COMP2_INN
27	27	A3	40	56	A4	PB4	I/O	FT	-	SPI1_MISO, EVENTOUT, TSC_G5_IO2, TIM22_CH1	COMP2_INP
28	28	C4	41	57	C4	PB5	I/O	FT	-	SPI1_MOSI, LPTIM1_IN1, I2C1_SMBA, TIM22_CH2	COMP2_INP
29	29	B4	42	58	D3	PB6	I/O	FTf	-	USART1_TX, I2C1_SCL, LPTIM1_ETR, TSC_G5_IO3	COMP2_INP
30	30	A4	43	59	C3	PB7	I/O	FTf	-	USART1_RX, I2C1_SDA, LPTIM1_IN2, TSC_G5_IO4	COMP2_INP, PVD_IN
31	31	C5	44	60	B4	BOOT0	B	-	-	-	-
-	32	B5	45	61	B3	PB8	I/O	FTf	-	TSC_SYNC, I2C1_SCL	-
-	-	-	46	62	A3	PB9	I/O	FTf	-	EVENTOUT, I2C1_SDA, SPI2_NSS/I2S2_WS	-
32	-	D6	47	63	D4	VSS	S	-	-	-	-
1	1	A5	48	64	E4	VDD	S	-	-	-	-

1. PB9/12/13/14/15, PH0/1 and PC13 GPIOs should be configured as output and driven Low, even if they are not available on this package.
2. PA4 offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.
3. These pins are powered by VDD_USB. For all characteristics that refer to V_{DD}, V_{DD_USB} must be used instead.

Table 25. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T _A	Temperature range	Maximum power dissipation (range 6)	−40	85	°C
		Maximum power dissipation (range 7)	−40	105	
		Maximum power dissipation (range 3)	−40	125	
T _J	Junction temperature range (range 6)	−40 °C ≤ T _A ≤ 85 °	−40	105	
	Junction temperature range (range 7)	−40 °C ≤ T _A ≤ 105 °C	−40	125	
	Junction temperature range (range 3)	−40 °C ≤ T _A ≤ 125 °C	−40	130	

1. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
2. V_{DD_USB} must respect the following conditions:
 - When V_{DD} is powered-on (V_{DD} < V_{DD_min}), V_{DD_USB} should be always lower than V_{DD}.
 - When V_{DD} is powered-down (V_{DD} < V_{DD_min}), V_{DD_USB} should be always lower than V_{DD}.
 - In operating mode, V_{DD_USB} could be lower or higher V_{DD}.
 - If the USB is not used, V_{DD_USB} must range from V_{DD_min} to V_{DD_max} to be able to use PA11 and PA12 as standard I/Os.
3. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see [Table 24: Thermal characteristics on page 56](#)).

Table 26. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Falling edge	2.97	3.05	3.09	V
		Rising edge	3.08	3.15	3.20	
V_{hyst}	Hysteresis voltage	BOR0 threshold	-	40	-	mV
		All BOR and PVD thresholds excepting BOR0	-	100	-	

1. Guaranteed by characterization results.

2. Valid for device version without BOR at power up. Please see option "D" in Ordering information scheme for more details.

6.3.3 Embedded internal reference voltage

The parameters given in [Table 28](#) are based on characterization results, unless otherwise specified.

Table 27. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C $V_{DDA} = 3\text{ V}$	0x1FF8 0078 - 0x1FF8 0079

Table 28. Embedded internal reference voltage⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}^{(2)}$	Internal reference voltage	$-40\text{ °C} < T_J < +125\text{ °C}$	1.202	1.224	1.242	V
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REFINT} value ⁽³⁾	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
$T_{Coeff}^{(4)}$	Temperature coefficient	$-40\text{ °C} < T_J < +125\text{ °C}$	-	25	100	ppm/°C
$A_{Coeff}^{(4)}$	Long-term stability	1000 hours, $T = 25\text{ °C}$	-	-	1000	ppm
$V_{DDCcoeff}^{(4)}$	Voltage coefficient	$3.0\text{ V} < V_{DDA} < 3.6\text{ V}$	-	-	2000	ppm/V
$T_{S_vrefint}^{(4)(5)}$	ADC sampling time when reading the internal reference voltage	-	5	10	-	µs
$T_{ADC_BUF}^{(4)}$	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
$I_{BUF_ADC}^{(4)}$	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
$I_{VREF_OUT}^{(4)}$	VREF_OUT output current ⁽⁶⁾	-	-	-	1	µA
$C_{VREF_OUT}^{(4)}$	VREF_OUT output load	-	-	-	50	pF

Table 41. Low-power mode wakeup timings (continued)

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	5.0	8	μs
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode	$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 1	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 2	5.0	8	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$ Voltage range 3	5.0	8	
		$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	7.3	13	
		$f_{HCLK} = f_{MSI} = 1.05 \text{ MHz}$	13	23	
		$f_{HCLK} = f_{MSI} = 524 \text{ kHz}$	28	38	
		$f_{HCLK} = f_{MSI} = 262 \text{ kHz}$	51	65	
		$f_{HCLK} = f_{MSI} = 131 \text{ kHz}$	100	120	
		$f_{HCLK} = f_{MSI} = 65 \text{ kHz}$	190	260	
		$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	8.0	11	
	Wakeup from Stop mode, regulator in low-power mode, code running from RAM	$f_{HCLK} = f_{HSI} = 16 \text{ MHz}$	4.9	7	
		$f_{HCLK} = f_{HSI}/4 = 4 \text{ MHz}$	7.9	10	
		$f_{HCLK} = f_{MSI} = 4.2 \text{ MHz}$	4.7	8	
$t_{WUSTDBY}$	Wakeup from Standby mode, FWU bit = 1	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	65	130	μs
	Wakeup from Standby mode, FWU bit = 0	$f_{HCLK} = f_{MSI} = 2.1 \text{ MHz}$	2.2	3	ms

Low-speed external user clock generated from an external source

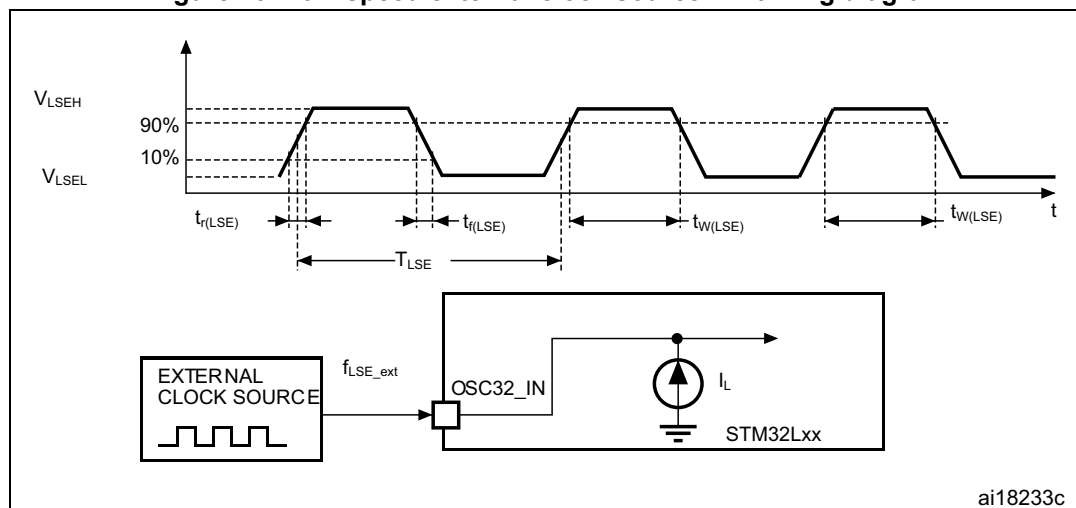
The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 25](#).

Table 43. Low-speed external user clock characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design, not tested in production

Figure 20. Low-speed external clock source AC timing diagram



ai18233c

Table 53. Flash memory and data EEPROM endurance and retention (continued)

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
t _{RET} ⁽²⁾	Data retention (program memory) after 10 kcycles at T _A = 85 °C	T _{RET} = +85 °C	30	years
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 85 °C		30	
	Data retention (program memory) after 10 kcycles at T _A = 105 °C	T _{RET} = +105 °C	10	
	Data retention (EEPROM data memory) after 100 kcycles at T _A = 105 °C			
	Data retention (program memory) after 200 cycles at T _A = 125 °C	T _{RET} = +125 °C		
	Data retention (EEPROM data memory) after 2 kcycles at T _A = 125 °C			

1. Guaranteed by characterization results.

2. Characterization is done according to JEDEC JESD22-A117.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 54](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 54. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{\text{DD}} = 3.3\text{ V}$, LQFP64, $T_A = +25\text{ °C}$, $f_{\text{HCLK}} = 32\text{ MHz}$ conforms to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{\text{DD}} = 3.3\text{ V}$, LQFP64, $T_A = +25\text{ °C}$, $f_{\text{HCLK}} = 32\text{ MHz}$ conforms to IEC 61000-4-4	4A

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 64. R_{AIN} max for $f_{ADC} = 16 \text{ MHz}^{(1)}$

T_S (cycles)	t_S (μs)	R_{AIN} max for fast channels ($k\Omega$)	R_{AIN} max for standard channels ($k\Omega$)						
			$V_{DD} > 2.7 \text{ V}$	$V_{DD} > 2.4 \text{ V}$	$V_{DD} > 2.0 \text{ V}$	$V_{DD} > 1.8 \text{ V}$	$V_{DD} > 1.75 \text{ V}$	$V_{DD} > 1.65 \text{ V}$ and $T_A > -10 \text{ }^\circ\text{C}$	$V_{DD} > 1.65 \text{ V}$ and $T_A > 25 \text{ }^\circ\text{C}$
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 65. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	$1.65 \text{ V} < V_{DDA} = V_{REF+} < 3.6 \text{ V}$, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11	-	bits
	Effective number of bits (16-bit mode oversampling with ratio =256) ⁽⁴⁾		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256) ⁽⁴⁾		70	76	-	
THD	Total harmonic distortion		-	-85	-73	

6.3.17 Temperature sensor characteristics

Table 67. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, $V_{DDA} = 3\text{ V}$	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, $V_{DDA} = 3\text{ V}$	0x1FF8 007E - 0x1FF8 007F

Table 68. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope ⁽¹⁾	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C $\pm 5^\circ\text{C}^{(2)}$	640	670	700	mV
$I_{DDA(TEMP)}^{(3)}$	Current consumption	-	3.4	6	μA
$t_{START}^{(3)}$	Startup time	-	-	10	μs
$T_{S_temp}^{(4)(3)}$	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at $V_{DD} = 3\text{ V} \pm 10\text{ mV}$. V_{130} ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 Comparators

Table 69. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	μs
t_d	Propagation delay ⁽²⁾	-	-	3	10	
V_{offset}	Comparator offset	-	-	± 3	± 10	mV
$d_{V_{offset}}/dt$	Comparator offset variation in worst voltage stress conditions	$V_{DDA} = 3.6\text{ V}$, $V_{IN+} = 0\text{ V}$, $V_{IN-} = V_{REFINT}$, $T_A = 25^\circ\text{C}$	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption ⁽³⁾	-	-	160	260	nA

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

The analog spike filter is compliant with I²C timings requirements only for the following voltage ranges:

- Fast mode Plus: $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ and voltage scaling Range 1
- Fast mode:
 - $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ and voltage scaling Range 1 or Range 2.
 - $V_{DD} < 2\text{ V}$, voltage scaling Range 1 or Range 2, $C_{load} < 200\text{ pF}$.

In other ranges, the analog filter should be disabled. The digital filter can be used instead.

Note: In Standard mode, no spike filter is required.

Table 72. I2C analog filter characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	Range 1	50 ⁽²⁾	260 ⁽³⁾	ns
		Range 2		-	
		Range 3		-	

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

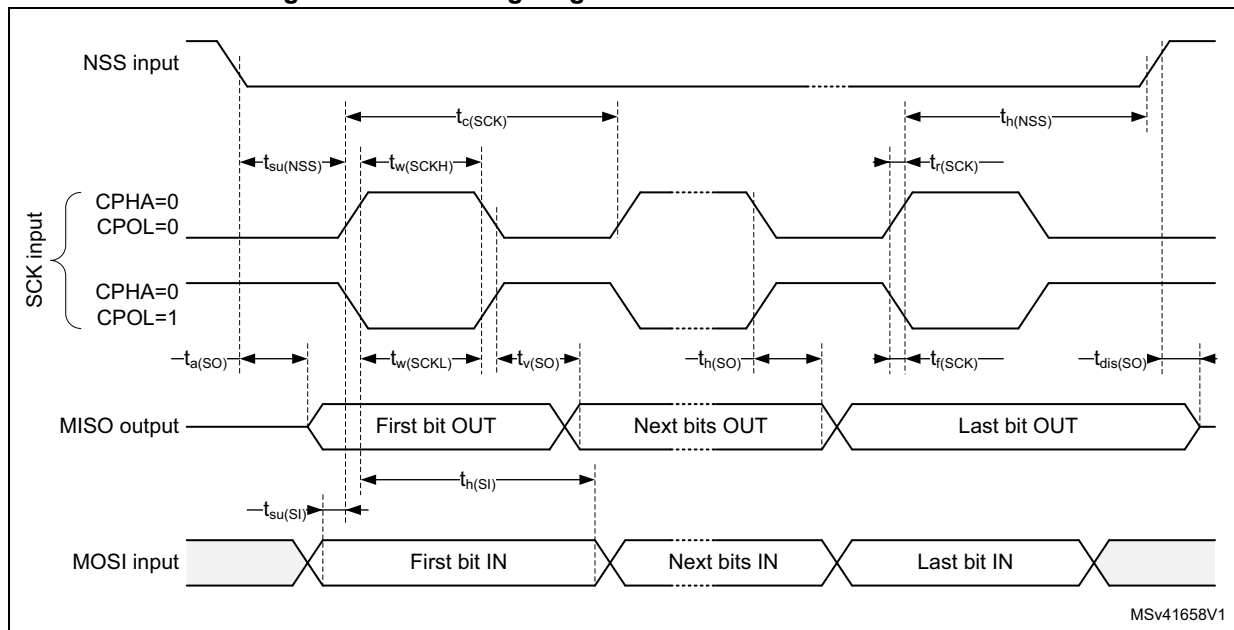
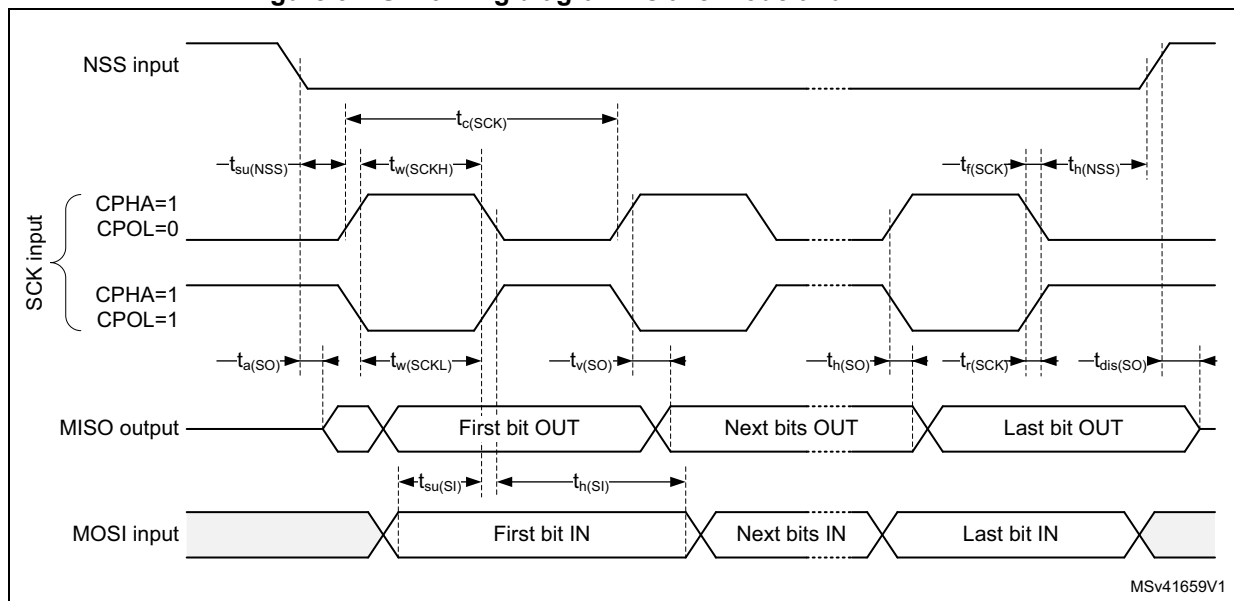
USART/LPUART characteristics

The parameters given in the following table are guaranteed by design.

Table 73. USART/LPUART characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$	Wakeup time needed to calculate the maximum USART/LPUART baudrate allowing to wake up from Stop mode when the USART/LPUART is clocked by HSI	Stop mode with main regulator in Run mode, Range 2 or 3	-	8.7	μs
		Stop mode with main regulator in Run mode, Range 1	-	8.1	
		Stop mode with main regulator in low-power mode, Range 2 or 3	-	12	
		Stop mode with main regulator in low-power mode, Range 1	-	11.4	

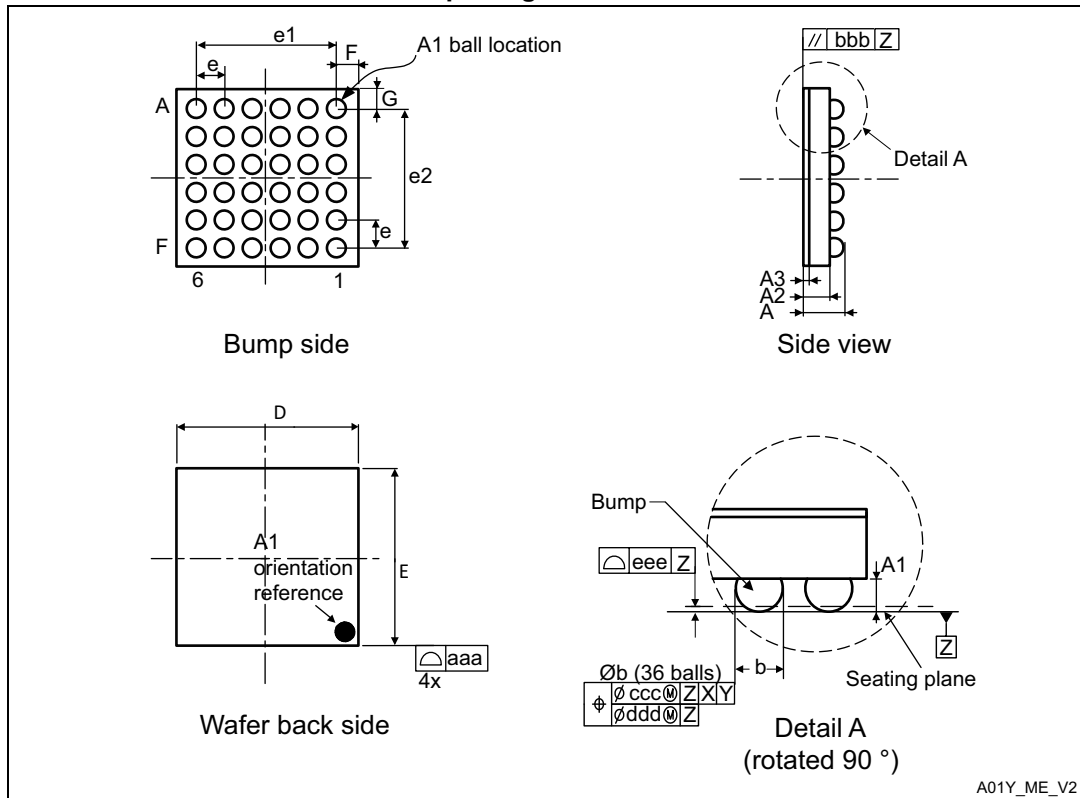
Figure 33. SPI timing diagram - slave mode and CPHA = 0

Figure 34. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7.4 Standard WLCSP36 package information

Figure 48. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.
2. b dimensions is measured at the maximum bump diameter parallel to primary datum Z

Table 85. Standard WLCSP36 - 2.61 x 2.88 mm, 0.4 mm pitch wafer level chip scale mechanical data

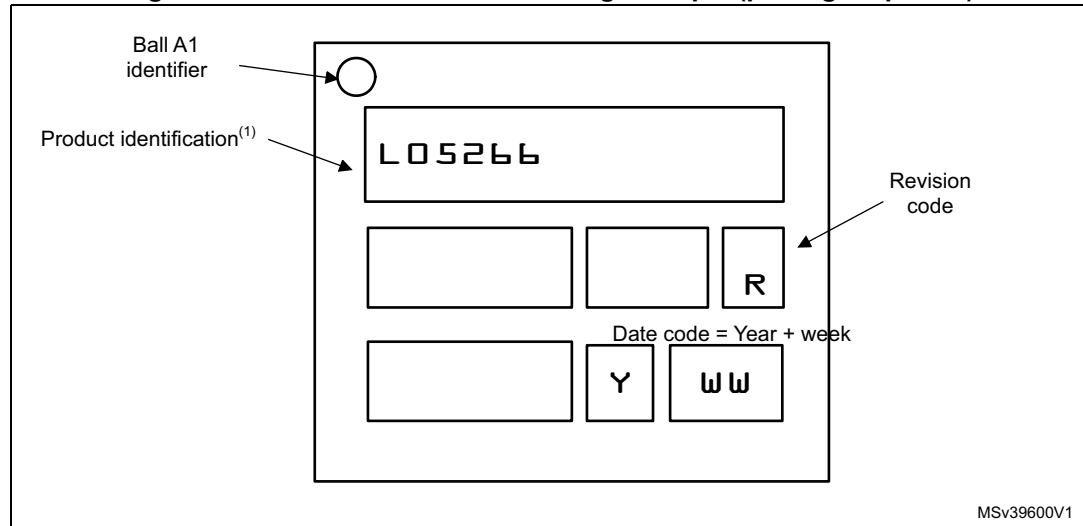
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.59	-	-	0.023
A1	-	0.18	-	-	0.007	-
A2	-	0.38	-	-	0.015	-
A3	-	0.025 ⁽²⁾	-	-	0.001	-
b	0.22	0.25	0.28	0.009	0.010	0.011
D	2.59	2.61	2.63	0.102	0.103	0.104
E	2.86	2.88	2.90	0.112	0.113	0.114
e	-	0.40	-	-	0.016	-
e1	-	2.00	-	-	0.079	-
e2	-	2.00	-	-	0.079	-

Device marking for standard WLCSP36

The following figure gives an example of topside marking versus ball A 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 50. Standard WLCSP36 marking example (package top view)



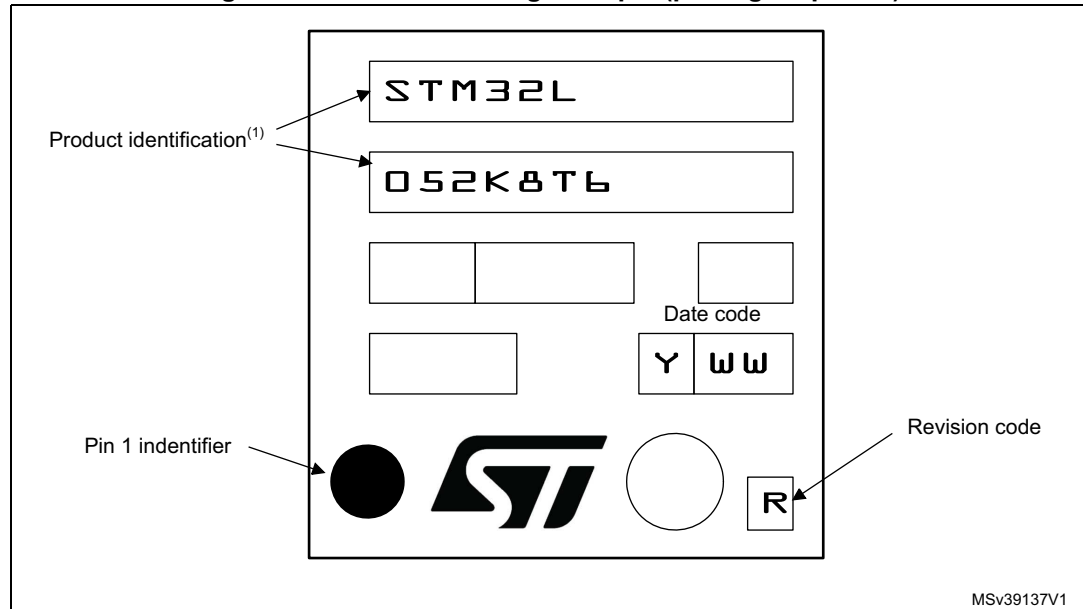
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Device marking for LQFP32

The following figure gives an example of topside marking versus pin 1 position identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

Figure 55. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip-junction temperature, $T_J \text{ max}$, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- $T_A \text{ max}$ is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D \text{ max}$ is the sum of $P_{INT} \text{ max}$ and $P_{I/O} \text{ max}$ ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- $P_{INT} \text{ max}$ is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O} \text{ max}$ represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 91. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient TFBGA64 - 5 x 5 mm / 0.5 mm pitch	61	°C/W
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch	45	
	Thermal resistance junction-ambient Standard WLCSP36 - 0.4 mm pitch	63	
	Thermal resistance junction-ambient Thin WLCSP36 - 0.4 mm pitch	59	
	Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch	55	
	Thermal resistance junction-ambient LQFP32 - 7 x 7 mm / 0.8 mm pitch	57	
	Thermal resistance junction-ambient UFQFPN32 - 5 x 5 mm / 0.5 mm pitch	38	