# Microchip Technology - TS68EN360VA25L Datasheet

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## Understanding Embedded - Microprocessors

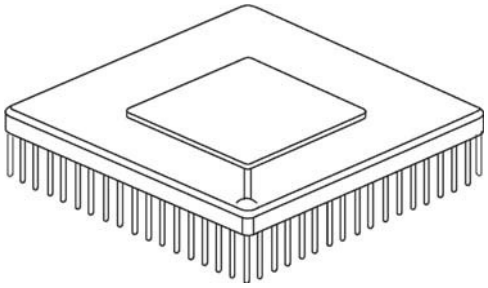
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

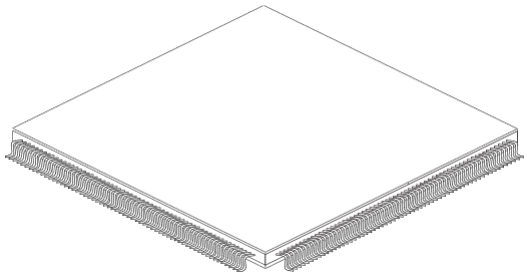
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | CPU32+ |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 25MHz |
| Co-Processors/DSP | Communications; CPM |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10Mbps (1) |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | -40°C ~ 85°C (TC) |
| Security Features | - |
| Package / Case | 240-BFCQFP |
| Supplier Device Package | 240-CERQUAD (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts68en360va25l |

**R suffix**
**PGA 241**
Ceramic Pin Grid Array Cavity Up



**A suffix**
**CERQUAD 240**
Ceramic Leaded Chip Carrier Cavity Down



# Introduction

## QUICC Architecture Overview

The QUICC is 32-bit controller that is an extension of other members of the TS68300 family. Like other members of the TS68300 family, the QUICC incorporates the inter-module bus (IMB). The TS68302 is an exception, having an 68000 bus on chip. The IMB provides a common interface for all modules of the TS68300 family, which allows the development of new devices more quickly by using the library of existing modules. Although the IMB definition always included an option for an on-chip 32-bit bus, the QUICC is the first device to implement this option.

The QUICC is comprised of three modules: the CPU32+ core, the SIM60, and the CPM. Each module utilizes the 32-bit IMB.

The TS68EN360 QUICC block diagram is shown in Figure 1.

**Figure 1.** QUICC Block Diagram

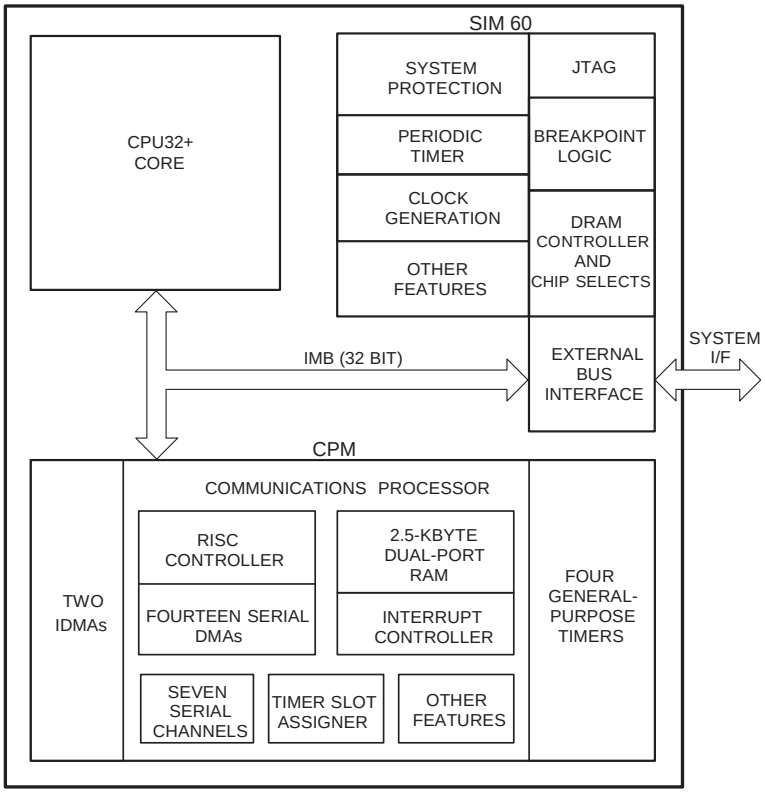


**Table 1.** System Bus Signal Index (Normal Operation) (Continued)

| Group | Signal Name | Mnemonic | Function |
|---|---|---|---|
| Bus Control | Data and Size Acknowledge | $\overline{\text{DSACK1}}$ - $\overline{\text{DSACK0}}$ | Provides asynchronous data transfer acknowledgement and dynamic bus sizing (open-drain I/O but driven high before three-stated). |
| | Address Strobe | $\overline{\text{AS}}$ | Indicates that a valid address is on the address bus. (I/O) |
| | Data Strobe | $\overline{\text{DS}}$ | During a read cycle, $\overline{\text{DS}}$ indicates that an external device should place valid data on the data bus. During a write cycle, $\overline{\text{DS}}$ indicates that valid data is on the data bus. (I/O) |
| | Size | SIZ1-SIZ0 | Indicates the number of bytes remaining to be transferred for this cycle. (I/O) |
| | Read/Write | R/$\overline{\text{W}}$ | Indicates the direction of data transfer on the bus. (I/O) |
| | Output Enable Address Multiplex | $\overline{\text{OE}}$/AMUX | Active during a read cycle indicates that an external device should place valid data on the data bus (O) or provides a strobe for external address multiplexing in DRAM accesses if internal multiplexing is not used. (O) |
| Interrupt Control | Interrupt Request Level 7-1 | $\overline{\text{IRQ7}}$-$\overline{\text{IRQ1}}$ | Provides external interrupt requests to the CPU32+ at priority levels 7-1. (I) |
| | Autovector/Interrupt Acknowledge 5 | $\overline{\text{AVEC}}$/$\overline{\text{IACK5}}$ | Autovector request during an interrupt acknowledge cycle (open-drain I/O) or interrupt level 5 acknowledge line. (O) |
| System Control | Soft Reset | $\overline{\text{RESETS}}$ | Soft system reset. (open-drain I/O) |
| | Hard Reset | $\overline{\text{RESETH}}$ | Hard system reset. (open-drain I/O) |
| | Halt | $\overline{\text{HALT}}$ | Suspends external bus activity. (open-drain I/O) |
| | Bus Error | $\overline{\text{BERR}}$ | Indicates an erroneous bus operation is being attempted. (open-drain I/O) |
| Clock and Test | System Clock Out 1 | CLKO1 | Internal system clock output 1. (O) |
| | System Clock Out 2 | CLKO2 | Internal system clock output 2 - normally 2x CLKO1. (O) |
| | Crystal Oscillator | EXTAL, XTAL | Connections for an external crystal to the internal oscillator circuit. EXTAL (I), XTAL (O). |
| | External Filter Capacitor | XFC | Connection pin for an external capacitor to filter the circuit of the PLL. (I) |
| | Clock Mode Select 1-0 | MODCK1-MODCK0 | Selects the source of the internal system clock. (I) THESE PINS SHOULD NOT BE SET TO 00 |
| | Instruction Fetch/ Development Serial Input | $\overline{\text{IFETCH}}$/DSI | Indicates when the CPU32+ is performing an instruction word prefetch (O) or input to the CPU32+ background debug mode. (I) |
| | Instruction Pipe 0/ Development Serial Output | $\overline{\text{IPIPE0}}$/DSO | Used to track movement of words through the instruction pipeline (O) or output from the CPU32+ background debug mode. (O) |
| | Instruction Pipe 1/Row Address Select 1 Double-Drive | $\overline{\text{IPIPE1}}$/$\overline{\text{RAS1DD}}$ | Used to track movement of words through the instruction pipeline (O), or a row address select 1 “double-drive” output (O). |
| | Breakpoint/Development Serial Clock | $\overline{\text{BKPT}}$/DSCLK | Signals a hardware breakpoint to the QUICC (open-drain I/O), or clock signal for CPU32+ background debug mode (I). |
| | Freeze/Initial Configuration 2 | FREEZE/CONFIG2 | Indicates that the CPU32+ has acknowledged a breakpoint (O), or initial QUICC configuration select (I). |

**Table 1.** System Bus Signal Index (Normal Operation) (Continued)

| Group | Signal Name | Mnemonic | Function |
|---|---|---|---|
| Clock and Test (Cont'd) | Three-State | $\overline{\text{TRIS}}$ | Used to three-state all pins if QUICC is configured as a master. Always Sampled except during system reset. (I) |
| | Test Clock | TCK | Provides a clock for Scan test logic. (I) |
| | Test Mode Select | TMS | Controls test mode operations. (I) |
| | Test Data In | TDI | Serial test instructions and test data signal. (I) |
| | Test Data Out | TDO | Serial test instructions and test data signal. (O) |
| | Test Reset | $\overline{\text{TRST}}$ | Provides an asynchronous reset to the test controller. (I) |
| Power | Clock Synthesizer Power | VCCSYN | Power supply to the PLL of the clock synthesizer. |
| | Clock Synthesizer Ground | GNDSYN | Ground supply to the PLL of the clock synthesizer. |
| | Clock Out Power | VCCCLK | Power supply to clock out pins. |
| | Clock Out Ground | GNDCLK | Ground supply to clock out pins. |
| | Special Ground 1 | GNDS1 | Special ground for fast AC timing on certain system bus signals. |
| | Special Ground 2 | GNDS2 | Special ground for fast AC timing on certain system bus signals. |
| | System Power Supply and Return | VCC, GND | Power supply and return to the QUICC. |
| -- | No Connect | NC4-NC1 | Four no-connect pins. |

Note: 1. I denotes input, O denotes output and I/O is input/output.

**Table 4.** Recommended Conditions Of Use
Unless otherwise stated, all voltages are referenced to the reference terminal.

| Symbol | Parameter | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage Range | | +4.75 | | +5.25 | V |
| $V_{IL}$ | Logic Low Level Input Voltage Range | | GND | | +0.8 | V |
| $V_{IH}$ | Logic High Level Input Voltage Range | | +2.0 | | $V_{CC}$ | V |
| $T_{case}$ | Operating Temperature | | -55 | | +125 | °C |
| $V_{OH}$ | High Level Output Voltage | | +2.4 | | | V |
| $f_{sys}$ | System Frequency | (For 25 MHz version) | | 25 | | MHz |
| | | (For 33 MHz version) | | 33 | | MHz |

**Table 5.** Thermal Characteristics

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $\theta_{JC}$ | Thermal Resistance - Junction to Case | 240-pin Cerquad | 2 | °C/W |
| | | 241-pin PGA | 7 | |
| $\theta_{JA}$ | Thermal Resistance - Junction to Ambient | 240-pin Cerquad | 27.4 | °C/W |
| | | 241-pin PGA | 22.8 | |

$T_J = T_A + (P_D \cdot \theta_{JA})$

$P_D = (V_{DD} \cdot I_{DD}) + P_{I/O}$

Where $P_{I/O}$ is the power dissipation on pins.

## Power Considerations

The average chip-junction temperature, $T_J$, in °C can be obtained from:

$$T_J = T_A \div (P_D \cdot \Theta_{JA}) \quad (1)$$

where:

$T_A$ = Ambient Temperature, °C

$\Theta_{JA}$ = Package Thermal Resistance, Junction-to-Ambient, C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \cdot V_{CC}$, Watts-chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins-User Determined

For most applications, $P_{I/O} < 0.3 \cdot P_{INT}$ and can be neglected.

An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \Theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from Equation (3) by measuring $P_D$ (at thermal equilibrium) for a know $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving Equations (1) and (2) iteratively for any value of $T_A$.

## Bus Operation AC Timing Specifications

GND = 0 Vdc, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7 to Figure 23).

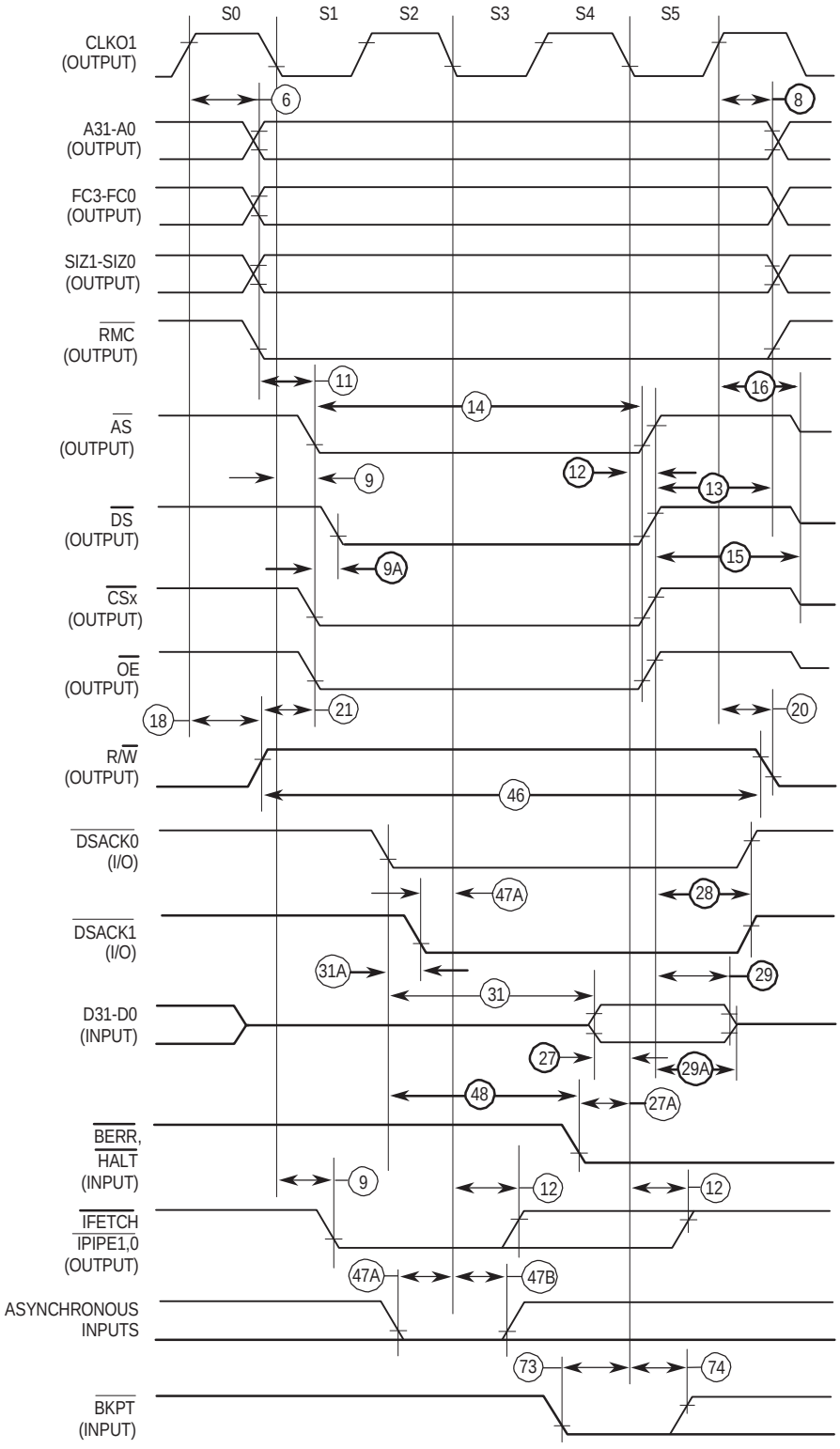
| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 6 | CLKO1 High to Address, FC, SIZ, RMC Valid | $t_{CHAV}$ | 0 | 15 | 0 | 12 | ns |
| 6A | CLKO1 High to Address Valid (GAMX = 1) | $t_{CHAV}$ | 0 | 20 | 0 | 15 | ns |
| 7 | CLKO1 High to Address, Data, FC, SIZ, RMC High Impedance | $t_{CHAZx}$ | 0 | 40 | 0 | 30 | ns |
| 8 | CLKO1 High to Address, Data, FC, SIZ, RMC Invalid | $t_{CHAZn}$ | -2 | - | -2 | - | ns |
| 9 | CLKO1 Low to AS, DS, OE, WE, IFETCH, IPIPE, IACKx Asserted | $t_{CLSA}$ | 3 | 20 | 3 | 15 | ns |
| 9[10] | CLKO1 Low to CSx/RASx Asserted | $t_{CLSA}$ | 4 | 16 | 4 | 12 | ns |
| 9B[11] | CLKO1 High to CSx/RASx Asserted | $t_{CHCA}$ | 4 | 16 | 4 | 12 | ns |
| 9A[2][10] | AS to DS or CSx/RASx or OE Asserted (Read) | $t_{STSA}$ | -6 | 6 | -5.625 | 5.625 | ns |
| 9C[2][11] | AS to CSx/RASx Asserted | $t_{STCA}$ | 14 | 26 | 9 | 21 | ns |
| 11[10] | Address, FC, SIZ, RMC, valid to AS, CSx/RASx, OE, WE, (and DS Read) Asserted | $t_{AVSA}$ | 10 | - | 8 | - | ns |
| 11A[11] | Address, FC, SIZ, RMC, Valid to CSx/RASx Asserted | $t_{AVCA}$ | 30 | - | 22.5 | - | ns |
| 12 | CLKO1 Low to AS, DS, OE, WE, IFETCH, IPIPE, IACKx Negated | $t_{CLSN}$ | 3 | 20 | 3 | 15 | ns |
| 12[16] | CLKO1 Low to CSx/RASx Negated | $t_{CLSN}$ | 4 | 16 | 4 | 12 | ns |
| 12A[13][16] | CLKO1 High to CSx/RASx Negated | $t_{CHCN}$ | 4 | 16 | 4 | 12 | ns |
| 12B | CS negate to WE negate (CSNTQ = 1) | Atmel$_{TW}$ | 15 | - | 12 | - | ns |
| 13[12] | AS, DS, CSx, OE, WE, IACKx Negated to Address, FC, SIZ Invalid (Address Hold) | $t_{SNAI}$ | 10 | - | 7.5 | - | ns |
| 13A[13] | CSx Negated to Address, FC, SIZ, Invalid (Address Hold) | $t_{CNAI}$ | 30 | - | 22.5 | - | ns |
| 14[10][12] | AS, CSx, OE, WE (and DS Read) Width Asserted | $t_{SWA}$ | 75 | - | 56.25 | - | ns |
| 14C[11][13] | CSx Width Asserted | $t_{CWA}$ | 35 | - | 26.25 | - | ns |
| 14A | DS Width Asserted (Write) | $t_{SWAW}$ | 35 | - | 26.25 | - | ns |
| 14B | AS, CSx, OE, WE, IACKx, (and DS Read) Width Asserted (Fast Termination Cycle) | $t_{SWDW}$ | 35 | - | 26.25 | - | ns |
| 14D[13] | CSx Width Asserted (Fast Termination Cycle) | $t_{CWDW}$ | 15 | - | 10 | - | ns |
| 15[3][10][12] | AS, DS, CSx, OE, WE Width Negated | $t_{SN}$ | 35 | - | 26.25 | - | ns |
| 16 | CLKO1 High to AS, DS, R/W High Impedance | $t_{CHSZ}$ | - | 40 | - | 30 | ns |
| 17[12] | AS, DS, CSx, WE Negated to R/W High | $t_{SNRN}$ | 10 | - | 7.5 | - | ns |
| 17A[13] | CSx Negated to R/W High | $t_{CNRN}$ | 30 | - | 22.5 | - | ns |
| 18 | CLKO1 High to R/W High | $t_{CHRH}$ | 0 | 20 | 0 | 15 | ns |

## Bus Operation AC Timing Specifications (Continued)

GND = 0 Vdc, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 7 to Figure 23).

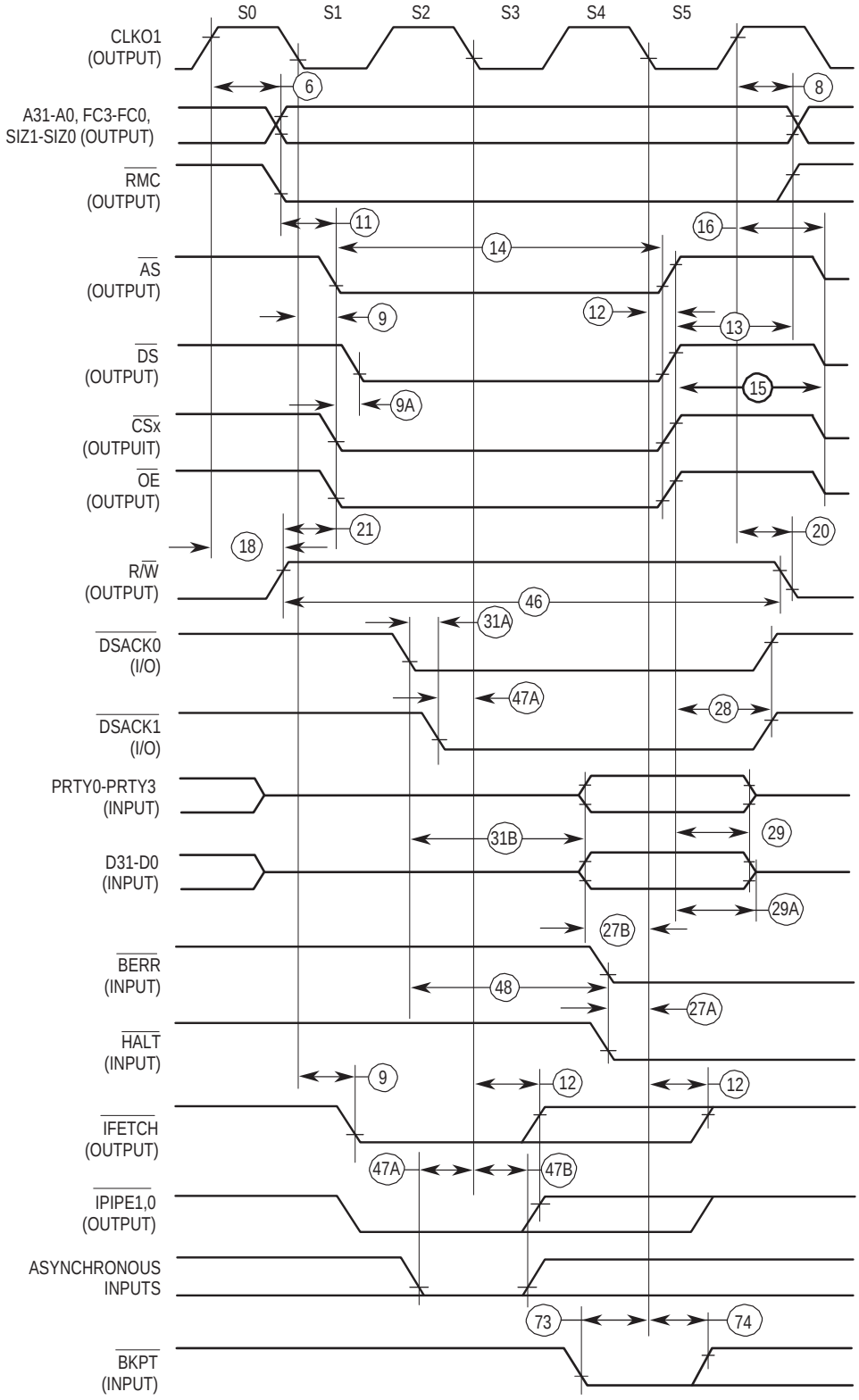
| Number | Characteristic | Symbol | 25 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 20 | CLKO1 High to R/$\overline{W}$ Low | $t_{CHRL}$ | 3 | 20 | 3 | 15 | ns |
| 21[10] | R/$\overline{W}$ High to $\overline{AS}$, $\overline{CSx}$, $\overline{OE}$ Asserted | $t_{RAAA}$ | 10 | - | 7.5 | - | ns |
| 21A[11] | R/$\overline{W}$ High to $\overline{CSx}$ Asserted | $t_{RACA}$ | 30 | - | | - | ns |
| 22 | R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write) | $t_{RASA}$ | 47 | - | 36 | - | ns |
| 23 | CLKO1 High to Data-Out | $t_{CHDO}$ | - | 23 | - | 18 | ns |
| 23A | CLKO1 High to Parity Valid | $t_{CHPV}$ | - | 25 | - | 20 | ns |
| 23B | Parity Valid to $\overline{CAS}$ Low | $t_{PVCL}$ | 3 | - | 3 | - | ns |
| 24[12] | Data-Out, Parity-Out Valid to Negating Edge of $\overline{AS}$, $\overline{CSx}$, $\overline{WE}$, (Fast Termination Write) | $t_{DVASN}$ | 10 | - | 7.5 | - | ns |
| 25[12] | $\overline{DS}$, $\overline{CSX}$, $\overline{WE}$ Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold) | $t_{SNDOI}$ | 10 | - | 7.5 | - | ns |
| 25A[13] | $\overline{CSx}$ Negated to Data-Out, Parity-Out Invalid (Data-Out, Parity-Out Hold) | $t_{CNDOI}$ | 35 | - | 25 | - | ns |
| 26 | Data-Out, Parity-Out Valid to $\overline{DS}$ Asserted (Write) | $t_{DVSA}$ | 10 | - | 7.5 | - | ns |
| 27[15] | Data-In, Parity-In to CLKO1 Low (Data-Setup) | $t_{DICL}$ | 1 | - | 1 | - | ns |
| 27B[14] | Data-In, Parity-In Valid to CLKO1 Low (Data-Setup) | $t_{DICL}$ | 20 | - | 15 | - | ns |
| 27A | Late $\overline{BERR}$, $\overline{HALT}$, $\overline{BKPT}$ Asserted to CLKO1 Low (Setup Time) | $t_{BELCL}$ | 10 | - | 7.5 | - | ns |
| 28[18] | $\overline{AS}$, $\overline{DS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$ Negated | $t_{SNDN}$ | 0 | 50 | 0 | 37.5 | ns |
| 29[4] | $\overline{DS}$, $\overline{CSx}$, $\overline{OE}$, Negated to Data-In Parity-In Invalid (Data-In, Parity-In Hold) | $t_{SNDI}$ | 0 | - | 0 | - | ns |
| 29A[4] | $\overline{DS}$, $\overline{CSx}$, $\overline{OE}$ Negated to Data-In High Impedance | $t_{SHDI}$ | - | 40 | - | 30 | ns |
| 30[4] | CLKO1 Low to Data-In, Parity-In Invalid (Fast Termination Hold) | $t_{CLDI}$ | 10 | - | 7.5 | - | ns |
| 30A[4] | CLKO1 Low to Data-In High Impedance | $t_{CLDH}$ | - | 60 | - | 45 | ns |
| 31[5][15] | $\overline{DSACKx}$ Asserted to Data-in, Parity-In Valid | $t_{DADI}$ | - | 32 | - | 24 | ns |
| 31A | $\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew) | $t_{DADV}$ | - | 10 | - | 7.5 | ns |
| 31B[5][14] | $\overline{DSACKx}$ Asserted to Data-in, Parity-In Valid | $t_{DADI}$ | - | 35 | - | 26 | ns |
| 32 | $\overline{HALT}$ an $\overline{RESET}$ Input Transition Time | $t_{HRrf}$ | - | 140 | - | | ns |
| 33 | CLKO1 High to $\overline{BG}$ Asserted | $t_{CLBA}$ | - | 20 | - | 15 | ns |
| 34 | CLKO1 High to $\overline{BG}$ Negated | $t_{CLBN}$ | - | 20 | 22.5 | 15 | ns |
| 35[6] | $\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted) | $t_{BRAGA}$ | 1 | - | 1 | - | CLKO1 |
| 37 | $\overline{BGACK}$ Asserted to $\overline{BG}$ Negated | $t_{GAGN}$ | 1 | 2.5 | 1 | 2.5 | CLKO1 |
| 39 | $\overline{BG}$ Width Negated | $t_{GH}$ | 2 | - | 2 | - | CLKO1 |
| 39A | $\overline{BG}$ Width Asserted | $t_{GA}$ | 1 | - | 1 | - | CLKO1 |

**Figure 7.** Read Cycle




Note: All timing is shown with respect to 0.8V and 2.0V levels.

**Figure 9.** Read Cycle (With Parity Check, PBEE = 1)




Note: All timing is shown with respect to 0.8V and 2.0V levels.

**Figure 13.** Fast Termination Write Cycle

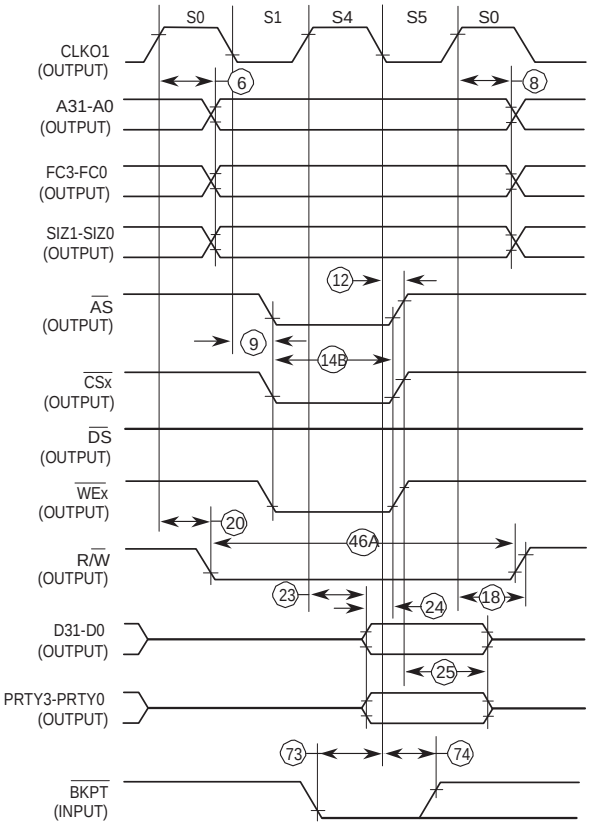



**Figure 14.** SRAM: Fast Termination Write Cycle (CSNTQ = 1)

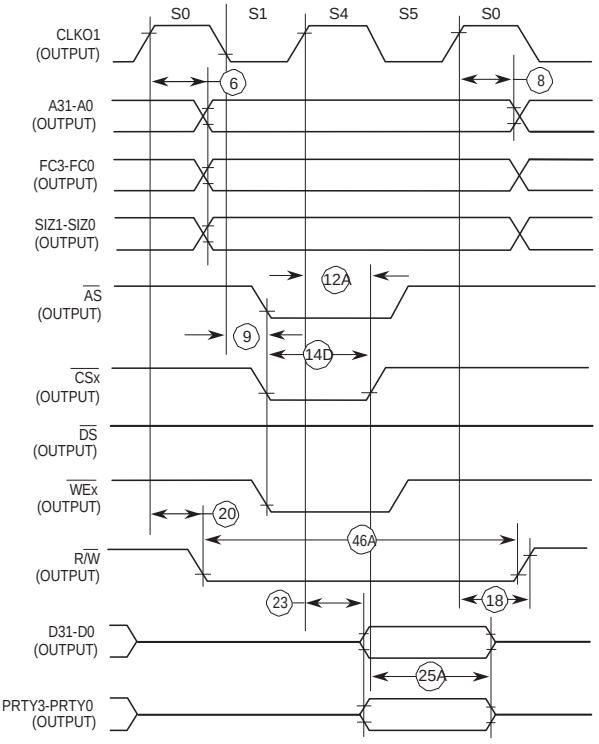


**Figure 17.** ASYNC Bus Arbitration – Active Bus Case

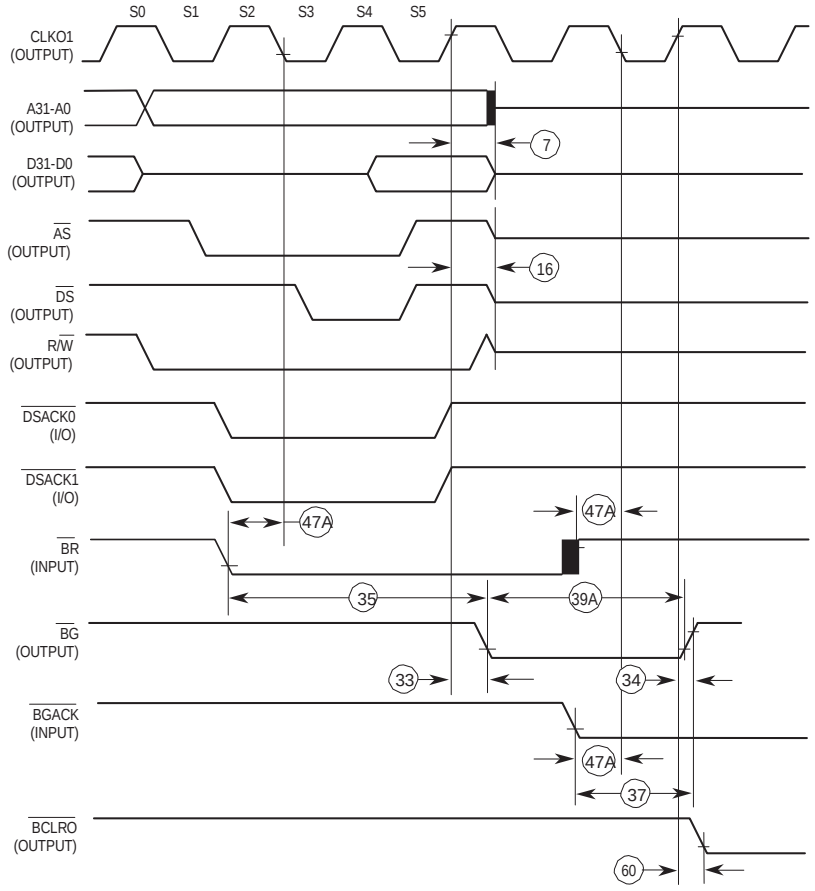
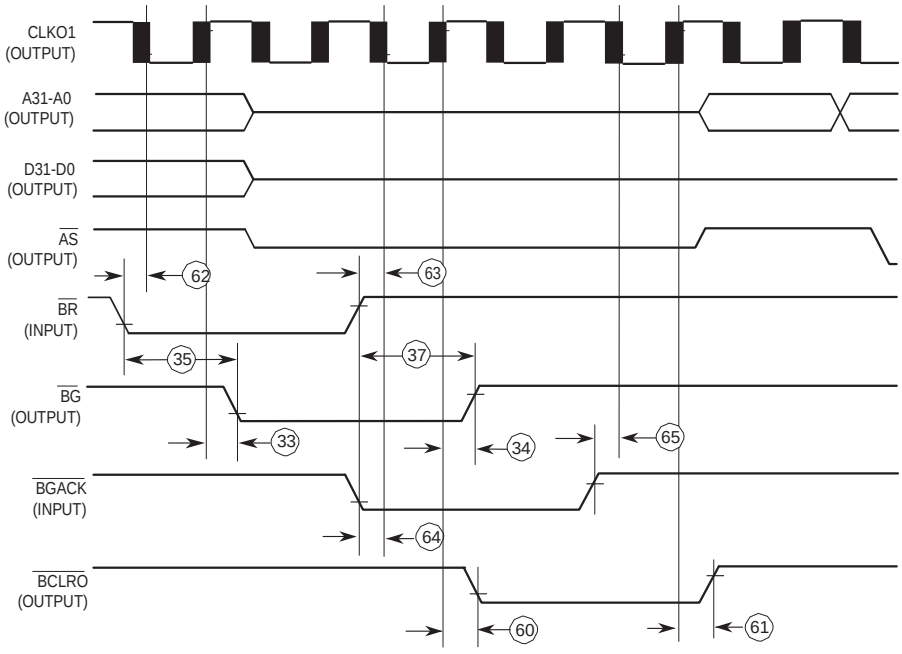



**Figure 18.** SYNC Bus Arbitration – IDLE Bus Case

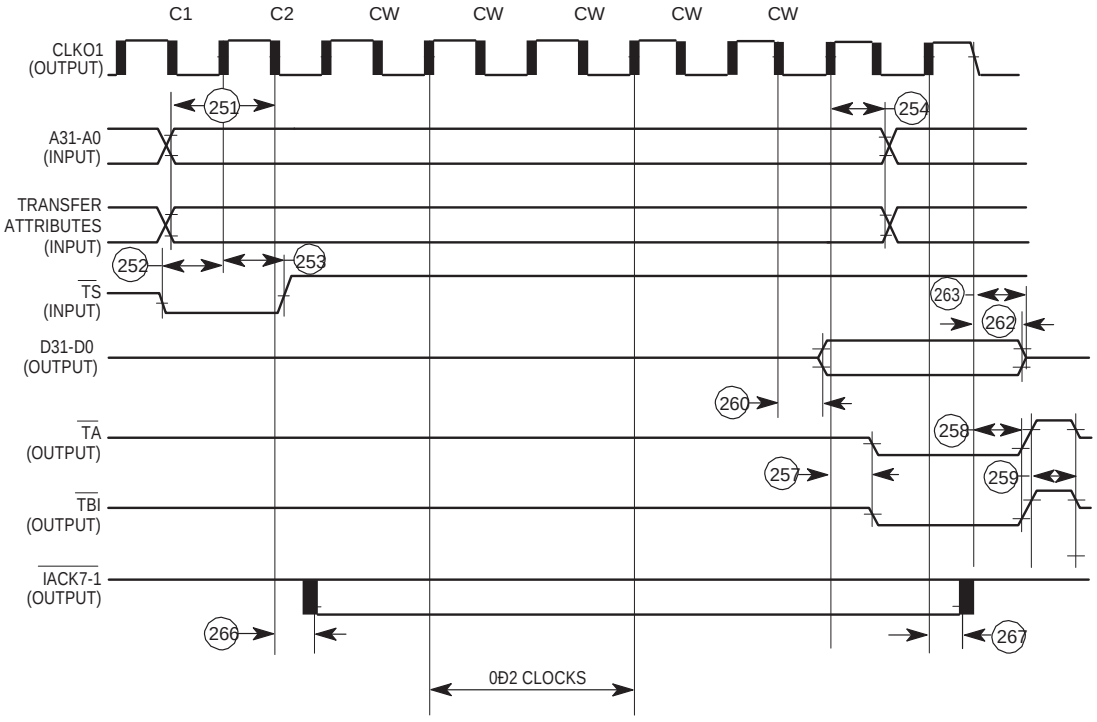


## Bus Operation - DRAM Accesses AC Timing Specification

GND = 0 Vdc, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 24 to Figure 28).

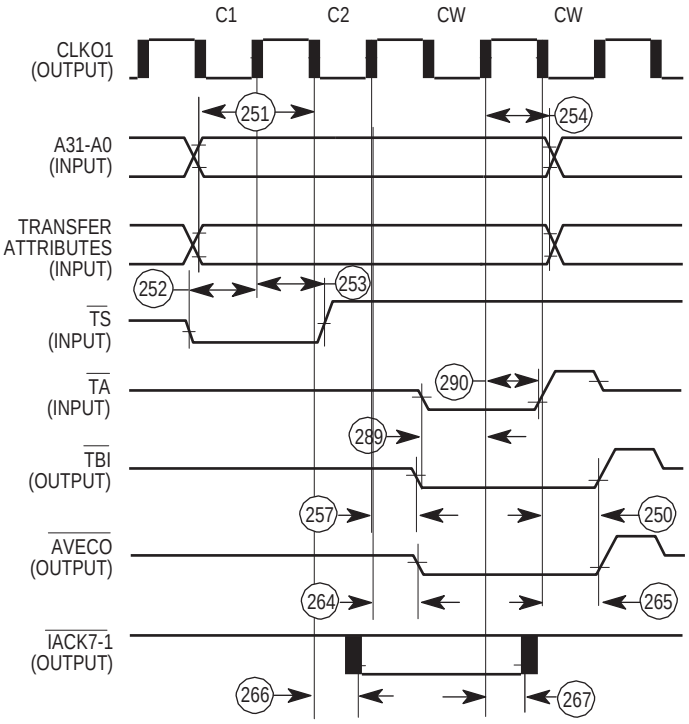
| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 100 | $\overline{RASx}$ Asserted to Row Address Invalid | 15 | | 11.25 | | ns |
| 101 | $\overline{RASx}$ Asserted to column Address Valid | 20 | | 15 | | ns |
| 102 | $\overline{RASx}$ Width Asserted | 75 | | 56.25 | | ns |
| 103A | $\overline{RASx}$ width Negated (Back to back Cycle) Non page mode @ WBTQ = 0 | 75 | | 56.25 | | ns |
| 103B | $\overline{RASx}$ width Negated (Back to back Cycle) Page mode @ WBTQ = 0 | 55 | | 41.25 | | ns |
| 103C | $\overline{RASx}$ width Negated (Back to back Cycle) Non page mode @ WBTQ = 1 | 115 | | 86.25 | | ns |
| 103D | $\overline{RASx}$ width Negated (Back to back Cycle) Page mode @ WBTQ = 1 | 95 | | 69.23 | | ns |
| 104 | $\overline{RASx}$ Asserted to $\overline{CASx}$ Asserted | 35 | | 26.25 | | ns |
| 105 | CLKO1 Low to $\overline{CASx}$ Asserted | 3 | 13 | 2 | 10 | ns |
| 105A | CLKO1 High to $\overline{CASx}$ Asserted (Refresh Cycle) | 3 | 13 | 2 | 10 | ns |
| 106 | CLKO1 High to $\overline{CASx}$ Negated | 3 | 13 | 2 | 10 | ns |
| 107 | Column Address Valid to $\overline{CASx}$ Asserted | 15 | | 11.25 | | ns |
| 108 | $\overline{CASx}$ Asserted to Column Address Negated | 40 | | 30 | | ns |
| 109 | $\overline{CASx}$ Asserted to $\overline{RASx}$ Negated | 35 | | 27 | | ns |
| 110 | $\overline{CASx}$ Width Asserted | 50 | | 37.5 | | ns |
| 111[1] | $\overline{CASx}$ Width Negated (Back to Back Cycles) | 95 | | 71.25 | | ns |
| 111A | $\overline{CASx}$ Width Negated (Page Mode) | 20 | | 15 | | ns |
| 113 | $\overline{WE}$ Low to $\overline{CASx}$ Asserted | 35 | | 27 | | ns |
| 114 | $\overline{CASx}$ Asserted to $\overline{WE}$ Negated | 35 | | 27 | | ns |
| 115 | R/$\overline{W}$ Low to $\overline{CASx}$ Asserted (Write) | 52.5 | | 40 | | ns |
| 116 | $\overline{CASx}$ Asserted to R/$\overline{W}$ High (Write) | 55 | | 41.25 | | ns |
| 117 | Data-Out, Parity-Out Valid to $\overline{CASx}$ Asserted | 10 | | 7.5 | | ns |
| 119 | CLKO1 High to AMUX Negated | 3 | 16 | 2 | 12 | ns |
| 120 | CLKO1 High to AMUX Asserted | 3 | 16 | 2 | 12 | ns |
| 121 | AMUX High to $\overline{RASx}$ Asserted | 15 | | 11.25 | | ns |
| 122 | $\overline{RASx}$ Asserted to AMUX Low | 15 | | 11.25 | | ns |
| 123 | AMUX Low to $\overline{CASx}$ Asserted | 15 | | 11.25 | | ns |
| 124 | $\overline{CASx}$ Asserted to AMUX High | 55 | | 41.25 | | ns |
| 125 | $\overline{RAS}$/$\overline{CASx}$ Negated to R/$\overline{W}$ change | 0 | | 0 | | ns |

**Figure 32.** TS68040 IACK Cycles (Vector Driven)




Notes: 1. TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/$\overline{W}$, $\overline{LOCK}$.
2. Up to two wait states may be inserted for internal peripheral.

**Figure 33.** TS68040 IACK Cycles (No Vector Driven)




Note: TS68040 Transfer Attribute Signals = SIZx, TTx, TMx, R/$\overline{W}$, $\overline{LOCK}$.

**Figure 53.** SI Transmit Timing with Double Speed Clocking (DSC = 1)

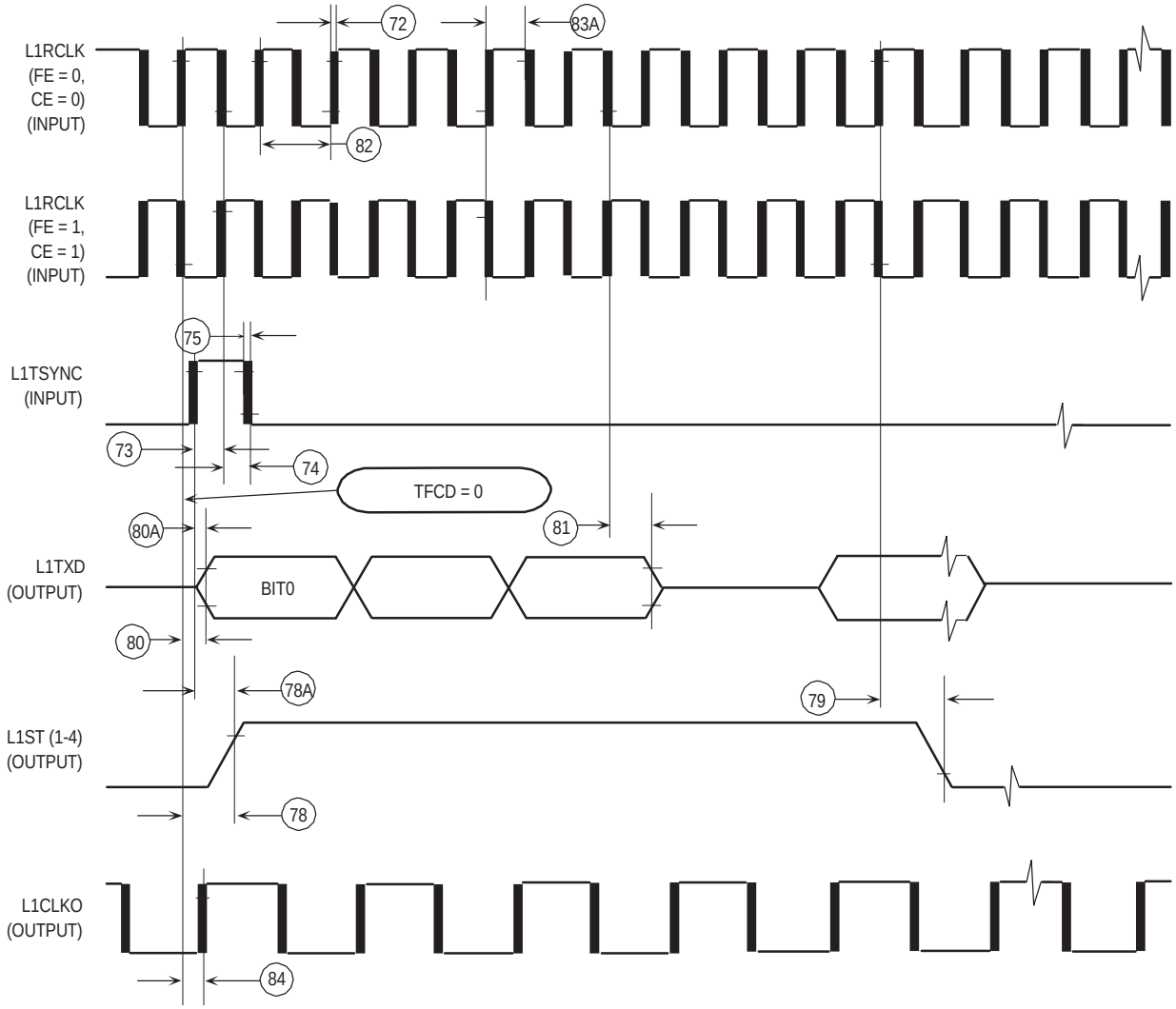
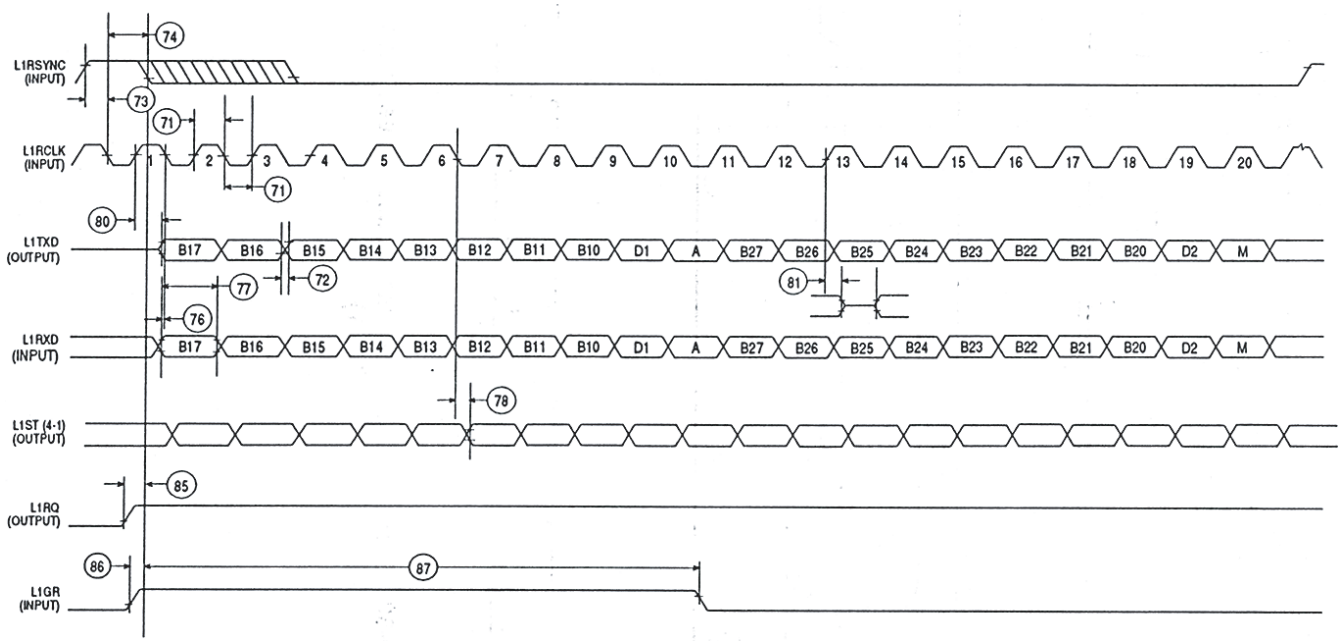


**Figure 54.** IDL Timing SI Transmit Timing with Double Speed Clocking (DSC = 1)




## SCC in NMSI Mode-external Clock Electrical Specifications

GND = 0 $V_{DC}$, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 55 to Figure 57).

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 100(1) | RCLK1 and TCLK1 Width High | CLKO1 | - | CLKO1 | - | |
| 101 | RCLK1 and TCLK1 Width Low | CLKO1 + 5 ns | - | CLKO1 + 5 ns | - | |
| 102 | RCLK1 and TCLK1 Rise/Fall Time | - | 15 | - | 15 | ns |
| 103 | TXD1 Active Delay (From TCLK1 Falling Edge) | 0 | 50 | 0 | 50 | ns |
| 104 | $\overline{RTS1}$ Active/Inactive Delay (From TCLK1 Falling Edge) | 0 | 50 | 0 | 50 | ns |
| 105 | $\overline{CTS1}$ Setup Time to TCLK1 Rising Edge | 40 | - | 40 | - | ns |
| 106 | RXD1 Setup Time to RCLK1 Rising Edge | 40 | - | 40 | - | ns |
| 107(2) | RXD1 Hold Time from RCLK1 Rising Edge | 0 | - | 0 | - | ns |
| 108 | $\overline{CD1}$ Setup Time to RCLK1 Rising Edge | 40 | - | 40 | - | ns |

Notes: 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1.
2. Also applies to $\overline{CD}$ and $\overline{CTS}$ hold time when they are used as external sync signals.

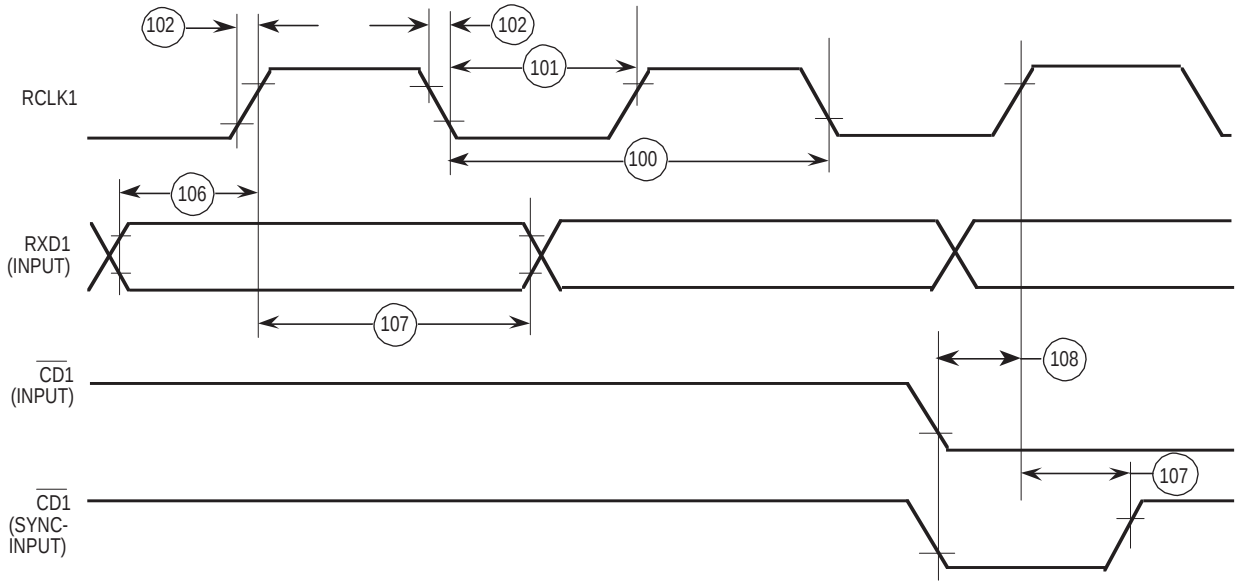
## SCC in NMSI Mode-internal Clock Electrical Specifications

GND = 0 $V_{dc}$, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 55 to Figure 57).

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 100(1) | RCLK1 and TCLK1 Frequency | 0 | 8.3 | 0 | 11 | MHz |
| 102 | RCLK1 and TCLK1 Rise/Fall Time | - | - | - | - | ns |
| 103 | TXD1 Active Delay (From TCLK1 Falling Edge) | 0 | 30 | 0 | 30 | ns |
| 104 | $\overline{RTS1}$ Active/Inactive Delay (From TCLK1 Falling Edge) | 0 | 30 | 40 | - | ns |
| 105 | $\overline{CTS1}$ Setup Time to TCLK1 Rising Edge | 40 | - | 40 | - | ns |
| 106 | RXD1 Setup Time to RCLK1 Rising Edge | 40 | - | 0 | - | ns |
| 107(2) | RXD1 Hold Time from RCLK1 Rising Edge | 0 | - | 40 | - | ns |
| 108 | $\overline{CD1}$ Setup Time to RCLK1 Rising Edge | 40 | - | 0 | 30 | ns |

Notes: 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 3/1.
2. Also applies to $\overline{CD}$ and $\overline{CTS}$ hold time when they are used as external sync signals.

**Figure 55.** SCC NMSI Receive



## Ethernet Electrical Specifications

GND = 0 $V_{dc}$, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 58 to Figure 63).

| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 120 | CLSN Width High | 40 | - | 40 | - | ns |
| 121 | RCLK1 Rise/Fall Time | - | 15 | - | 15 | ns |
| 122 | RCLK1 Width Low | CLKO1 + 5 ns | - | CLKO1 + 5 ns | - | |
| 123(1) | RCLK1 Width High | CLKO1 | - | CLKO1 | - | |
| 124 | RXD1 Setup Time | 20 | - | 20 | - | ns |
| 125 | RXD1 Hold Time | 5 | - | 5 | - | ns |
| 126 | RENA Active Delay (from RCLK1 rising edge of the last data bit) | 10 | - | 10 | - | ns |
| 127 | RENA Width Low | 100 | - | 100 | - | ns |
| 128 | TCLK1 Rise/Fall Time | - | 15 | - | 15 | ns |
| 129 | TCLK1 Width Low | CLKO1 + 5 ns | - | CLKO1 + 5 ns | - | |
| 130(1) | TCLK1 Width High | CLKO1 | - | CLKO1 | - | |
| 131 | TXD1 Active Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 132 | TXD1 Inactive Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 133 | TENA Active Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 134 | TENA Inactive Delay (from TCLK1 rising edge) | 10 | 50 | 10 | 50 | ns |
| 135 | RSTRT Active Delay (from TCLK1 falling edge) | 10 | 50 | 10 | 50 | ns |
| 136 | RSTRT Inactive Delay (from TCLK1 falling edge) | 10 | 50 | 10 | 50 | ns |
| 137 | RRJCT Width Low | 1 | - | 1 | - | CLKO1 |
| 138(2) | CLKO1 Low to $\overline{\text{SDACK}}$ Asserted | - | 20 | - | 20 | ns |
| 139(2) | CLKO1 Low to $\overline{\text{SDACK}}$ Negated | - | 20 | - | 20 | ns |

Notes: 1. SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2.25/1
2. $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

**Figure 58.** Ethernet Collision Timing

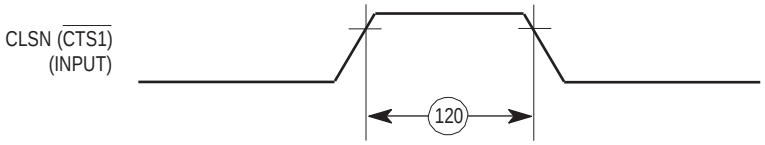


**Figure 59.** Ethernet Receive Timing

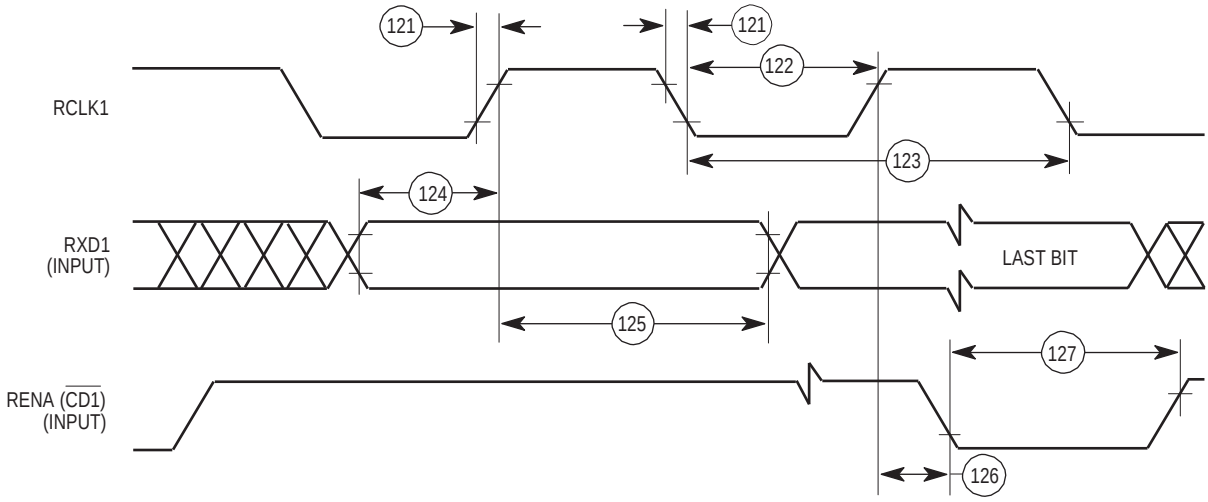
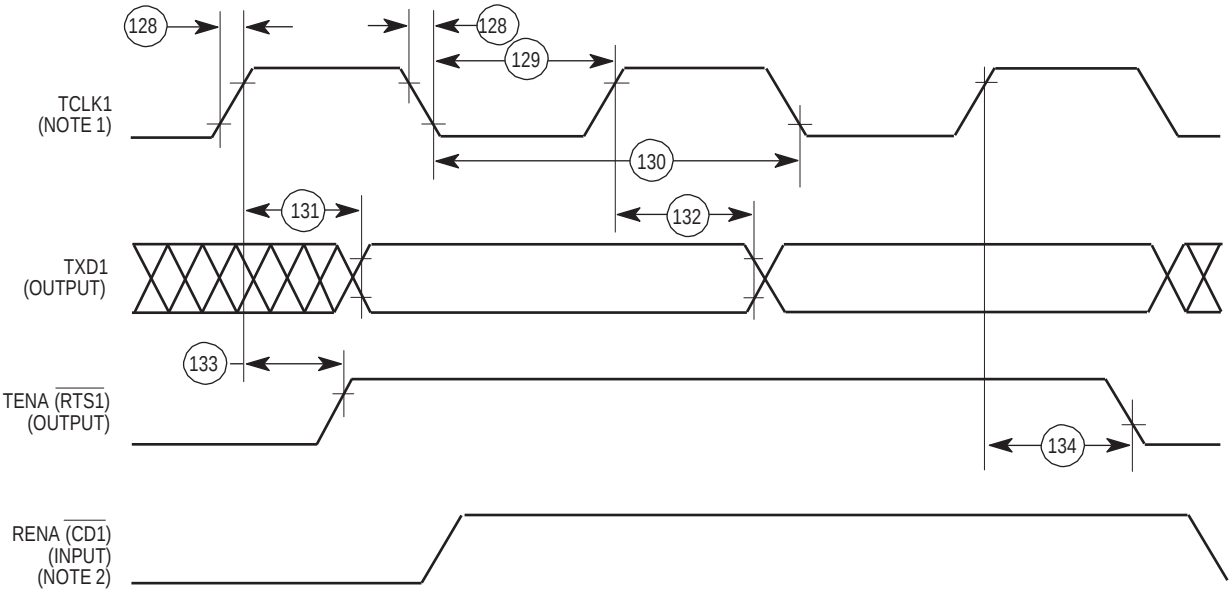
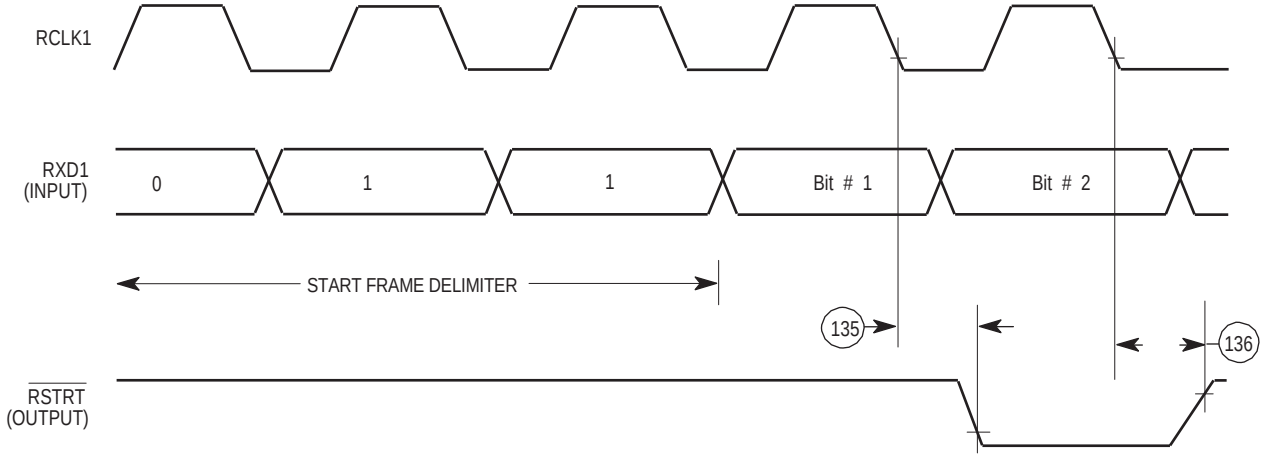



**Figure 60.** Ethernet Transmit Timing



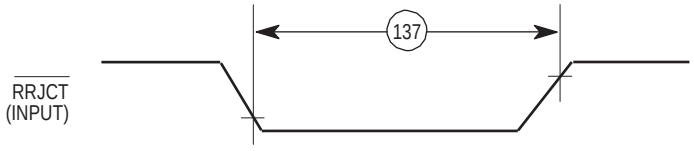

Notes: 1. Transmit clock invert (TCI) bit in GSMR is set.
2. If RENA is deasserted before TENA, or RENA is not asserted at all during transit, then CSL bit is set in the buffer descriptor at the end of frame transmission.

**Figure 61.** CAM Interface Receive Start Timing



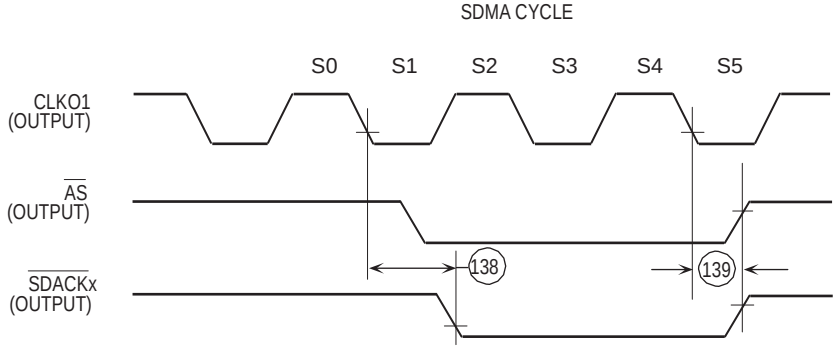

Note: Valid for the ethernet protocol only.

**Figure 62.** CAM Interface Reject Timing




Note: Valid for the ethernet protocol only.

**Figure 63.** SDACK Timing Diagram




Note: SDACKx is asserted when the SDMA writes the received Ethernet frame into memory.

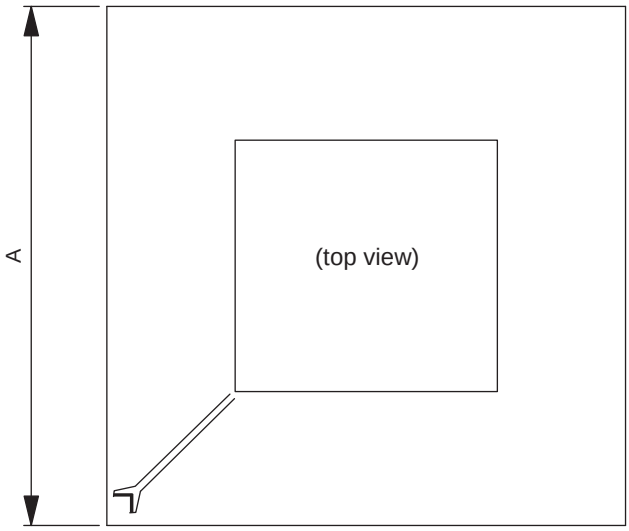
## SMC Transparent Mode Electrical Specifications

GND = 0 $V_{DC}$, $T_C$ = -55 to +125°C. The electrical specifications in this document are preliminary (See Figure 64).

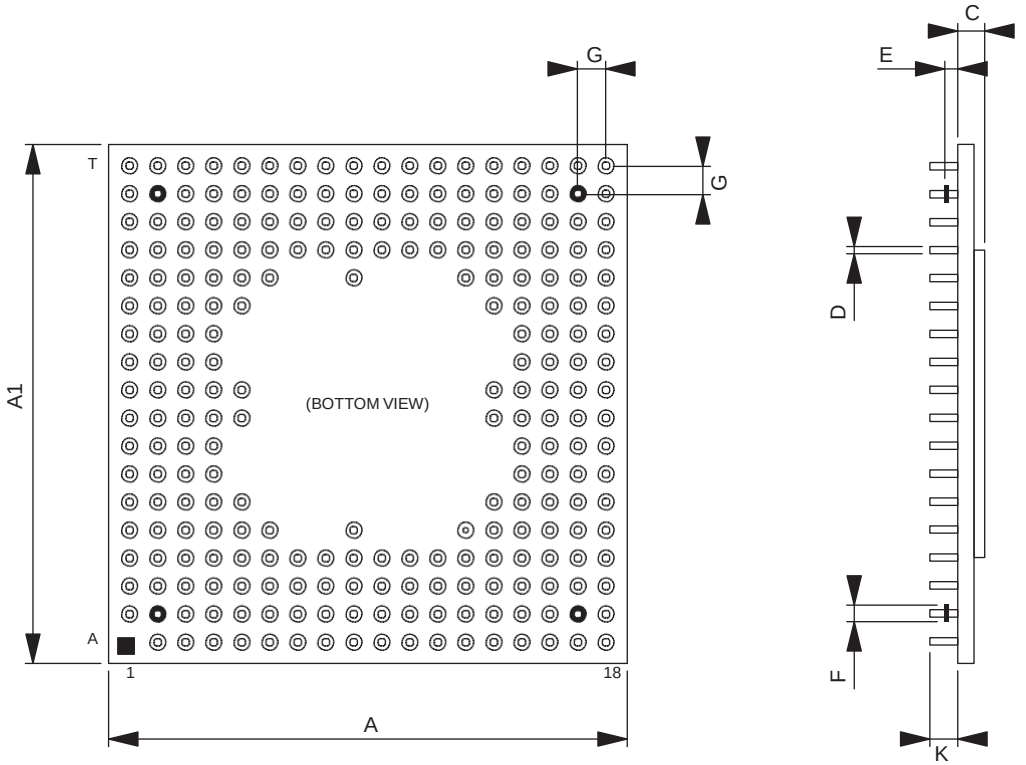
| Number | Characteristic | 25.0 MHz | | 33.34 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 150(1) | SMCLK Clock Period | 100 | - | 100 | - | ns |
| 151 | SMCLK Width Low | 50 | - | 50 | - | ns |
| 151A | SMCLK Width High | 50 | - | 50 | - | ns |

## Package Mechanical Data

### 241-pin – PGA




| Dim | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.840 | 1.880 | 46.74 | 47.75 |
| C | 0.110 | 0.140 | 2.79 | 3.56 |
| D | 0.016 | 0.020 | 0.41 | 0.51 |
| E | 0.045 | 0.055 | 1.143 | 1.4 |
| F | 0.045 | 0.055 | 1.143 | 1.4 |
| G | 0.100 BASIC | | 2.54 BASIC | |
| K | 0.150 | 0.170 | 3.81 | 4.32 |



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