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## Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

### Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	125
Number of Logic Elements/Cells	1000
Total RAM Bits	65536
Number of I/O	18
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	25-XFBGA, WLCSP
Supplier Device Package	25-WLCSP (1.7x1.7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lm1k-swg25tr50">https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lm1k-swg25tr50</a>

**Table 1-1. iCE40LM Family Selection Guide**

Part Number	iCE40LM1K	iCE40LM2K	iCE40LM4K
Logic Cells (LUT + Flip-Flop)	1000	2000	3520
RAM4K Memory Blocks	16	20	20
RAM4K RAM Bits	64K	80K	80K
Package	Programmable I/O Count		
25-pin WLCSP, 1.71 x 1.71 mm, 0.35mm	18	18	18
36-pin ucBGA, 2.5 x 2.5 mm, 0.40mm	28	28	28
49-pin ucBGA, 3 x 3 mm, 0.40mm	37	37	37

## Introduction

The iCE40LM family of ultra-low power FPGAs has three devices with densities ranging from 1000 to 3520 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), two Strobe Generators (LPSG, HSSG), two hardened I<sup>2</sup>C Controllers and two hardened SPI Controllers. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications,

The iCE40LM devices are fabricated on a 40nm CMOS low power process. The device architecture has several features such as user configurable I<sup>2</sup>C and SPI Controllers, either as master or slave, and two Strobe Generators.

The iCE40LM FPGAs are available in very small form factor packages, with the smallest in 25-pin WLCSP. The 25-pin WLCSP package has a 0.35mm ball pitch, resulting to an overall package size of 1.71mm x 1.71mm that easily fits into a lot of mobile applications. Table 1-1 shows the LUT densities, package and I/O pin count.

The iCE40LM devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

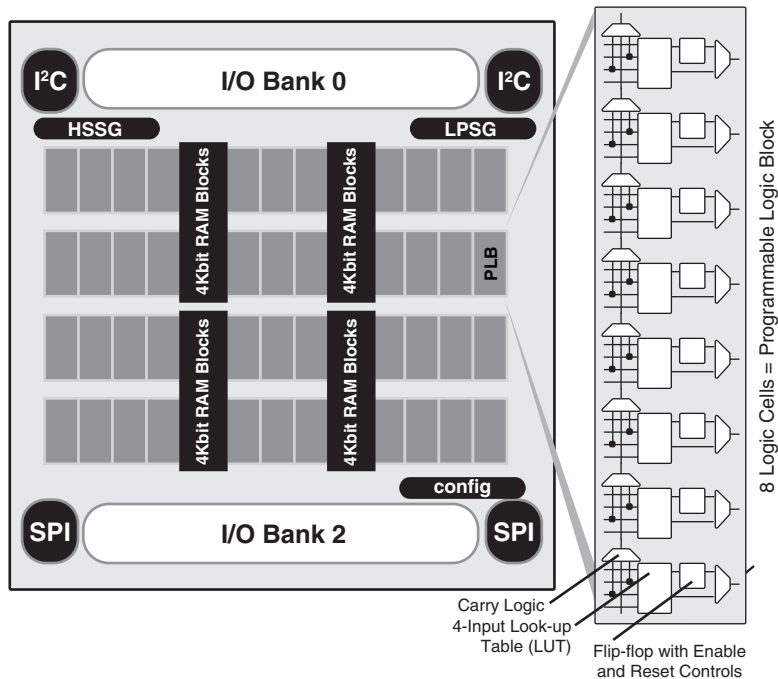
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40LM family of devices. Popular logic synthesis tools provide synthesis library support for iCE40LM. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40LM device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40LM FPGA family. Lattice also can provide fully verified bit-stream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice’s Reference Designs or fully-verified bitstreams, please contact your local Lattice representative.

## Architecture Overview

The iCE40LM family architecture contains an array of Programmable Logic Blocks (PLB), two Strobe Generators, two user configurable I<sup>2</sup>C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE40LM-4K device.

Figure 2-1. iCE40LM-4K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

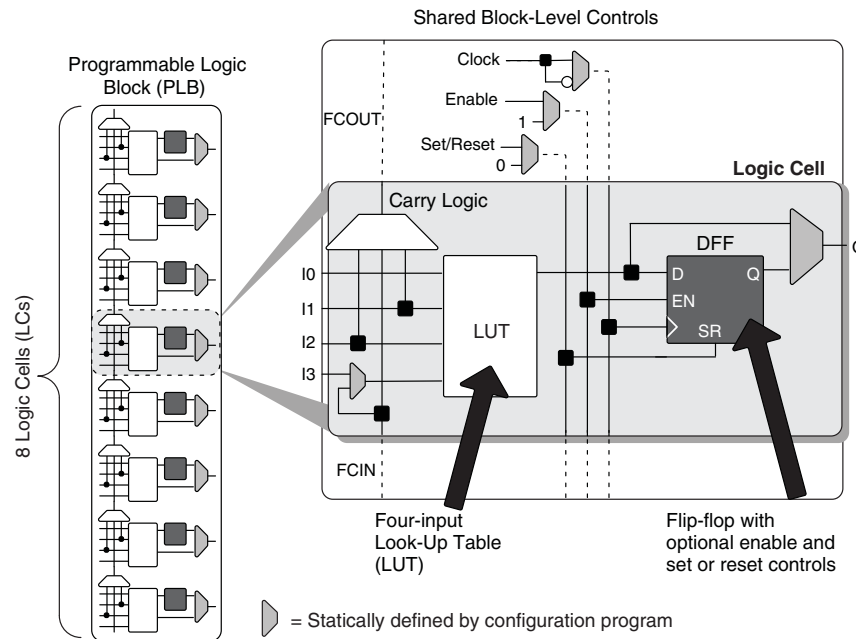
In the iCE40LM family, There are two sysIO banks, one on top and one on bottom. User can connect both V<sub>CCIO</sub>s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 Kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40LM also includes two user I<sup>2</sup>C ports, and two Strobe Generators.

## PLB Blocks

The core of the iCE40LM device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

**Figure 2-2. PLB Block Diagram**



## Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

**Table 2-1. Logic Cell Signal Descriptions**

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset <sup>1</sup>	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

## Routing

There are many resources provided in the iCE40LM devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

## Clock/Control Distribution Network

Each iCE40LM device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and the global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Strobe Generators (GBUF4 connects to LPSG, GBUF5 connects to HSSG).

**Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks**

Global Buffer	LUT Inputs	Clock	Clock Enable	Reset
GBUF0	Yes, any 4 of 8 GBUF Inputs	✓	✓	
GBUF1		✓		✓
GBUF2		✓	✓	
GBUF3		✓		✓
GBUF4		✓	✓	
GBUF5		✓		✓
GBUF6		✓	✓	
GBUF7		✓		✓

The maximum frequency for the global buffers are shown in the iCE40LM External Switching Characteristics tables later in this document.

### Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40LM device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

### Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40LM device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

**sysCLOCK Phase Locked Loops (PLLs) - NOT SUPPORTED on the 25-Pin WLCSP**

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40LM devices have one sysCLOCK PLL (Please note that the 25-pin WLCSP package does not support the PLL). REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal strobe generator or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

The iCE40LM PLL functions the same as the PLLs in the iCE40 family. For more details on the PLL, see TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-3. PLL Diagram**

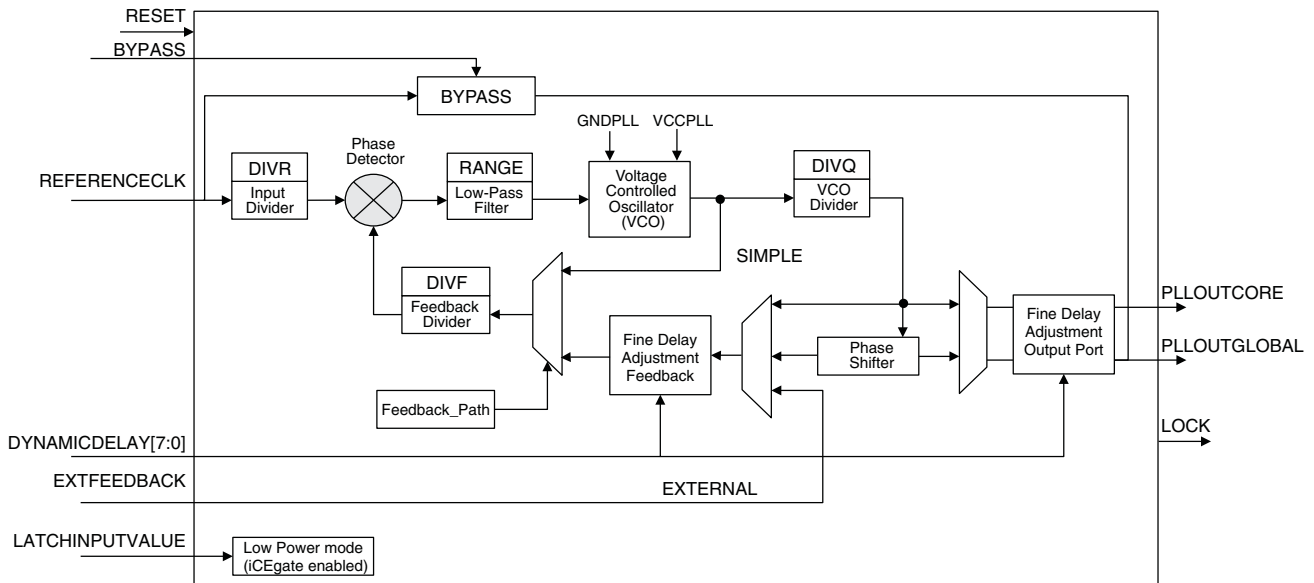


Table 2-3 provides signal descriptions of the PLL block.

**Table 2-3. PLL Signal Descriptions**

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

### sysMEM Embedded Block RAM Memory

Larger iCE40LM device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 Kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

#### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

**Table 2-4. sysMEM Block Configurations<sup>1</sup>**

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40LM EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

Figure 2-6. iCE I/O Register Block Diagram

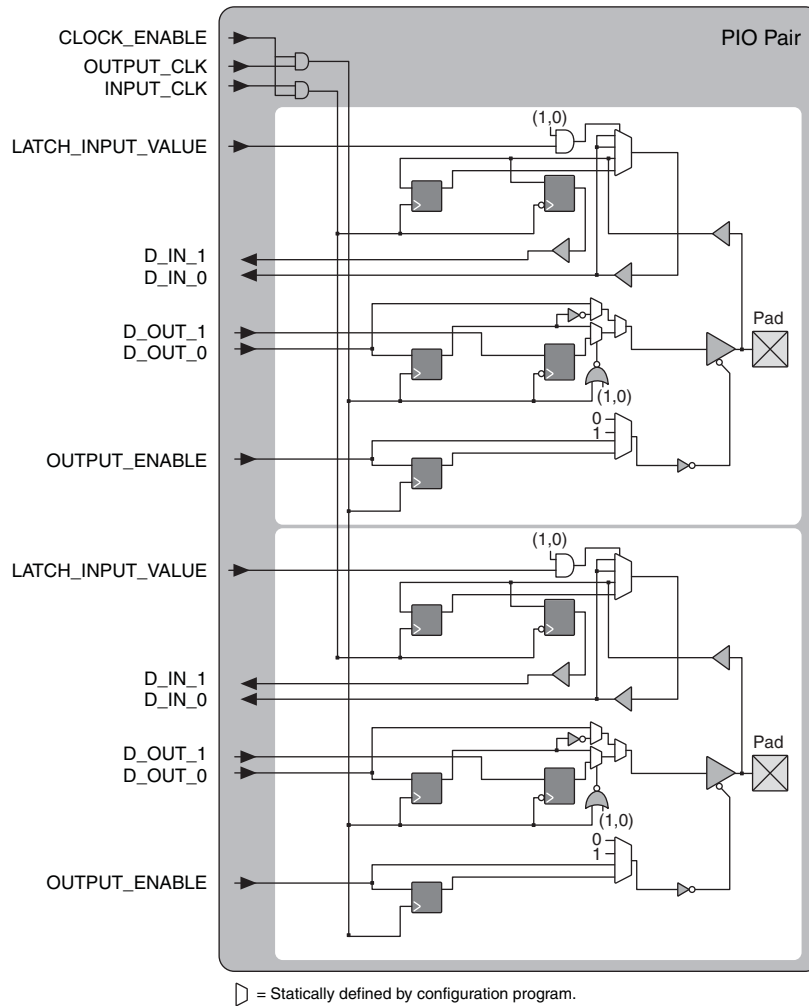


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.



**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO\_2}$  and  $V_{CC\_SPI}$  ( $V_{CC\_SPI}$  is connected to  $V_{CCIO\_2}$  on the 25-pin WLCSP) reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to  $V_{CCIO}$ . The I/O pins maintain the pre-configuration state until  $V_{CC}$  and  $V_{CCIO\_2}$  reach the defined levels. The I/Os take on the software user-configured settings only after  $V_{CC\_SPI}$  reaches the level and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

**Supported Standards**

The iCE40LM sysIO buffer supports all single-ended input and output standards. The buffer supports the LVCMOS 1.8, 2.5, and 3.3V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40LM devices.

**Table 2-7. Supported Input Standards**

Input Standard	$V_{CCIO}$ (Typical)		
	3.3V	2.5V	1.8V
<b>Single-Ended Interfaces</b>			
LVC MOS33	✓		
LVC MOS25		✓	
LVC MOS18			✓

**Table 2-8. Supported Output Standards**

Output Standard	$V_{CCIO}$ (Typical)
<b>Single-Ended Interfaces</b>	
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8

**On-Chip Strobe Generators**

The iCE40LM devices feature two different Strobe Generators. One is tailored for low-power operation (Low Power Strobe Generator – LPSG), and generates periodic strobes in the Microsecond ( $\mu$ s) ranges. The other is tailored for high speed operation (High Speed Strobe Generator – HSSG), and generates periodic strobes in the Nanosecond (ns) ranges. Add a paragraph:

The Strobe Generators (HSSG and LPSG) provide fixed periodic strobes, and these strobes can be used as a clock source. When used as a clock source, the HSSG can provide strobe frequency in the range of 5MHz - 20MHz. The LPSG can provide strobe frequency in the range of 4KHz - 20KHz.

For further information on how to use the LPSG and HSSG, please refer to TN1275, [iCE40LM On-Chip Strobe Generator Usage Guide](#).

## iCE40LM Configuration

This section describes the programming and configuration of the iCE40LM family.

### Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40LM, please see TN1248, [iCE40 Programming and Configuration](#).

### Power Saving Options

The iCE40LM devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-9 describes the function of these features.

**Table 2-9. iCE40LM Power Saving Features Description**

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

## Power-On-Reset Voltage Levels<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units	
V <sub>PORUP</sub>	Power-On-Reset ramp-up trip point (circuit monitoring V <sub>CC</sub> , V <sub>CCIO_2</sub> and V <sub>CC_SPI</sub> )	V <sub>CC</sub>	0.64	0.99	V
		V <sub>CCIO_2</sub> , V <sub>CC_SPI</sub>	0.70	1.59	V
V <sub>PORDN</sub>	Power-On-Reset ramp-down trip point (circuit monitoring V <sub>CC</sub> , V <sub>CCIO_2</sub> and V <sub>CC_SPI</sub> )	V <sub>CC</sub>	—	0.66	V
		V <sub>CCIO_2</sub> , V <sub>CC_SPI</sub>	—	1.59	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

## Power Up Sequence

For all iCE40LM devices, it is required to have the V<sub>CC</sub>/V<sub>CCPLL</sub> power supply powered up before all other power supplies. The V<sub>CC</sub>/V<sub>CCPLL</sub> has to be higher than 0.5V before other supplies are powered from GND.

Following V<sub>CC</sub>/V<sub>CCPLL</sub>, V<sub>CCSPI</sub> should be ramped up, followed by the remaining supplies. For 25-pin WLCSP, V<sub>CC\_SPI</sub> is connected to V<sub>CCIO\_2</sub>, and the V<sub>CCPLL</sub> is internally connected for that package.

## ESD Performance

Please contact Lattice Semiconductor for additional information.

## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I <sub>IL</sub> , I <sub>IH</sub> <sup>1,3,4</sup>	Input or I/O Leakage	0V < V <sub>IN</sub> < V <sub>CCIO</sub> + 0.2V	—	—	+/-10	μA
C <sub>1</sub>	I/O Capacitance <sup>2</sup>	V <sub>CCIO</sub> = 3.3V, 2.5V, 1.8V V <sub>CC</sub> = Typ., V <sub>IO</sub> = 0 to V <sub>CCIO</sub> + 0.2V	—	6	—	pf
C <sub>2</sub>	Global Input Buffer Capacitance <sup>2</sup>	V <sub>CCIO</sub> = 3.3V, 2.5V, 1.8V V <sub>CC</sub> = Typ., V <sub>IO</sub> = 0 to V <sub>CCIO</sub> + 0.2V	—	6	—	pf
V <sub>HYST</sub>	Input Hysteresis	V <sub>CCIO</sub> = 1.8V, 2.5V, 3.3V	—	200	—	mV
I <sub>PU</sub>	Internal PIO Pull-up Current	V <sub>CCIO</sub> = 1.8V, 0=<V <sub>IN</sub> <=0.65 V <sub>CCIO</sub>	-3	—	-31	μA
		V <sub>CCIO</sub> = 2.5V, 0=<V <sub>IN</sub> <=0.65 V <sub>CCIO</sub>	-8	—	-72	μA
		V <sub>CCIO</sub> = 3.3V, 0=<V <sub>IN</sub> <=0.65 V <sub>CCIO</sub>	-11	—	-128	μA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.

2. T<sub>J</sub> 25°C, f = 1.0 MHz.

3. Please refer to V<sub>IL</sub> and V<sub>IH</sub> in the sysIO Single-Ended DC Electrical Characteristics table of this document.

4. Some products are clamped to a diode when V<sub>IN</sub> is larger than V<sub>CCIO</sub>.

## sysIO Recommended Operating Conditions

Standard	V <sub>CCIO</sub> (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89

## sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V <sub>IL</sub>		V <sub>IH</sub> <sup>1</sup>		V <sub>OL</sub> Max. (V)	V <sub>OH</sub> Min. (V)	I <sub>OL</sub> Max. (mA)	I <sub>OH</sub> Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	-0.3	0.8	2.0	V <sub>CCIO</sub> + 0.2V	0.4	V <sub>CCIO</sub> - 0.5	8	-8
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVC MOS 2.5	-0.3	0.7	1.7	V <sub>CCIO</sub> + 0.2V	0.4	V <sub>CCIO</sub> - 0.5	6	-6
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1
LVC MOS 1.8	-0.3	0.35V <sub>CCIO</sub>	0.65V <sub>CCIO</sub>	V <sub>CCIO</sub> + 0.2V	0.4	V <sub>CCIO</sub> - 0.4	4	-4
					0.2	V <sub>CCIO</sub> - 0.2	0.1	-0.1

1. Some products are clamped to a diode when V<sub>IN</sub> is larger than V<sub>CCIO</sub>.

## Typical Building Block Function Performance<sup>1,2</sup>

### Pin-to-Pin Performance (LVC MOS25)

Function	Timing	Units
<b>Basic Functions</b>		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

### Register-to-Register Performance

Function	Timing	Units
<b>Basic Functions</b>		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
<b>Embedded Memory Functions</b>		
256x16 Pseudo-Dual Port RAM	150	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

2. Using a V<sub>CC</sub> of 1.14V at Junction Temp 85C.

## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

### Maximum sysIO Buffer Performance<sup>1</sup>

I/O Standard	Max. Speed	Units
<b>Inputs</b>		
LVC MOS33		MHz
LVC MOS25		MHz
LVC MOS18		MHz
<b>Outputs</b>		
LVC MOS33		MHz
LVC MOS25		MHz
LVC MOS18		MHz

1. Measured with a toggling pattern

## iCE40LM Family Timing Adders

Over Recommended Commercial Operating Conditions<sup>1, 2, 3</sup>

Buffer Type	Description	Timing	Units
<b>Input Adjusters</b>			
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3V$	0.18	nS
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5V$	0.00	nS
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8V$	0.19	nS
<b>Output Adjusters</b>			
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3V$	-0.12	nS
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5V$	0.00	nS
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8V$	1.32	nS

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Condition table.

3. Commercial timing numbers are shown.

## iCE40LM External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device			Units
<b>Clocks</b>					
<b>Global Clocks</b>					
$f_{MAX\_GBUF}$	Frequency for Global Buffer Clock network	All devices		185	MHz
$t_{W\_GBUF}$	Clock Pulse Width for Global Buffer	All devices	TBD	—	ns
$t_{SKEW\_GBUF}$	Global Buffer Clock Skew Within a Device	All devices	—	650	ps
<b>Pin-LUT-Pin Propagation Delay</b>					
$t_{PD}$	Best case propagation delay through one LUT logic	All devices	—	14.0	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock without PLL)</b>					
$t_{SKEW\_IO}$	Data bus skew across a bank of IOs	All devices	—	400	ps
$t_{CO}$	Clock to Output - PIO Output Register	All devices	—	9.0	ns
$t_{SU}$	Clock to Data Setup - PIO Input Register	All devices		—	ns
$t_H$	Clock to Data Hold - PIO Input Register	All devices	5.55	—	ns
<b>General I/O Pin Parameters (Using Global Buffer Clock with PLL)<sup>1</sup></b>					
$t_{CO}$	Clock to Output - PIO Output Register	All devices	—	TBD	ns
$t_{SU}$	Clock to Data Setup - PIO Output Register	All devices	TBD	—	ns
$t_H$	Clock to Data Hold - PIO Output Register	All devices	TBD	—	ns
1. 25-pin WLCSP package does not support PLL.					

## sysCLOCK PLL Timing – Preliminary

Over Recommended Operating Conditions

Parameter	Descriptions	Conditions	Min.	Max.	Units
$f_{IN}$	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)		TBD	TBD	MHz
$f_{OUT}$	Output Clock Frequency (PLLOUT)		TBD	TBD	MHz
$f_{VCO}$	PLL VCO Frequency		TBD	TBD	MHz
$f_{PFD}$	Phase Detector Input Frequency		TBD	TBD	MHz
<b>AC Characteristics</b>					
$t_{DT}$	Output Clock Duty Cycle			TBD	%
$t_{PH}$	Output Phase Accuracy		—	TBD	deg
$t_{OPJIT}^{1,5}$	Output Clock Period Jitter	$f_{OUT} \leq 100$ MHz	—	TBD	ps p-p
		$f_{OUT} > 100$ MHz	—	TBD	UIPP
	Output Clock Cycle-to-cycle Jitter	$f_{OUT} \leq 100$ MHz	—	TBD	ps p-p
		$f_{OUT} > 100$ MHz	—	TBD	UIPP
	Output Clock Phase Jitter	$f_{PFD} \leq 25$ MHz	—	TBD	ps p-p
		$f_{PFD} > 25$ MHz	—	TBD	UIPP
$t_W$	Output Clock Pulse Width	At 90% or 10%		TBD	ns
$t_{LOCK}^{2,3}$	PLL Lock-in Time		—	TBD	us
$t_{UNLOCK}$	PLL Unlock Time		—	TBD	ns
$t_{IPJIT}^4$	Input Clock Period Jitter	$f_{PFD} \geq 20$ MHz	—	TBD	ps p-p
		$f_{PFD} < 20$ MHz	—	TBD	UIPP
$t_{FDTAP}$	Fine Delay adjustment, per Tap		—	TBD	ps
$t_{STABLE}^3$	LATCHINPUTVALUE LOW to PLL Stable		—	TBD	ns
$t_{STABLE\_PW}^3$	LATCHINPUTVALUE Pulse Width		—	TBD	ns
$t_{RST}$	RESET Pulse Width		TBD	TBD	ns
$t_{RSTREC}$	RESET Recovery Time		TBD	TBD	ns
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width		TBD	TBD	VCO Cycles

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. At minimum  $f_{PFD}$ . As the  $f_{PFD}$  increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

## SPI Master Configuration Time<sup>1</sup>

Symbol	Parameter	Conditions	Max.	Units
t <sub>CONFIG</sub>	POR/CRESET_B to Device I/O Active	All devices - Low Frequency (Default)	70	ms
		All devices - Medium frequency	35	ms
		All devices - High frequency	18	ms

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

## sysCONFIG Port Timing Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>All Configuration Modes</b>						
t <sub>CRESET_B</sub>	Minimum CRESET_B LOW pulse width required to restart configuration, from falling edge to rising edge		200	—	—	ns
t <sub>DONE_IO</sub>	Number of configuration clock cycles after CDONE goes HIGH before the PIO pins are activated		49	—	—	Cycles
<b>Slave SPI</b>						
t <sub>CR_SCK</sub>	Minimum time from a rising edge on CRESET_B until the first SPI WRITE operation, first SPI_XCK clock. During this time, the iCE40LM device is clearing its internal configuration memory		1200	—	—	us
f <sub>MAX</sub>	CCLK clock frequency	Write	1	—	25	MHz
		Read <sup>1</sup>	—	15	—	MHz
t <sub>CCLKH</sub>	CCLK clock pulsewidth HIGH		20	—	—	ns
t <sub>CCLKL</sub>	CCLK clock pulsewidth LOW		20	—	—	ns
t <sub>STSU</sub>	CCLK setup time		12	—	—	ns
t <sub>STH</sub>	CCLK hold time		12	—	—	ns
t <sub>STCO</sub>	CCLK falling edge to valid output		13	—	—	ns
<b>Master SPI</b>						
f <sub>MCLK</sub>	MCLK clock frequency	Low Frequency (Default)	6			MHz
		Medium Frequency <sup>2</sup>	18			MHz
		High Frequency <sup>2</sup>	31			MHz
t <sub>MCLK</sub>	CRESET_B HIGH to first MCLK edge		1200	—	—	us

1. Supported with 1.2V V<sub>CC</sub> and at 25C.

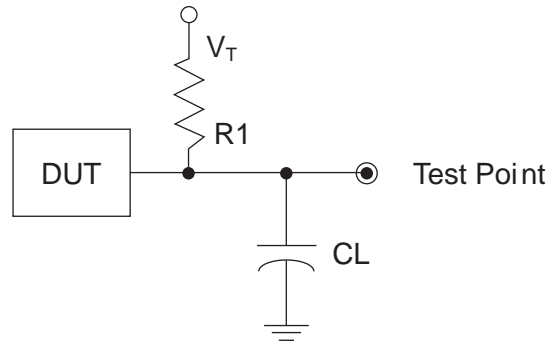
2. Extended range f<sub>MAX</sub> Write operation support up to 53MHz with 1.2V V<sub>CC</sub> and at 25C.



## Switching Test Conditions

Figure 3-1 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-1.

**Figure 3-1. Output Test Load, LVCMOS Standards**



**Table 3-1. Test Fixture Required Components, Non-Terminated Interfaces**

Test Condition	R <sub>1</sub>	C <sub>L</sub>	Timing Reference	V <sub>T</sub>
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = V <sub>CCIO</sub> /2	—
			LVCMOS 1.8 = V <sub>CCIO</sub> /2	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V <sub>OL</sub>
LVCMOS 3.3 (Z -> L)			1.5	V <sub>OH</sub>
Other LVCMOS (Z -> H)			V <sub>CCIO</sub> /2	V <sub>OL</sub>
Other LVCMOS (Z -> L)			V <sub>CCIO</sub> /2	V <sub>OH</sub>
LVCMOS (H -> Z)			V <sub>OH</sub> - 0.15	V <sub>OL</sub>
LVCMOS (L -> Z)			V <sub>OL</sub> - 0.15	V <sub>OH</sub>

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Name	Function	I/O	Description
SPI1_CSN/PIO[T/B]_x[HD]	User SPI1	I/O	In user mode, used as CSN signal on SPI interface for sensor management function. This pin is output pin in Master Mode, and input in in Slave Mode.
	Configuration	I/O	This pins is shared with device configuration. During configura-tion, this pin is CSN signal connecting to external SPI memory
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x repre-sents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_SCK/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as CLK signal on SPI interface for sensor management function.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x repre-sents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_MISO/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as Input (Master Mode) or Output (Slave Mode) signal on SPI interface for sensor management func-tion.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x repre-sents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_MOSI/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as Output (Master Mode) or Input (Slave Mode) signal on SPI interface for sensor management func-tion.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x repre-sents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_CSN/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as CSN signal on SPI interface for sensor management function. This pin is output pin in Master Mode, and input in in Slave Mode.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x repre-sents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
<b>I<sup>2</sup>C Ports</b>			
I2C1_SCL/PIO[T/B]_x[HD]	User I2C1	I/O	Used as CLK signal on I <sup>2</sup> C interface for sensor management function.
	General I/O	I/O	When the I <sup>2</sup> C interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
I2C1_SDA/PIO[T/B]_x[HD]	User I2C1	I/O	Used as Data signal on I <sup>2</sup> C interface for sensor management function.
	General I/O	I/O	When the I <sup>2</sup> C interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O

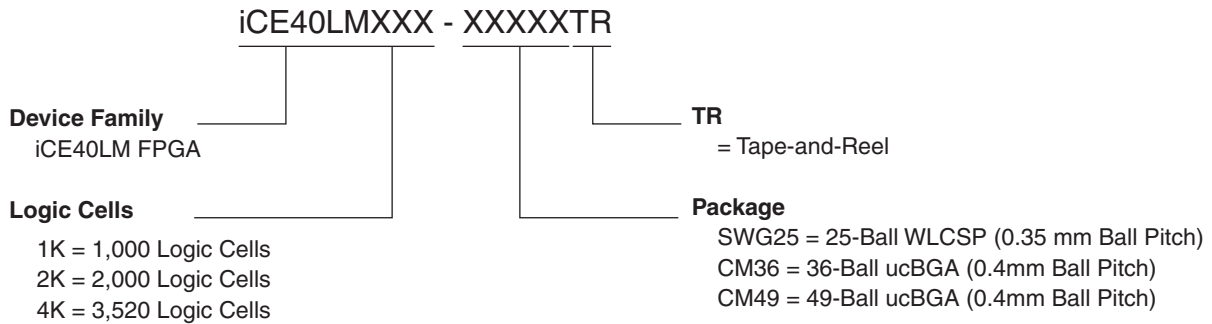
Signal Name	Function	I/O	Description
I2C2_SCL/PIO[T/B]_x[HD]	User I2C2	I/O	Used as CLK signal on I <sup>2</sup> C interface for sensor management function.
	General I/O	I/O	When the I <sup>2</sup> C interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
I2C2_SDA/PIO[T/B]_x[HD]	User I2C2	I/O	Used as Data signal on I <sup>2</sup> C interface for sensor management function.
	General I/O	I/O	When the I <sup>2</sup> C interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
<b>Global Signals</b>			
PIO[T/B]_x[HD]/Gn	General I/O	I/O	User can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
	Global Signal	I	Global input used for high fanout, or clock/reset net. n=0,1,2,3,6,7. The Gn Global input pin can drive the corresponding GBUF <sub>n</sub> global buffer.
<b>General Purpose I/O</b>			
PIO[T/B]_x[HD]	General I/O	I/O	User can program this pin as general I/O pin for user functions. (x represents ball on the package)

### Pin Information Summary

Pin Type		iCE40LM-1K			iCE40LM-2K			iCE40LM-4K		
		SWG25	CM36	CM49	SWG25	CM36	CM49	SWG25	CM36	CM49
General Purpose I/O Per Bank	Bank 0	7	15	20	7	15	20	7	15	20
	Bank 2 <sup>1</sup>	11	13	17	11	13	17	11	13	17
Total General Purpose I/Os		18	28	37	18	28	37	18	28	37
Vcc		1	1	2	1	1	2	1	1	2
Vccio	Bank 0	1	1	1	1	1	1	1	1	1
	Bank 2	1	1	1	1	1	1	1	1	1
V <sub>CC_SPI</sub>		0	0	1	0	0	1	0	0	1
V <sub>CCPLL</sub>		0	1	1	0	1	1	0	1	1
Miscellaneous Dedicated Pins		2	2	2	2	2	2	2	2	2
GND		2	2	4	2	2	4	2	2	4
NC		0	0	0	0	0	0	0	0	0
Reserved		0	0	0	0	0	0	0	0	0
Total Balls		25	36	49	25	36	49	25	36	49
SPI Interfaces	Bank 0	0	0	0	0	0	0	0	0	0
	Bank 2	1	1	1	2	2	2	2	2	2
I <sup>2</sup> C Interfaces	Bank 0	1	1	1	2	2	2	2	2	2
	Bank 2	0	0	0	0	0	0	0	0	0

1. Including General Purpose I/Os powered by V<sub>CC\_SPI</sub> and V<sub>CCPLL</sub>.

## iCE40LM Part Number Description



All parts are shipped in tape-and-reel.

## Ordering Part Numbers

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
iCE40LM1K-SWG25TR	1000	1.2V	Halogen-Free caBGA	25	IND
iCE40LM1K-CM36TR	1000	1.2V	Halogen-Free csBGA	36	IND
iCE40LM1K-CM49TR	1000	1.2V	Halogen-Free csBGA	49	IND
iCE40LM2K-SWG25TR	2000	1.2V	Halogen-Free caBGA	25	IND
iCE40LM2K-CM36TR	2000	1.2V	Halogen-Free csBGA	36	IND
iCE40LM2K-CM49TR	2000	1.2V	Halogen-Free csBGA	49	IND
iCE40LM4K-SWG25TR	3520	1.2V	Halogen-Free caBGA	25	IND
iCE40LM4K-CM36TR	3520	1.2V	Halogen-Free csBGA	36	IND
iCE40LM4K-CM49TR	3520	1.2V	Halogen-Free csBGA	49	IND



# iCE40LM Family Data Sheet Revision History

October 2013

Advance Data Sheet DS1045

Date	Version	Section	Change Summary
August 2013	00.1 EAP	All	Initial release.
September 2013	00.2 EAP	All	General updates to all sections.
October 2013	01.0	All	General updates for product launch.
		Pinout Information	Updated ball map to 25-pin WLCSP.