Lattice Semiconductor Corporation - ICE40LM4K-CM36 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

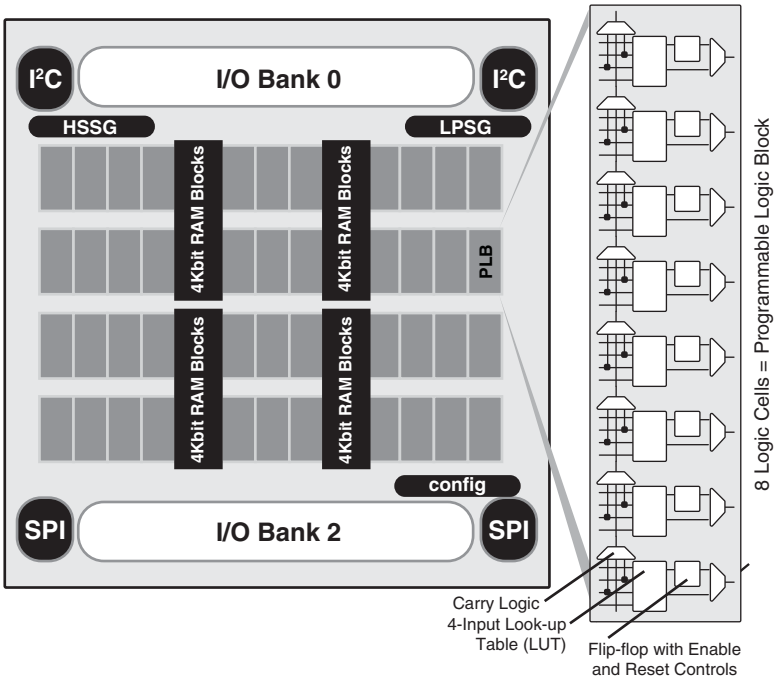
Details	
Product Status	Obsolete
Number of LABs/CLBs	440
Number of Logic Elements/Cells	3520
Total RAM Bits	81920
Number of I/O	28
Number of Gates	-
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	36-VFBGA
Supplier Device Package	36-UCBGA (2.5x2.5)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/ice40lm4k-cm36

iCE40LM Family Data Sheet Architecture

Architecture Overview

The iCE40LM family architecture contains an array of Programmable Logic Blocks (PLB), two Strobe Generators, two user configurable I²C controllers, two user configurable SPI controllers, and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1shows the block diagram of the iCE40LM-4K device.

Figure 2-1. iCE40LM-4K Device, Top View



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

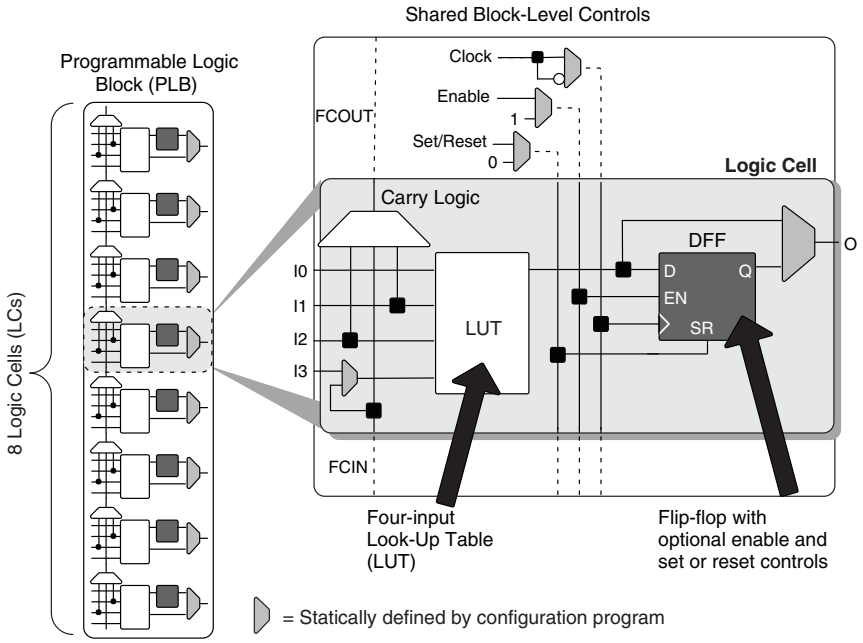
In the iCE40LM family, There are two sysIO banks, one on top and one on bottom. User can connect both V_{CCIO}s together, if all the I/Os are using the same voltage standard. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 Kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

Every device in the family has two user SPI ports, one of these (right side) SPI port also supports programming and configuration of the device. The iCE40LM also includes two user I²C ports, and two Strobe Generators.

PLB Blocks

The core of the iCE40LM device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

Figure 2-2. PLB Block Diagram



Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 2-1. Logic Cell Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

sysCLOCK Phase Locked Loops (PLLs) - *NOT SUPPORTED on the 25-Pin WLCSP*

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40LM devices have one sysCLOCK PLL (Please note that the 25-pin WLCSP package does not support the PLL). REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal strobe generator or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

The iCE40LM PLL functions the same as the PLLs in the iCE40 family. For more details on the PLL, see TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

Figure 2-3. PLL Diagram

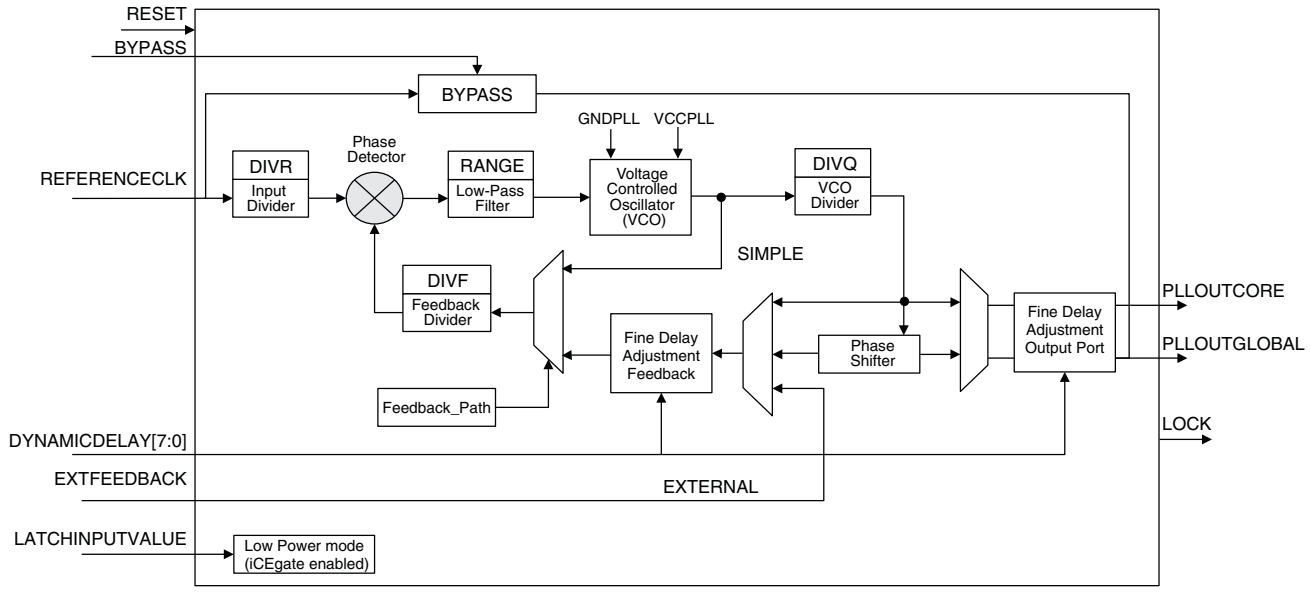


Table 2-3 provides signal descriptions of the PLL block.

Table 2-3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLL-OUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

sysMEM Embedded Block RAM Memory

Larger iCE40LM device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 Kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

Table 2-4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40LM EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

Figure 2-4. sysMEM Memory Primitives

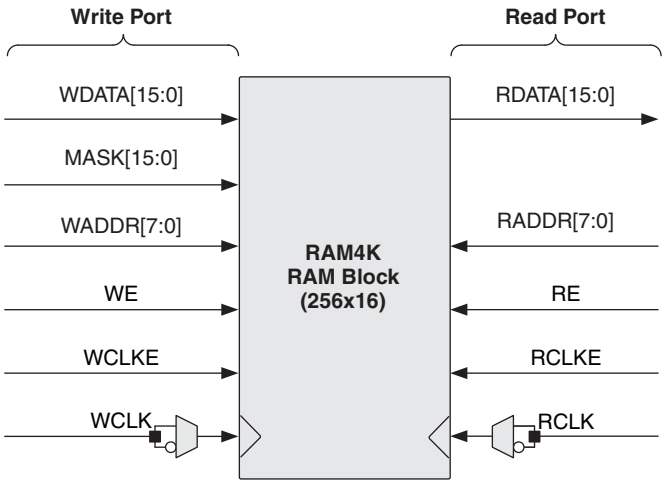


Table 2-5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

The iCE40LM EBR block functions the same as EBR blocks in the iCE40 family. For further information on the sysMEM EBR block, please refer to TN1250, Memory Usage Guide for iCE40 Devices.

Figure 2-6. iCE I/O Register Block Diagram

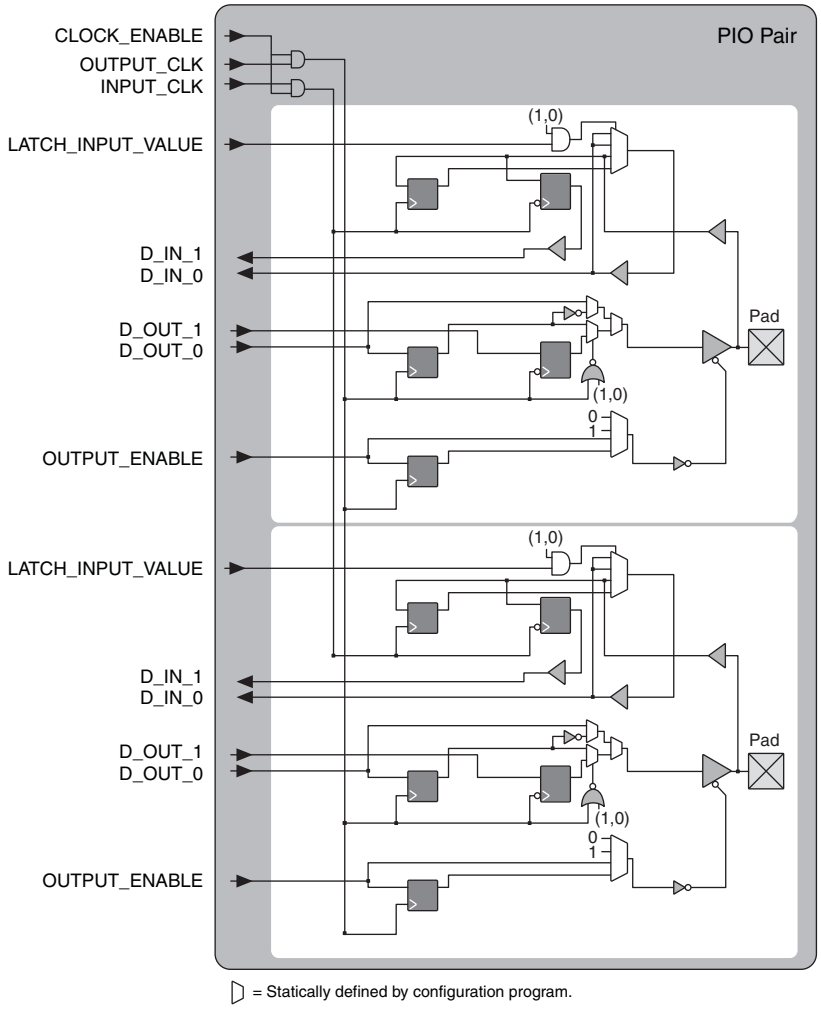


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO_2} and V_{CC_SPI} (V_{CC_SPI} is connected to V_{CCIO_2} on the 25-pin WLCSP) reach the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins maintain the pre-configuration state until V_{CC} and V_{CCIO_2} reach the defined levels. The I/Os take on the software user-configured settings only after V_{CC_SPI} reaches the level and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40LM sysIO buffer supports all single-ended input and output standards. The buffer supports the LVCMOS 1.8, 2.5, and 3.3V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40LM devices.

Table 2-7. Supported Input Standards

Input Standard	V_{CCIO} (Typical)		
	3.3V	2.5V	1.8V
Single-Ended Interfaces			
LVCMOS33	✓		
LVCMOS25		✓	
LVCMOS18			✓

Table 2-8. Supported Output Standards

Output Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8

On-Chip Strobe Generators

The iCE40LM devices feature two different Strobe Generators. One is tailored for low-power operation (Low Power Strobe Generator – LPSG), and generates periodic strobes in the Microsecond (µs) ranges. The other is tailored for high speed operation (High Speed Strobe Generator – HSSG), and generates periodic strobes in the Nanosecond (ns) ranges.Add a paragraph:

The Strobe Generators (HSSG and LPSG) provide fixed periodic strobes, and these strobes can be used as a clock source. When used as a clock source, the HSSG can provide strobe frequency in the range of 5MHz - 20MHz. The LPSG can provide strobe frequency in the range of 4KHz - 20KHz.

For further information on how to use the LPSG and HSSG, please refer to TN1275, iCE40LM On-Chip Strobe Generator Usage Guide.

User I²C IP

The iCE40LM devices have two I²C IP cores. Either of the two cores can be configured either as an I²C master or as an I²C slave. Both I²C cores have preassigned pins, or user can select different pins, when the core is used.

When the IP core is configured as master, it will be able to control other devices on the I²C bus through the pre-assigned pin interface. When the core is configured as the slave, the device will be able to provide I/O expansion to an I²C Master. The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 400 KHz data transfer speed
- General Call support

For further information on the User I²C, please refer to TN1274, iCE40LM SPI/I2C Hardened IP Usage Guide.

User SPI IP

The iCE40LM devices have two SPI IP cores. Both SPI cores have preassigned pins, or user can select different pins, when the SPI core is used. Both SPI IP core can be configured as a SPI master or as a slave. When the SPI IP core is configured as a master, it controls the other SPI enabled devices connected to the SPI Bus. When SPI IP core is configured as a slave, the device will be able to interface to an external SPI master.

The SPI IP core supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer

For further information on the User SPI, please refer to TN1274, iCE40LM SPI/I2C Hardened IP Usage Guide.

High Drive I/O Pins

The iCE40LM family devices offer 3 High Drive (HD) outputs in each device in the family. The HD outputs are ideal to drive LED signals on mobile application.

These HD outputs can be driven in different drive modes. The default is standard drive, which source/sink 8mA current nominally. When HD drive option is selected, these HD outputs can source/sink 24mA current nominally.

The pins on the HD I/Os are labeled with HD in it.

Power On Reset

iCE40LM devices have power-on reset circuitry to monitor V_{CC}, V_{CCIO_2} and V_{CC_SPI} voltage levels during power-up and operation. At power-up, the POR circuitry monitors these voltage levels. It then triggers download from the external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

iCE40LM Configuration

This section describes the programming and configuration of the iCE40LM family.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

- From a SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

For more details on configuring the iCE40LM, please see TN1248, iCE40 Programming and Configuration.

Power Saving Options

The iCE40LM devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. Table 2-9 describes the function of these features.

Table 2-9. iCE40LM Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

iCE40LM Family Data Sheet
DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . -0.5 to 1.42V

Output Supply Voltage V_{CCIO} and V_{CC_SPI} . . . . . -0.5 to 3.60V

PLL Power Supply, V_{CCPLL} . . . . . -0.5 to 1.3V

I/O Tri-state Voltage Applied. . . . . -0.5 to 3.60V

Dedicated Input Voltage Applied . . . . . -0.5 to 3.60V

Storage Temperature (Ambient). . . . . -65°C to 150°C

Junction Temperature (T_J) . . . . . -55°C to 125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.

Recommended Operating Conditions[1]

Symbol	Parameter		Min.	Max.	Units
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	V_{CCIO_0}, V_{CCIO_2}	1.71	3.46	V
V_{CCPLL}[4]	PLL Power Supply Voltage		1.14	1.26	V
V_{CC_SPI}[5]	Config SPI port Power Supply Voltage		1.71	3.46	V
t_{JIND}	Junction Temperature Industrial Operation		-40	100	°C

1. Like power supplies must be tied together. V_{CC} to V_{CCPLL}, V_{CCIO_0} to V_{CCIO_2} if they are at same supply voltage.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.
4. For 25-pin WLCSP, PLL is not supported.
5. For 25-pin WLCSP, V_{CC_SPI} is connected to V_{CCIO_2} on the package. For all other packages, V_{CC_SPI} is used to power the SPI1 ports in both configuration mode and user mode.

Power Supply Ramp Rates[1]

Symbol	Parameter	Min.	Max.	Units
t_{RAMP}	Power supply ramp rates for all power supplies.	0.6	10	V/ms

1. Assumes monotonic ramp rates.

Power-On-Reset Voltage Levels[1]

Symbol	Parameter		Min.	Max.	Units
V_{PORUP}	Power-On-Reset ramp-up trip point (circuit monitoring V_{CC}, V_{CCIO_2} and V_{CC_SPI})	V_{CC}	0.64	0.99	V
		V_{CCIO_2}, V_{CC_SPI}	0.70	1.59	V
V_{PORDN}	Power-On-Reset ramp-down trip point (circuit monitoring V_{CC}, V_{CCIO_2} and V_{CC_SPI})	V_{CC}	—	0.66	V
		V_{CCIO_2}, V_{CC_SPIl}	—	1.59	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

Power Up Sequence

For all iCE40LM devices, it is required to have the V_{CC}/V_{CCPLL} power supply powered up before all other power supplies. The V_{CC}/V_{CCPLL} has to be higher than 0.5V before other supplies are powered from GND.

Following V_{CC}/V_{CCPLL}, V_{CCSPI} should be ramped up, followed by the remaining supplies. For 25-pin WLCSP, V_{CC_SPI} is connected to V_{CCIO_2}, and the V_{CCPLL} is internally connected for that package.

ESD Performance

Please contact Lattice Semiconductor for additional information.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1, 3, 4]	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2V$	—	—	+/-10	µA
C_1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pf
C_2	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V V_{CC} = Typ., V_{IO} = 0 to V_{CCIO} + 0.2V	—	6	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8V, 2.5V, 3.3V	—	200	—	mV
I_{PU}	Internal PIO Pull-up Current	V_{CCIO} = 1.8V, 0=<V_{IN}<=0.65 V_{CCIO}	-3	—	-31	µA
		V_{CCIO} = 2.5V, 0=<V_{IN}<=0.65 V_{CCIO}	-8	—	-72	µA
		V_{CCIO} = 3.3V, 0=<V_{IN}<=0.65 V_{CCIO}	-11	—	-128	µA

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25°C, f = 1.0 MHz.
3. Please refer to V_{IL} and V_{IH} in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.

Supply Current [1, 2, 3, 4]

Symbol	Parameter	Typ. VCC[4]	Units
$I_{CCSTDBY}$	Core Power Supply Static Current	100	µA
$I_{CCPLLSTDBY}$	PLL Power Supply Static Current		µA
$I_{CCIOSTDBY}$, $I_{CC\_SPISTDBY}$	V_{CCIO}, V_{CC_SPI} Power Supply Static Current		µA
I_{CCPEAK}	Core Power Supply Startup Peak Current		µA
$I_{CCPLLPEAK}$	PLL Power Supply Startup Peak Current		µA
$I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$	V_{CCIO}, V_{CC_SPI} Power Supply Startup Peak Current		µA

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. TJ = 25°C, power supplies at nominal voltage.
4. Does not include pull-up.
5. For 25-pin WLCSP, V_{CCPLL} is tied internally on the package, and V_{CC_SPI} is also connected to V_{CCIO_2} on the package.

User I²C Specifications

Parameter Symbol	Parameter Description	spec (STD Mode)			spec (FAST Mode)			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Maximum SCL clock frequency	—	—	100	—	—	400	KHz
t_{HI}	SCL clock HIGH Time	4	—	—	0.6	—	—	us
t_{LO}	SCL clock LOW Time	4.7	—	—	1.3	—	—	us
$t_{SU,DAT}$	Setup time (DATA)	250	—	—	100	—	—	ns
$t_{HD,DAT}$	Hold time (DATA)	0	—	—	0	—	—	ns
$t_{SU,STA}$	Setup time (START condition)	4.7	—	—	0.6	—	—	us
$t_{HD,STA}$	Hold time (START condition)	4	—	—	0.6	—	—	us
$t_{SU,STO}$	Setup time (STOP condition)	4	—	—	0.6	—	—	us
t_{BUF}	Bus free time between STOP and START	4.7	—	—	1.3	—	—	us
$t_{CO,DAT}$	SCL LOW to DATAOUT valid	—	—	3.4	—	—	0.9	us

User SPI Specifications

Parameter Symbol	Parameter Description	Min	Typ	Max	Units
f_{MAX}	Maximum SCK clock frequency	—	—	45	MHz
t_{HI}	HIGH period of SCK clock	9	—	—	ns
t_{LO}	LOW period of SCK clock	9	—	—	ns
$t_{SUmaster}$	Setup time (master mode)	2	—	—	ns
$t_{HOLDmaster}$	Hold time (master mode)	5	—	—	ns
$t_{SUslave}$	Setup time (slave mode)	2	—	—	ns
$t_{HOLDslave}$	Hold time (slave mode)	5	—	—	ns
$t_{SCK2OUT}$	SCK to out (slave mode)	—	—	13.5	ns

sysIO Recommended Operating Conditions

Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89

sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.5	8	-8
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.5	6	-6
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2V	0.4	V_{CCIO} - 0.4	4	-4
					0.2	V_{CCIO} - 0.2	0.1	-0.1

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.

Typical Building Block Function Performance[1, 2]

Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
Basic Functions		
16-bit decoder	16.5	ns
4:1 MUX	18.0	ns
16:1 MUX	19.5	ns

Register-to-Register Performance

Function	Timing	Units
Basic Functions		
16:1 MUX	110	MHz
16-bit adder	100	MHz
16-bit counter	100	MHz
64-bit counter	40	MHz
Embedded Memory Functions		
256x16 Pseudo-Dual Port RAM	150	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a V_{CC} of 1.14V at Junction Temp 85C.

Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

Maximum sysIO Buffer Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVCMOS33		MHz
LVCMOS25		MHz
LVCMOS18		MHz
Outputs		
LVCMOS33		MHz
LVCMOS25		MHz
LVCMOS18		MHz

1. Measured with a toggling pattern

iCE40LM Family Timing Adders

Over Recommended Commercial Operating Conditions[1, 2, 3]

Buffer Type	Description	Timing	Units
Input Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3V	0.18	nS
LVCMOS25	LVCMOS, V_{CCIO} = 2.5V	0.00	nS
LVCMOS18	LVCMOS, V_{CCIO} = 1.8V	0.19	nS
Output Adjusters			
LVCMOS33	LVCMOS, V_{CCIO} = 3.3V	-0.12	nS
LVCMOS25	LVCMOS, V_{CCIO} = 2.5V	0.00	nS
LVCMOS18	LVCMOS, V_{CCIO} = 1.8V	1.32	nS

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Condition table.
3. Commercial timing numbers are shown.

iCE40LM External Switching Characteristics

Over Recommended Commercial Operating Conditions

Parameter	Description	Device			Units
Clocks					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All devices		185	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All devices	TBD	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	All devices	—	650	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT logic	All devices	—	14.0	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)					
t_{SKEW_IO}	Data bus skew across a bank of IOs	All devices	—	400	ps
t_{CO}	Clock to Output - PIO Output Register	All devices	—	9.0	ns
t_{SU}	Clock to Data Setup - PIO Input Register	All devices		—	ns
t_{H}	Clock to Data Hold - PIO Input Register	All devices	5.55	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[1]					
t_{CO}	Clock to Output - PIO Output Register	All devices	—	TBD	ns
t_{SU}	Clock to Data Setup - PIO Output Register	All devices	TBD	—	ns
t_{H}	Clock to Data Hold - PIO Output Register	All devices	TBD	—	ns

1. 25-pin WLCSP package does not support PLL.

Switching Test Conditions

Figure 3-1 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-1.

Figure 3-1. Output Test Load, LVCMOS Standards

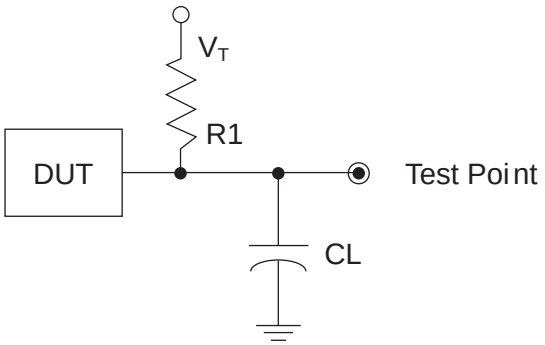


Table 3-1. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVCMOS 3.3 = 1.5V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z -> L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H -> Z)			V_{OH} - 0.15	V_{OL}
LVCMOS (L -> Z)			V_{OL} - 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

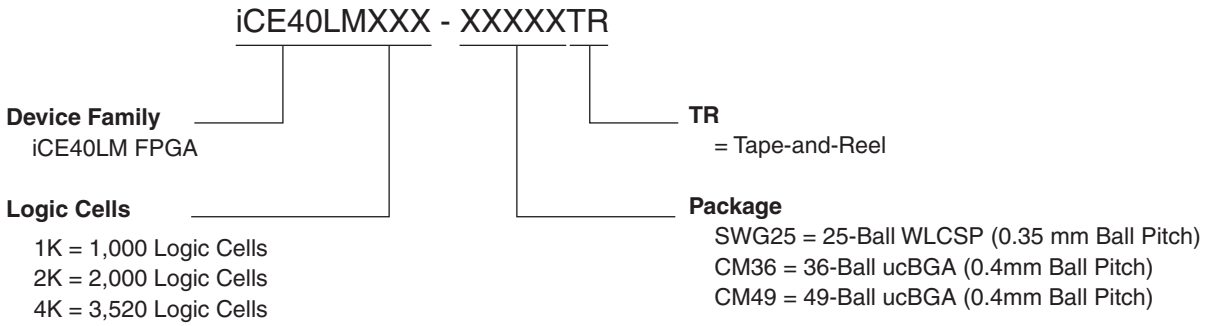
Signal Name	Function	I/O	Description
Power Supplies			
V_{CC}	Power	-	Core Power Supply
V_{CCIO_0}	Power	-	Power Supply for I/Os in Bank 0
V_{CCIO_2}	Power	-	Power Supply for I/Os in Bank 2
V_{CC_SPI}	Power	-	Power supply for SPI1 ports. For 25-pin WLCSP, this signal is connected to V_{CCIO_2}
V_{CCPLL}	Power	-	Power supply for PLL. For 25-pin WLCSP, this is connected internally to V_{CC}
GND/GNDPLL	GROUND	-	Ground
Dedicated Configuration Signals			
CRESET	Configuration	I	Configuration Reset, active LOW. No internal pull-up resistor. Either actively driven externally or connect an 10K-ohm pull-up resistor to V_{CCIO_2}.
CDONE	Configuration	I/O	Configuration Done. Includes a weak pull-up resistor to V_{CCIO_2}.
SPI and Config SPI Ports			
SPI1_SCK/PIO[T/B]_x[HD]	User SPI1	I/O	In user mode, used as CLK signal on SPI interface for sensor management function.
	Configuration	I/O	This pins is shared with device configuration. During configuration, this pin is CLK signal connecting to external SPI memory
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI1_MISO/PIO[T/B]_x[HD]	User SPI1	I/O	In user mode, used as Input (Master Mode) or Output (Slave Mode) signal on SPI interface for sensor management function.
	Configuration	I/O	This pins is shared with device configuration. During configuration, this pin is Input signal connecting to external SPI memory.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI1_MOSI/PIO[T/B]_x[HD]	User SPI1	I/O	In user mode, used as Output (Master Mode) or Input (Slave Mode) signal on SPI interface for sensor management function.
	Configuration	I/O	This pins is shared with device configuration. During configuration, this pin is Output signal connecting to external SPI memory.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O

Signal Name	Function	I/O	Description
SPI1_CSN/PIO[T/B]_x[HD]	User SPI1	I/O	In user mode, used as CSN signal on SPI interface for sensor management function. This pin is output pin in Master Mode, and input in in Slave Mode.
	Configuration	I/O	This pins is shared with device configuration. During configuration, this pin is CSN signal connecting to external SPI memory
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_SCK/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as CLK signal on SPI interface for sensor management function.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_MISO/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as Input (Master Mode) or Output (Slave Mode) signal on SPI interface for sensor management function.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_MOSI/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as Output (Master Mode) or Input (Slave Mode) signal on SPI interface for sensor management function.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
SPI2_CSN/PIO[T/B]_x[HD]	User SPI2	I/O	In user mode, used as CSN signal on SPI interface for sensor management function. This pin is output pin in Master Mode, and input in in Slave Mode.
	General I/O	I/O	In user mode, when the SPI interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
I^2C Ports			
I2C1_SCL/PIO[T/B]_x[HD]	User I2C1	I/O	Used as CLK signal on I^2C interface for sensor management function.
	General I/O	I/O	When the I^2C interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O
I2C1_SDA/PIO[T/B]_x[HD]	User I2C1	I/O	Used as Data signal on I^2C interface for sensor management function.
	General I/O	I/O	When the I^2C interface is not used, user can program this pin as general I/O pin for user functions. (x represents ball on the package) [T/B]: T=Vccio_0 bank, B=Vccio_2 bank. [HD]=High Drive I/O

iCE40LM Family Data Sheet Ordering Information

September 2013 Advance Data Sheet DS1045

iCE40LM Part Number Description



All parts are shipped in tape-and-reel.

Ordering Part Numbers

Part Number	LUTs	Supply Voltage	Package	Leads	Temp.
iCE40LM1K-SWG25TR	1000	1.2V	Halogen-Free caBGA	25	IND
iCE40LM1K-CM36TR	1000	1.2V	Halogen-Free csBGA	36	IND
iCE40LM1K-CM49TR	1000	1.2V	Halogen-Free csBGA	49	IND
iCE40LM2K-SWG25TR	2000	1.2V	Halogen-Free caBGA	25	IND
iCE40LM2K-CM36TR	2000	1.2V	Halogen-Free csBGA	36	IND
iCE40LM2K-CM49TR	2000	1.2V	Halogen-Free csBGA	49	IND
iCE40LM4K-SWG25TR	3520	1.2V	Halogen-Free caBGA	25	IND
iCE40LM4K-CM36TR	3520	1.2V	Halogen-Free csBGA	36	IND
iCE40LM4K-CM49TR	3520	1.2V	Halogen-Free csBGA	49	IND

iCE40LM Family Data Sheet Supplemental Information

For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, iCE40 Programming and Configuration
- TN1274, iCE40LM SPI/I2C Hardened IP Usage Guide
- TN1275, iCE40LM On-Chip Strobe Generator Usage Guide
- TN1276, iCE40LM Advanced SPI/I2C Hardened IP Usage Guide
- TN1250, Memory Usage Guide for iCE40 Devices
- TN1251, iCE40 sysCLOCK PLL Design and Usage Guide
- iCE40LM Pinout Files
- iCE40LM Pin Migration Files
- Thermal Management document
- Lattice design tools
- Schematic Symbols