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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	10
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705kj1cdw

Chapter 4
Central Processor Unit (CPU)

Chapter 5
External Interrupt Module (IRQ)

Chapter 9
Multifunction Timer Module

Chapter 10
Electrical Specifications

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Ordering Information and Mechanical Specifications

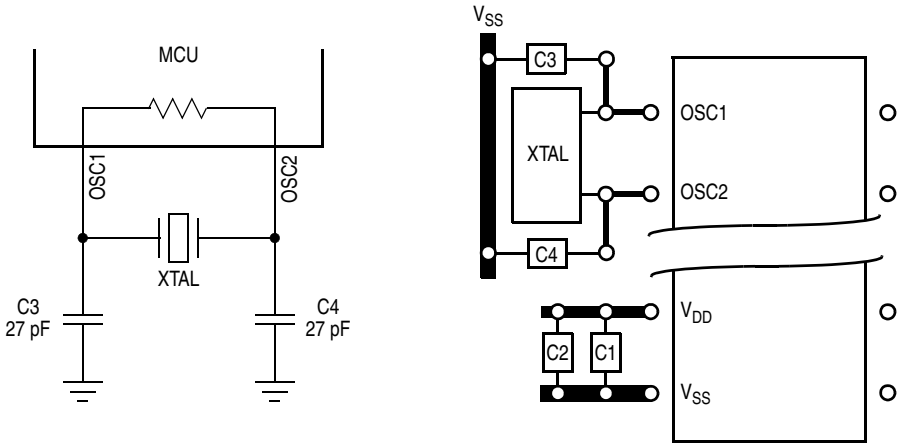


Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option

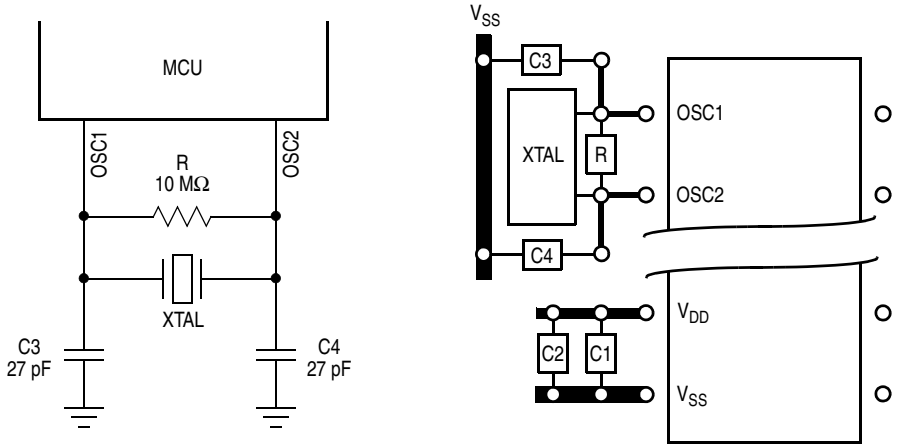


Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option

1.4.2.2 Ceramic Resonator Oscillator

To reduce cost, use a ceramic resonator instead of the crystal. The circuits shown in Figure 1-6 and Figure 1-7 show ceramic resonator circuits. Follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 as a programmable mask option.

Table 4-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2

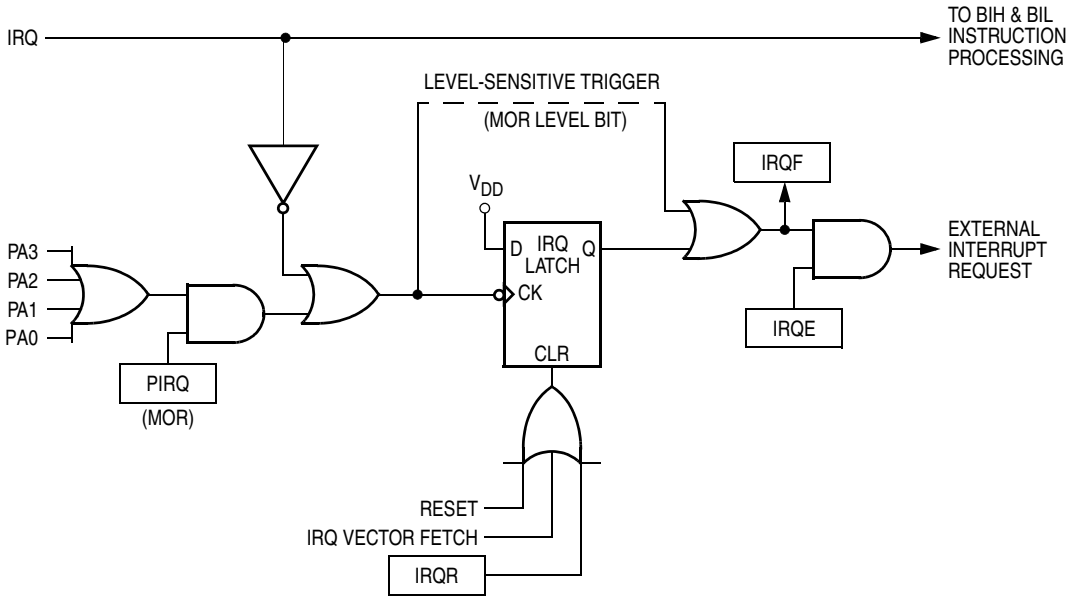


Figure 5-1. IRQ Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	IRQ Status and Control Register (ISCR) See page 54.	Read:	IRQE	0	0	0	IRQF	0	0	0
		Write:				R			IRQR	
		Reset:	1	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 5-2. IRQ Module I/O Register Summary

If edge-sensitive-only triggering is selected, a falling edge on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level on the $\overline{IRQ}/V_{PP}$ pin returns to logic 1 and then falls again to logic 0.

The $\overline{IRQ}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin can affect the mode of operation and should not exceed V_{DD}.

5.3.2 Optional External Interrupts

The inputs for the lower four bits of port A (PA0–PA3) can be connected to the $\overline{IRQ}$ pin input of the CPU if enabled by the PIRQ bit in the mask option register. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{IRQ}/V_{PP}$ pin except for the inverted phase (logic 1, rising edge). The active state of the $\overline{IRQ}/V_{PP}$ pin is a logic 0 (falling edge).

The PA0–PA3 pins are selected as a group to function as IRQ interrupts and are enabled by the IRQE bit in the IRQ status and control register. The PA0–PA3 pins can be positive-edge triggered only or positive-edge and high-level triggered.

If edge- and level-sensitive triggering is selected, a rising edge or a high level on a PA0–PA3 pin latches an external interrupt request. Edge- and level-sensitive triggering allows the use of multiple wired-OR external interrupt sources. As long as any source is holding a PA0–PA3 pin high, an external interrupt request is latched, and the CPU continues to execute the interrupt service routine.

If edge-sensitive only triggering is selected, a rising edge on a PA0–PA3 pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level of the previous interrupt signal returns to logic 0 and then rises again to logic 1.

NOTE

The BIH and BIL instructions apply only to the level on the $\overline{IRQ}/V_{PP}$ pin itself and not to the output of the logic OR function with the PA0–PA3 pins. The state of the individual port A pins can be checked by reading the appropriate port A pins as inputs.

Enabled PA0–PA3 pins cause an IRQ interrupt regardless of whether these pins are configured as inputs or outputs.

The $\overline{IRQ}$ pin has an internal Schmitt trigger. The optional external interrupts (PA0–PA3) do not have internal Schmitt triggers.

The interrupt mask bit (I) in the condition code register (CCR) disables all maskable interrupt requests, including external interrupt requests.

5.4 IRQ Status and Control Register

The IRQ status and control register (ISCR) controls and monitors operation of the IRQ module. All unused bits in the ISCR read as logic 0s. The IRQF bit is cleared and the IRQE bit is set by reset.

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQE	0	0	0	IRQF	0	0	0
Write:				R			IRQR	
Reset:	1	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 5-4. IRQ Status and Control Register (ISCR)

IRQR — Interrupt Request Reset Bit

This write-only bit clears the external interrupt request flag.

1 = Clears external interrupt and IRQF bit
0 = No effect on external interrupt and IRQF bit

IRQF — External Interrupt Request Flag

The external interrupt request flag is a clearable, read-only bit that is set when an external interrupt request is pending. Reset clears the IRQF bit.

1 = External interrupt request pending
0 = No external interrupt request pending

IRQE — External Interrupt Request Enable Bit

This read/write bit enables external interrupts. Reset sets the IRQE bit.

1 = External interrupt requests enabled
0 = External interrupt requests disabled

6.3 Effects of Stop and Wait Modes

The STOP and WAIT instructions have the following effects on MCU modules.

6.3.1 Clock Generation

Effects of STOP and WAIT on clock generation are discussed here.

6.3.1.1 STOP

The STOP instruction disables the internal oscillator, stopping the CPU clock and all peripheral clocks.

After exiting stop mode, the CPU clock and all enabled peripheral clocks begin running after the oscillator stabilization delay.

NOTE

The oscillator stabilization delay holds the MCU in reset for the first 4064 internal clock cycles.

6.3.1.2 WAIT

The WAIT instruction disables the CPU clock.

After exiting wait mode, the CPU clock and all enabled peripheral clocks immediately begin running.

6.3.2 CPU

Effects of STOP and WAIT on the CPU are discussed here.

6.3.2.1 STOP

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

After exit from stop mode by external interrupt, the I bit remains clear.

After exit from stop mode by reset, the I bit is set.

6.3.2.2 WAIT

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts
- Disables the CPU clock

After exit from wait mode by interrupt, the I bit remains clear.

After exit from wait mode by reset, the I bit is set.

6.3.3 COP Watchdog

Effects of STOP and WAIT on the COP watchdog are discussed here.

6.3.3.1 STOP

The STOP instruction:

- Clears the COP watchdog counter
- Disables the COP watchdog clock

NOTE

To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.

After exit from stop mode by external interrupt, the COP watchdog counter immediately begins counting from $0000 and continues counting throughout the oscillator stabilization delay.

NOTE

Immediately after exiting stop mode by external interrupt, service the COP to ensure a full COP timeout period.

After exit from stop mode by reset:

- The COP watchdog counter immediately begins counting from $0000.
- The COP watchdog counter is cleared at the end of the oscillator stabilization delay and begins counting from $0000 again.

6.3.3.2 WAIT

The WAIT instruction has no effect on the COP watchdog.

NOTE

To prevent a COP timeout during wait mode, exit wait mode periodically to service the COP.

6.3.4 Timer

Effects of STOP and WAIT on the timer are discussed here.

6.3.4.1 STOP

The STOP instruction:

- Clears the RTIE, TOFE, RTIF, and TOF bits in the timer status and control register, disabling timer interrupt requests and removing any pending timer interrupt requests
- Disables the clock to the timer

After exiting stop mode by external interrupt, the timer immediately resumes counting from the last value before the STOP instruction and continues counting throughout the oscillator stabilization delay.

After exiting stop mode by reset and after the oscillator stabilization delay, the timer resumes operation from its reset state.

6.3.4.2 WAIT

The WAIT instruction has no effect on the timer.

6.3.5 EPROM/OTPROM

Effects of STOP and WAIT on the EPROM/OTPROM are discussed here.

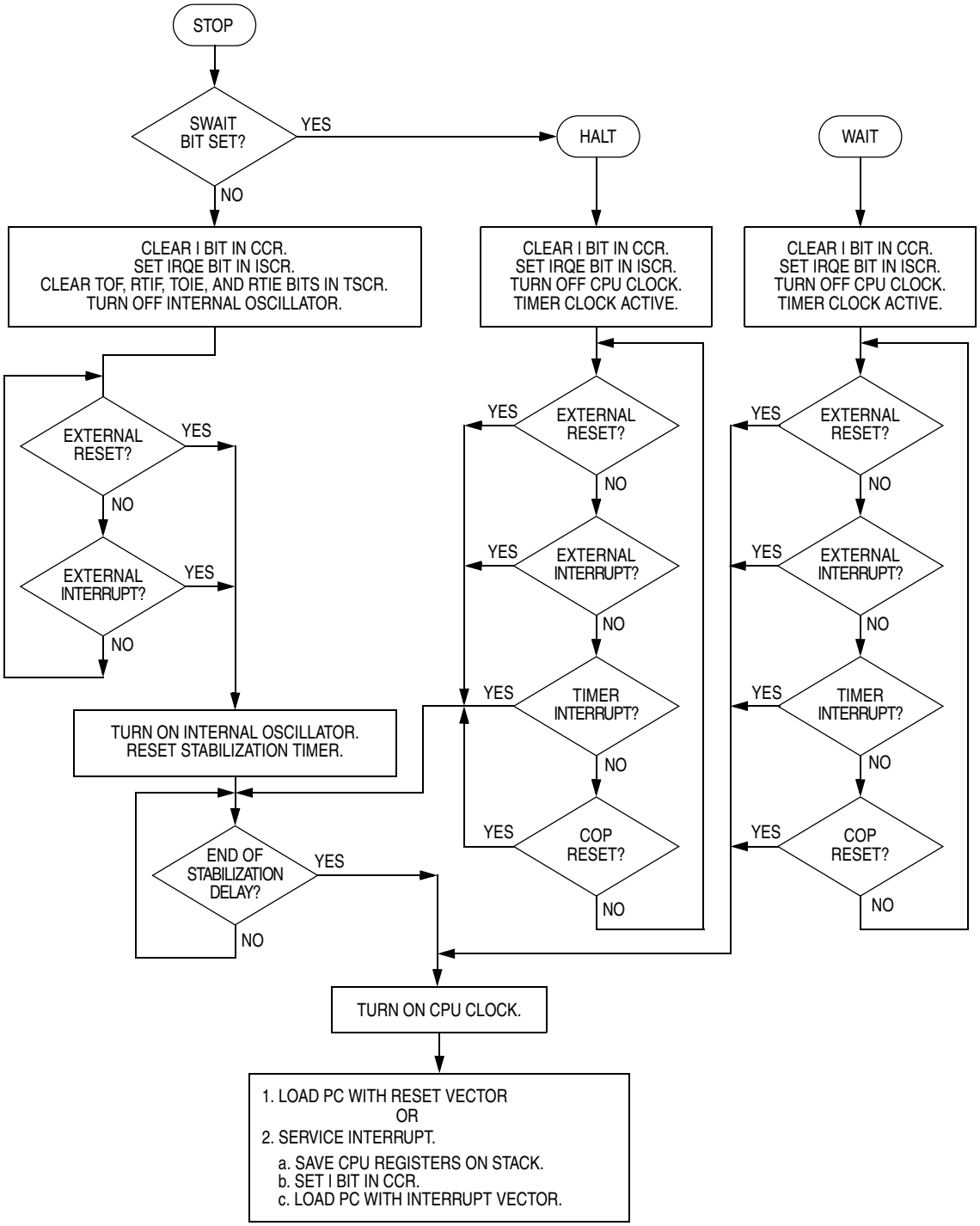


Figure 6-2. STOP/HALT/WAIT Flowchart

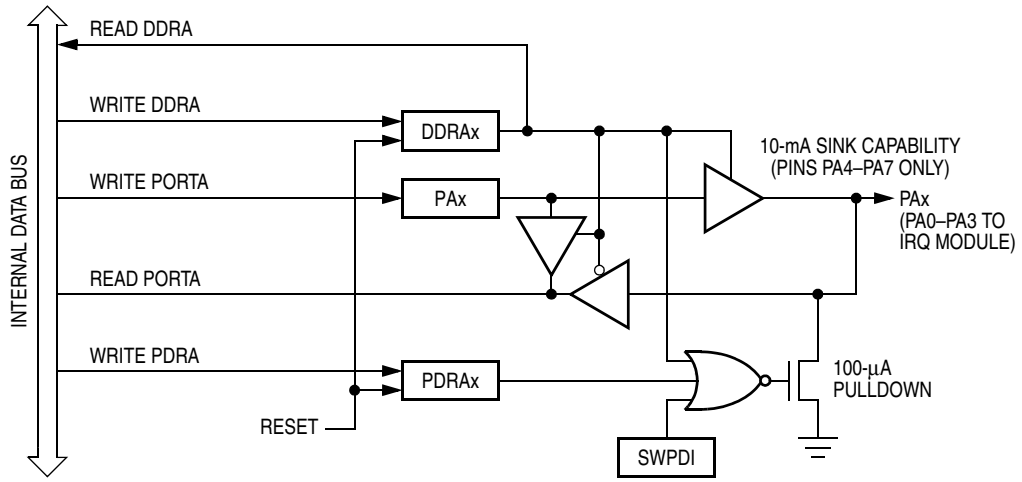


Figure 7-4. Port A I/O Circuitry

Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

When bit DDRAx is a logic 1, reading address $0000 reads the PAx data latch. When bit DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 7-1 summarizes the operation of the port A pins.

Table 7-1. Port A Pin Operation

Data Direction Bit	I/O Pin Mode	Accesses to Data Bit	
		Read	Write
0	Input, high-impedance	Pin	Latch(1)
1	Output	Latch	Latch

1. Writing affects the data register but does not affect input.

7.2.3 Pulldown Register A

Pulldown register A inhibits the pulldown devices on port A pins programmed as inputs.

NOTE

If the SWPDI bit in the mask option register is programmed to logic 1, reset initializes all port A pins as inputs with disabled pulldown devices.

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-5. Pulldown Register A (PDRA)

PDIA[7:0] — Pulldown Inhibit A Bits

PDIA[7:0] disable the port A pulldown devices. Reset clears PDIA[7:0].

1 = Corresponding port A pulldown device disabled

0 = Corresponding port A pulldown device not disabled

7.4 I/O Port Electrical Characteristics

Table 7-3. I/O Port DC Electrical Characteristics (V_{DD} = 5.0 V)(1)

Characteristic	Symbol	Min	Typ(2)	Max	Unit
Current Drain Per Pin	I	—	—	25	mA
Output High Voltage (I_{Load} = –2.5 mA) PA4–PA7 (I_{Load} = –5.5 mA) PB2–PB3, PA0–PA3	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output Low Voltage (I_{Load} = 10.0 mA) PA0–PA7, PB2–PB3	V_{OL}	—	—	0.8	V
Input High Voltage PA0–PA7, PB2–PB3	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage PA0–PA7, PB2–PB3	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
I/O Ports Hi-Z Leakage Current PA0–PA7, PB2–PB3 (Without Individual Pulldown Activated)	I_{IL}	—	0.2	±1	µA
Input Pulldown Current PA0–PA7, PB2–PB3 (With Individual Pulldown Activated)	I_{IL}	35	80	200	µA

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25°C.

Table 7-4. I/O Port DC Electrical Characteristics (V_{DD} = 3.3 V)(1)

Characteristic	Symbol	Min	Typ(2)	Max	Unit
Current Drain Per Pin	I	—	—	25	mA
Output High Voltage (I_{Load} = –0.8 mA) PA4–PA7 (I_{Load} = –1.5 mA) PA0–PA3, PB2–PB3	V_{OH}	V_{DD} –0.3 V_{DD} –0.3	— —	— —	V
Output Low Voltage (I_{Load} = 5.0 mA) PA4–PA7 (I_{Load} = 3.5 mA) PA0–PA3, PB2–PB3	V_{OL}	— —	— —	0.5 0.5	V
Input High Voltage PA0–PA7, PB2–PB3	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input Low Voltage PA0–PA7, PB2–PB3	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
I/O Ports Hi-Z Leakage Current PA0–PA7, PB2–PB3 (Without Individual Pulldown Activated)	I_{IL}	—	0.1	±1	µA
Input Pulldown Current PA0–PA7, PB2–PB3 (With Individual Pulldown Activated)	I_{IL}	12	30	100	µA

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS}= 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25°C.

9.5 I/O Registers

The following registers control and monitor the timer operation:

- Timer status and control register (TSCR)
- Timer counter register (TCR)

9.5.1 Timer Status and Control Register

The read/write timer status and control register performs the following functions:

- Flags timer interrupts
- Enables timer interrupts
- Resets timer interrupt flags
- Selects real-time interrupt rates

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
Write:					TOFR	RTIFR		
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 9-3. Timer Status and Control Register (TSCR)

TOF — Timer Overflow Flag

This read-only flag becomes set when the first eight stages of the counter roll over from $FF to $00. TOF generates a timer overflow interrupt request if TOIE is also set. Clear TOF by writing a logic 1 to the TOFR bit. Writing to TOF has no effect. Reset clears TOF.

RTIF — Real-Time Interrupt Flag

This read-only flag becomes set when the selected RTI output becomes active. RTIF generates a real-time interrupt request if RTIE is also set. Clear RTIF by writing a logic 1 to the RTIFR bit. Writing to RTIF has no effect. Reset clears RTIF.

TOIE — Timer Overflow Interrupt Enable Bit

This read/write bit enables timer overflow interrupts. Reset clears TOIE.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

RTIE — Real-Time Interrupt Enable Bit

This read/write bit enables real-time interrupts. Reset clears RTIE.

1 = Real-time interrupts enabled
0 = Real-time interrupts disabled

TOFR — Timer Overflow Flag Reset Bit

Writing a logic 1 to this write-only bit clears the TOF bit. TOFR always reads as logic 0. Reset clears TOFR.

RTIFR — Real-Time Interrupt Flag Reset Bit

Writing a logic 1 to this write-only bit clears the RTIF bit. RTIFR always reads as logic 0. Reset clears RTIFR.

10.5 5.0-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –2.5 mA) PA4–PA7 (I_{Load} = –5.5 mA) PB2–PB3, PA0–PA3	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output low voltage[8] (I_{Load} = 10.0 mA) PA0–PA7, PB2–PB3	V_{OL}	—	—	0.8	V
Input high voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (f_{OP} = 2.1 MHz; f_{OSC} = 4.2 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 4.0 1.0 0.1	 6.0 2.8 5.0	 mA mA µA
Supply current (f_{OP} = 4.0 MHz; f_{OSC} = 8.0 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 5.2 1.1 0.1	 7.0 3.3 5.0	 mA mA µA
I/O Ports Hi-Z leakage current PA0–PA7, PB2–PB3 (without individual pulldown activated)	I_{IL}	—	0.2	±1	µA
Input pulldown current PA0–PA7, PB2–PB3 (with individual pulldown activated)	I_{IL}	35	80	200	µA
Input pullup current $\overline{RESET}$	I_{IL}	–15	–35	–85	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.2	±1	µA
Capacitance Ports (As Inputs or Outputs) $\overline{RESET}$, $\overline{IRQ}$, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{OSC}	1.0	2.0	3.0	MΩ

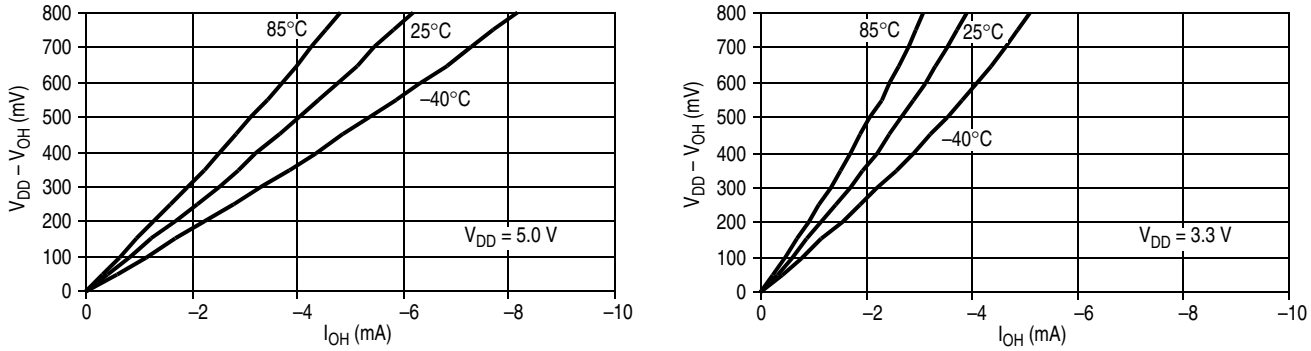
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{OSC} value selected for RC oscillator versions of this device is unspecified.
8. Maximum current drain for all I/O pins combined should not exceed 100 mA.

10.6 3.3-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –0.8 mA) PA4–PA7 (I_{Load} = –1.5 mA) PA0–PA3, PB2–PB3	V_{OH}	V_{DD} –0.3 V_{DD} –0.3	— —	— —	V
Output low voltage (I_{Load} = 5.0 mA) PA4–PA7 (I_{Load} = 3.5 mA) PA0–PA3, PB2–PB3	V_{OL}	— —	— —	0.5 0.5	V
Input high voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (f_{OP} = 1.0 MHz; f_{OSC} = 2.0 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 1.2 0.3 0.1	 2.5 0.8 5.0	 mA mA µA
Supply current (f_{OP} = 2.1 MHz; f_{OSC} = 4.2 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 1.4 0.3 0.1	 3.0 1.0 5.0	 mA mA µA
I/O ports hi-z leakage current PA0–PA7, PB2–PB3 (without individual pulldown activated)	I_{IL}	—	0.1	±1	µA
Input pulldown current PA0–PA7, PB2–PB3 (with individual pulldown activated)	I_{IL}	12	30	100	µA
Input pullup current $\overline{RESET}$	I_{IL}	–10	–25	–45	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.1	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{OSC}	1.0	2.0	3.0	MΩ

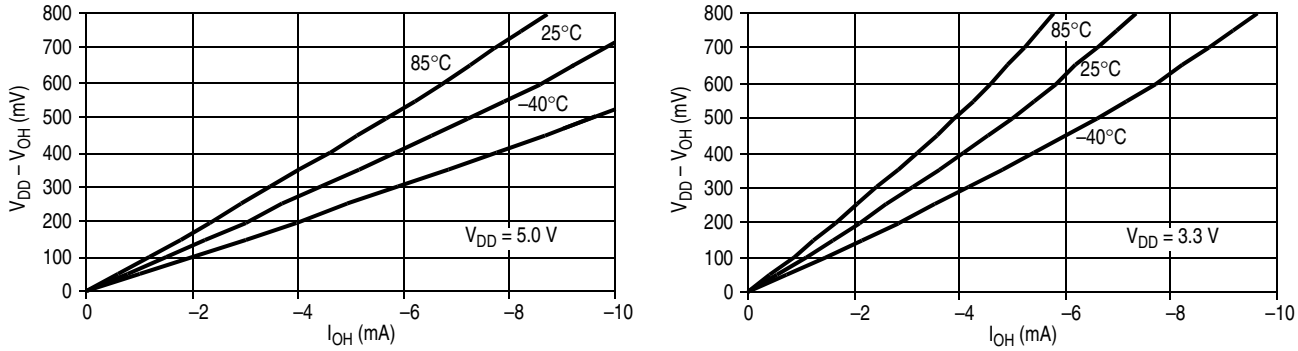
1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{OSC} value selected for RC oscillator versions of this device is unspecified.

10.7 Driver Characteristics



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 800 mV @ I_{OH} = –2.5 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 300 mV @ I_{OH} = –0.8 mA.

Figure 10-1. PA4–PA7 Typical High-Side Driver Characteristics



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 800 mV @ I_{OH} = –5.5 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 300 mV @ I_{OH} = –1.5 mA.

Figure 10-2. PA0–PA3 and PB2–PB3 Typical High-Side Driver Characteristics

10.9 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{IRQ}/V_{PP}$	I_{PP}	—¡	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.

10.10 Control Timing

Table 10-2. Control Timing (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	 — dc	 8.0 8.0	MHz
Internal operating frequency (f_{OSC} ÷ 2) Crystal oscillator External clock	f_{OP}	 — dc	 4.0 4.0	MHz
Cycle time (1 ÷ f_{OP})	t_{cyc}	250	—	ns
$\overline{RESET}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 Interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	100	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

A.5 Typical Internal Operating Frequency Versus Temperature (No External Resistor)

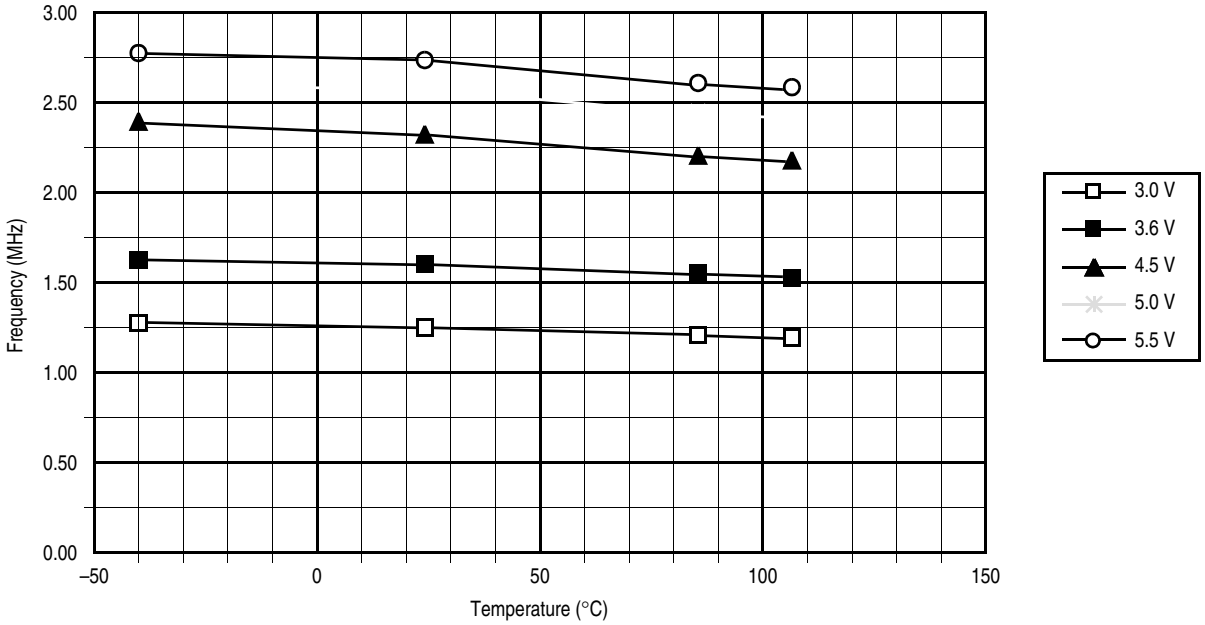


Figure A-4. Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)

NOTE

Due to process variations, operating voltages, and temperature requirements, the internal resistance and tolerance are unspecified. Typically for a given voltage and temperature, the frequency should not vary more than ± 500 kHz. However, this data is not guaranteed. It is the user's responsibility to ensure that the resulting internal operating frequency meets user's requirements.

A.6 Package Types and Order Numbers

Table A-1. MC68HRC705KJ1 (RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	648	16	–40 to +85°C	MC68HRC705KJ1C(2)P(3)
SOIC	751G	16	–40 to +85°C	MC68HRC705KJ1CDW(4)
Cerdip	620A	16	–40 to +85°C	MC68HRC705KJ1CS(5)

1. Refer to Chapter 11 Ordering Information and Mechanical Specifications for standard part ordering information.
2. C = extended temperature range
3. P = plastic dual in-line package (PDIP)
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (Cerdip)