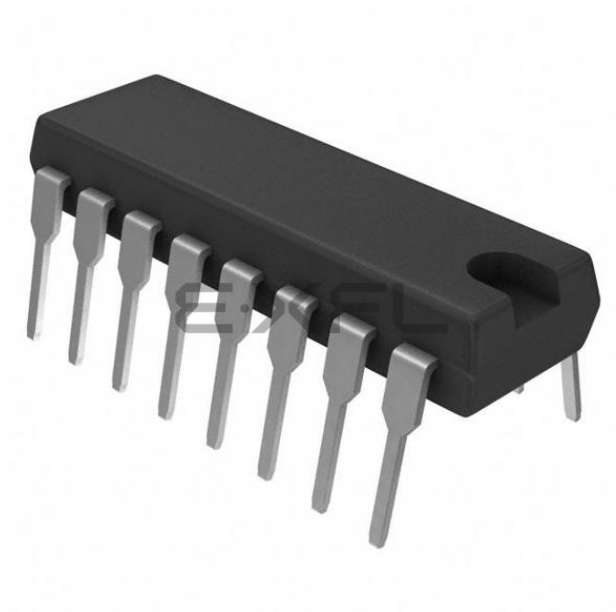

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	10
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705kj1cp

List of Chapters

Chapter 6
Low-Power Modes

Chapter 7
Parallel I/O Ports (PORTS)

Chapter 8
Resets and Interrupts

1.3 Programmable Options

The options in Table 1-1 are programmable in the mask option register.

Table 1-1. Programmable Options

Feature	Option
COP watchdog timer	Enabled or disabled
External interrupt triggering	Edge-sensitive only or edge- and level-sensitive
Port A $\overline{IRQ}$ pin interrupts	Enabled or disabled
Port pulldown resistors	Enabled or disabled
STOP instruction mode	Stop mode or halt mode
Crystal oscillator internal resistor	Enabled or disabled
EPROM security	Enabled or disabled
Short oscillator delay counter	Enabled or disabled

1.4 Pin Functions

Pin assignments are shown in Figure 1-2 with the functions described in the following subsections.

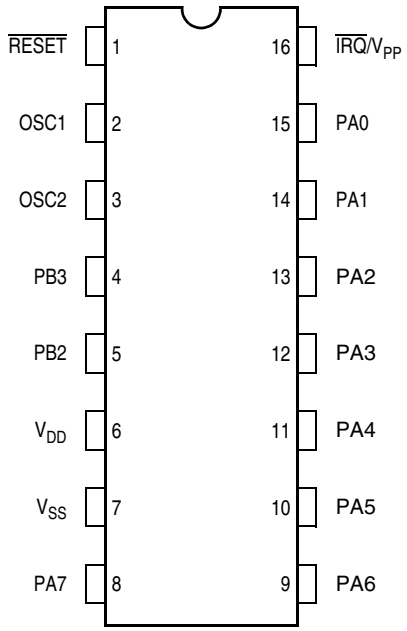


Figure 1-2. Pin Assignments

1.4.1 V_{DD} and V_{SS}

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins, placing high, short-duration current demands on the power supply. To prevent noise problems, take special care, as Figure 1-3 shows, by placing the bypass capacitors as close as possible to the MCU. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.

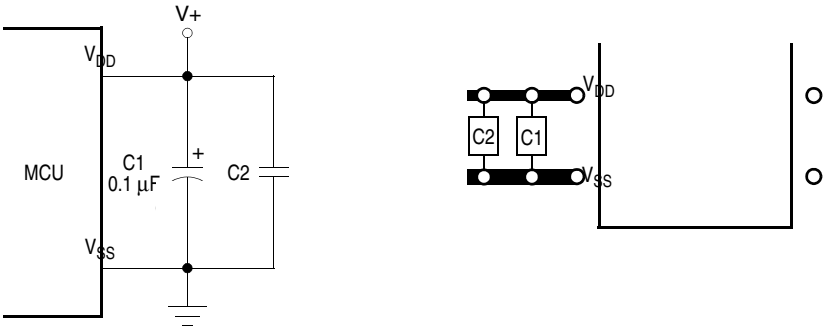


Figure 1-3. Bypassing Layout Recommendation

1.4.2 OSC1 and OSC2

The OSC1 and OSC2 pins are the connections for the on-chip oscillator. The oscillator can be driven by any of the following:

1. Standard crystal (See Figure 1-4 and Figure 1-5.)
2. Ceramic resonator (See Figure 1-6 and Figure 1-7.)
3. Resistor/capacitor (RC) oscillator (Refer to Appendix A MC68HRC705KJ1.)
4. External clock signal as shown in (See Figure 1-8.)
5. Low speed (32 kHz) crystal connections (Refer to Appendix B MC68HLC705KJ1.)

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{OP}.

1.4.2.1 Crystal Oscillator

Figure 1-4 and Figure 1-5 show a typical crystal oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal supplier's recommendations, as the crystal parameters determine the external component values required to provide reliable startup and maximum stability. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances.

To minimize output distortion, mount the crystal and capacitors as close as possible to the pins. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 for the crystal oscillator as a programmable mask option.

NOTE

Use an AT-cut crystal and not an AT-strip crystal because the MCU can overdrive an AT-strip crystal.

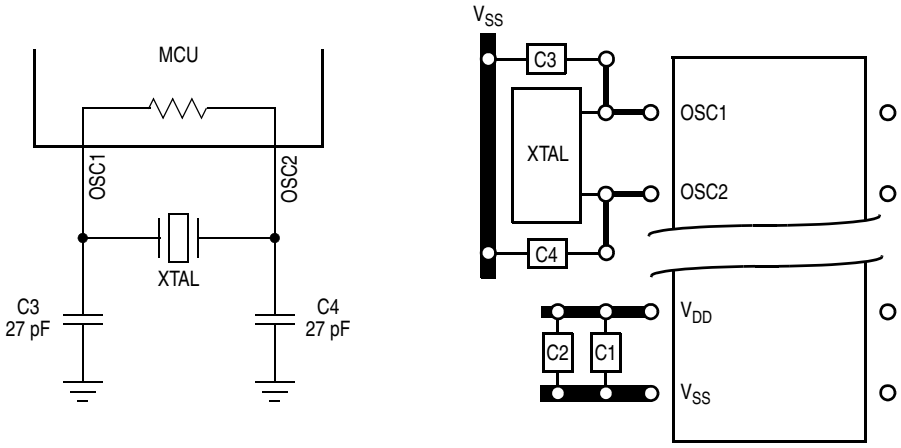


Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option

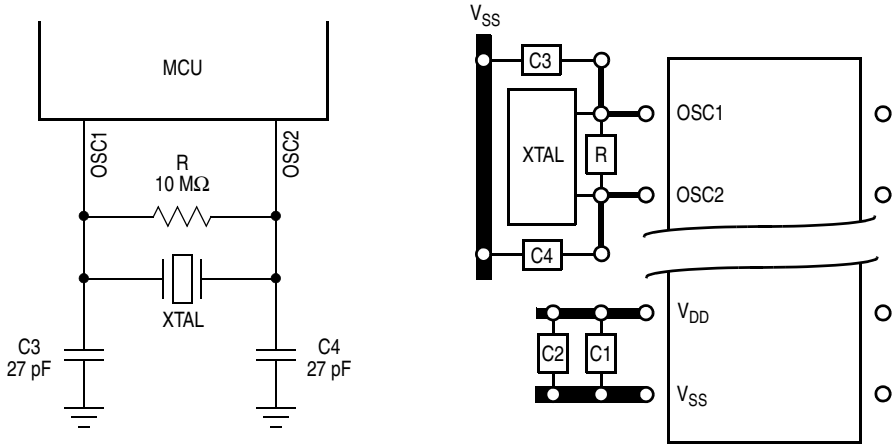


Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option

1.4.2.2 Ceramic Resonator Oscillator

To reduce cost, use a ceramic resonator instead of the crystal. The circuits shown in Figure 1-6 and Figure 1-7 show ceramic resonator circuits. Follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 as a programmable mask option.

4.5 CPU Registers

The M68HC05 CPU contains five registers that control and monitor MCU operation:

- Accumulator
- Index register
- Stack pointer
- Program counter
- Condition code register

CPU registers are not memory mapped.

4.5.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and results of ALU operations.

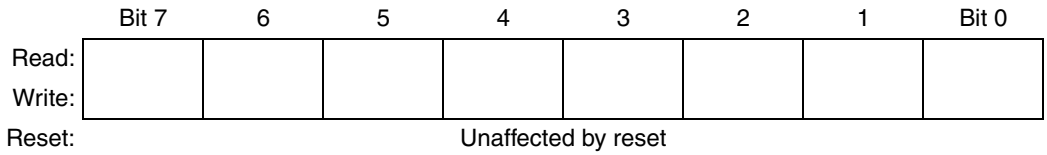


Figure 4-2. Accumulator (A)

4.5.2 Index Register

In the indexed addressing modes, the CPU uses the byte in the index register to determine the conditional address of the operand. The index register also can serve as a temporary storage location or a counter.

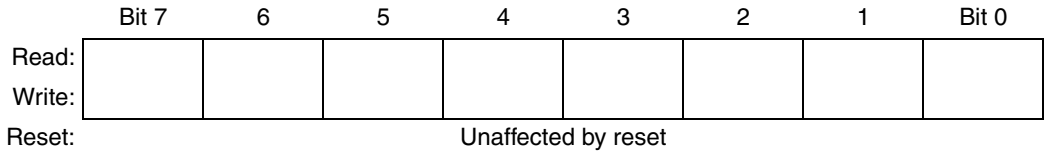


Figure 4-3. Index Register (X)

4.5.3 Stack Pointer

The stack pointer is a 16-bit register that contains the address of the next location on the stack. During a reset or after the reset stack pointer instruction (RSP), the stack pointer is preset to $00FF. The address in the stack pointer decrements after a byte is stacked and increments before a byte is unstacked.

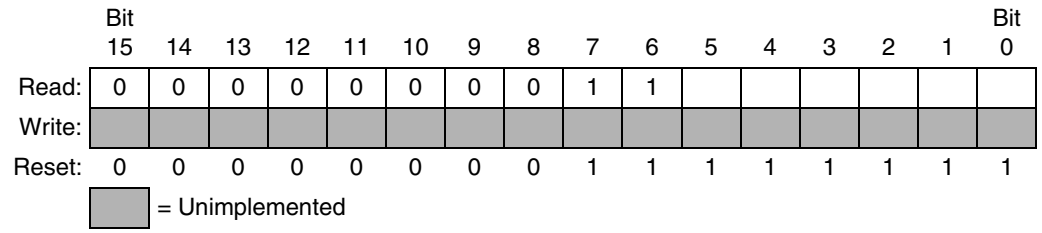


Figure 4-4. Stack Pointer (SP)

When using the Freescale assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

4.6.1.5 Indexed, No Offset

Indexed instructions with no offset are 1-byte instructions that can access data with variable addresses within the first 256 memory locations. The index register contains the low byte of the effective address of the operand. The CPU automatically uses $00 as the high byte, so these instructions can address locations $0000–$00FF.

Indexed, no offset instructions are often used to move a pointer through a table or to hold the address of a frequently used RAM or input/output (I/O) location.

4.6.1.6 Indexed, 8-Bit Offset

Indexed, 8-bit offset instructions are 2-byte instructions that can access data with variable addresses within the first 511 memory locations. The CPU adds the unsigned byte in the index register to the unsigned byte following the opcode. The sum is the effective address of the operand. These instructions can access locations $0000–$01FE.

Indexed 8-bit offset instructions are useful for selecting the kth element in an n-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 ($01FE). The k value is typically in the index register, and the address of the beginning of the table is in the byte following the opcode.

4.6.1.7 Indexed, 16-Bit Offset

Indexed, 16-bit offset instructions are 3-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned byte in the index register to the two unsigned bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte of the offset.

Indexed, 16-bit offset instructions are useful for selecting the kth element in an n-element table anywhere in memory.

As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

4.6.1.8 Relative

Relative addressing is only for branch instructions. If the branch condition is true, the CPU finds the effective branch destination by adding the signed byte following the opcode to the contents of the program counter. If the branch condition is not true, the CPU goes to the next instruction. The offset is a signed, two’s complement byte that gives a branching range of –128 to +127 bytes from the address of the next location after the branch instruction.

When using the Freescale assembler, the programmer does not need to calculate the offset because the assembler determines the proper offset and verifies that it is within the span of the branch.

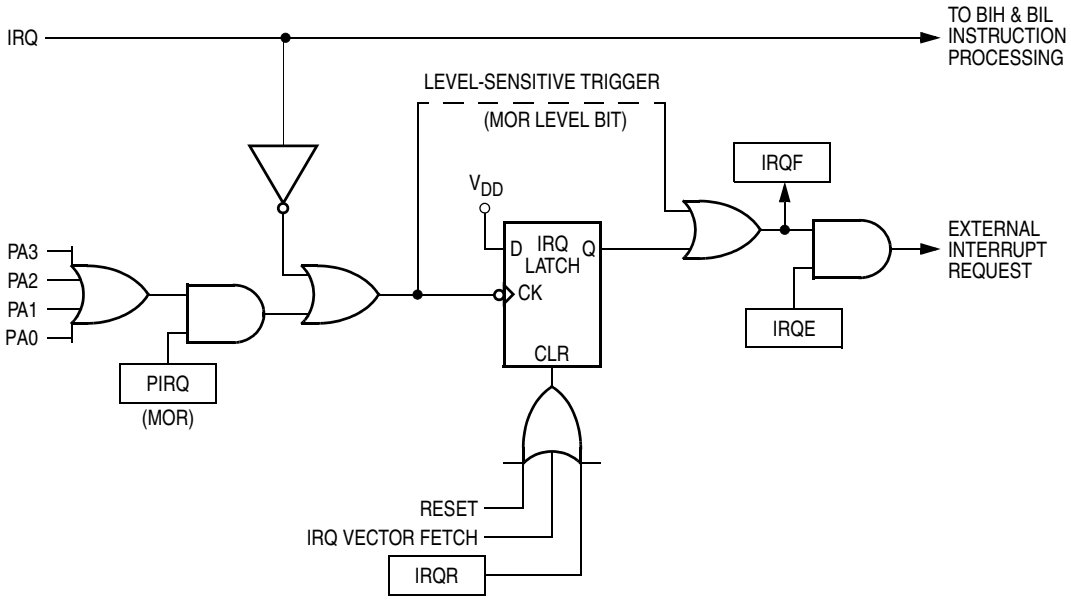


Figure 5-1. IRQ Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	IRQ Status and Control Register (ISCR) See page 54.	Read:	IRQE	0	0	0	IRQF	0	0	0
		Write:				R			IRQR	
		Reset:	1	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 5-2. IRQ Module I/O Register Summary

If edge-sensitive-only triggering is selected, a falling edge on the $\overline{IRQ}/V_{PP}$ pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level on the $\overline{IRQ}/V_{PP}$ pin returns to logic 1 and then falls again to logic 0.

The $\overline{IRQ}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin can affect the mode of operation and should not exceed V_{DD}.

5.3.2 Optional External Interrupts

The inputs for the lower four bits of port A (PA0–PA3) can be connected to the $\overline{IRQ}$ pin input of the CPU if enabled by the PIRQ bit in the mask option register. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{IRQ}/V_{PP}$ pin except for the inverted phase (logic 1, rising edge). The active state of the $\overline{IRQ}/V_{PP}$ pin is a logic 0 (falling edge).

The PA0–PA3 pins are selected as a group to function as IRQ interrupts and are enabled by the IRQE bit in the IRQ status and control register. The PA0–PA3 pins can be positive-edge triggered only or positive-edge and high-level triggered.

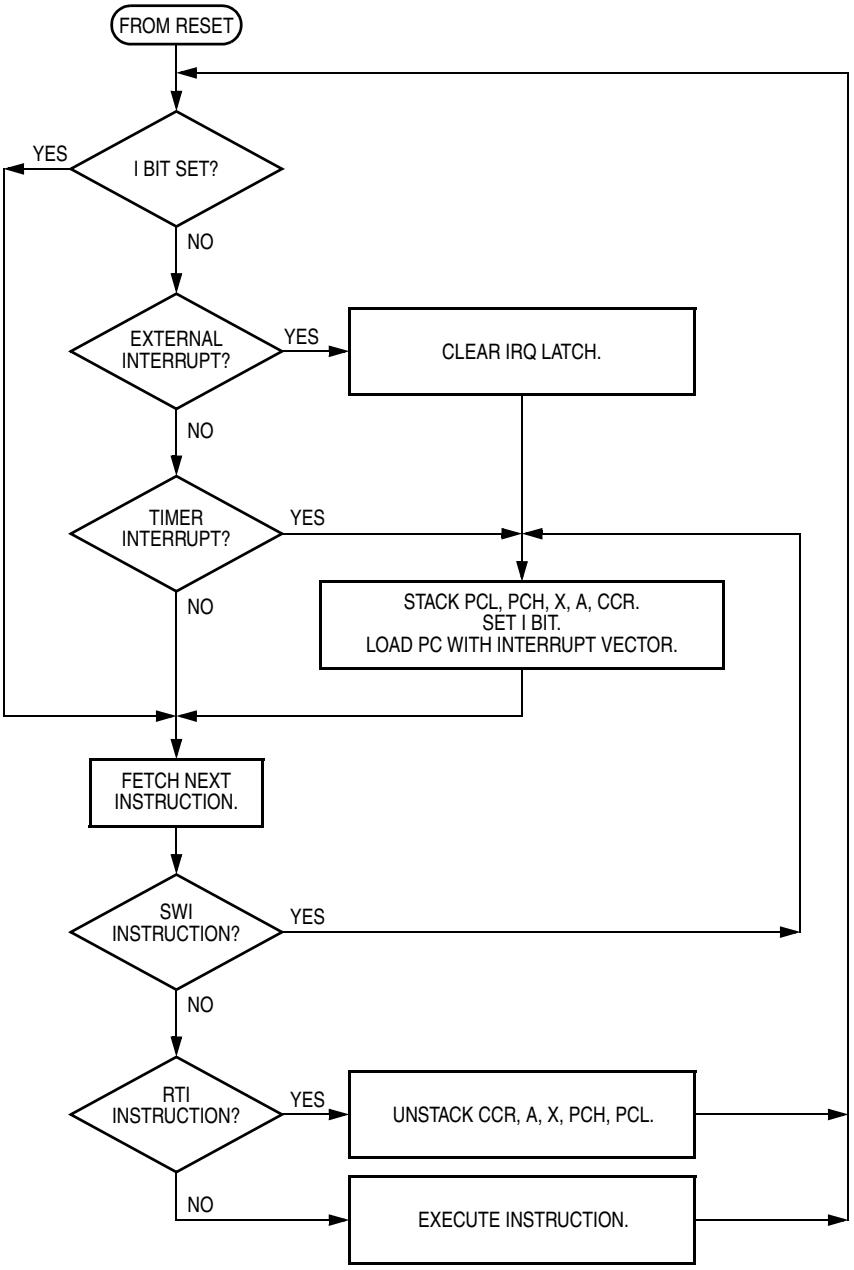


Figure 5-3. Interrupt Flowchart

6.3.5.1 STOP

The STOP instruction during EPROM programming clears the EPGM bit in the EPROM programming register, removing the programming voltage from the EPROM.

6.3.5.2 WAIT

The WAIT instruction has no effect on EPROM/OTPROM operation.

6.4 Data-Retention Mode

In data-retention mode, the MCU retains RAM contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. The data-retention feature allows the MCU to remain in a low power-consumption state during which it retains data, but the CPU cannot execute instructions.

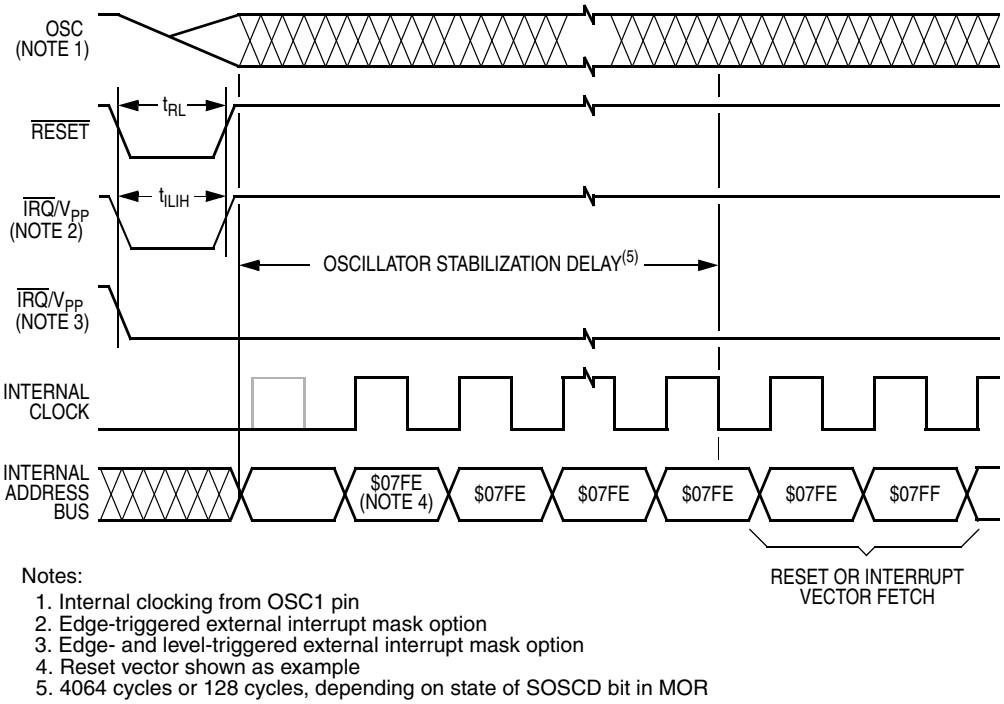
To put the MCU in data-retention mode:

1. Drive the $\overline{\text{RESET}}$ pin to logic 0.
2. Lower the V_{DD} voltage. The $\overline{\text{RESET}}$ pin must remain low continuously during data-retention mode.

To take the MCU out of data-retention mode:

1. Return V_{DD} to normal operating voltage.
2. Return the $\overline{\text{RESET}}$ pin to logic 1.

6.5 Timing



Notes:
1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example
5. 4064 cycles or 128 cycles, depending on state of SOSCD bit in MOR

Figure 6-1. Stop Mode Recovery Timing

Chapter 8
Resets and Interrupts

8.1 Introduction

Reset initializes the MCU by returning the program counter to a known address and by forcing control and status bits to known states.

Interrupts temporarily change the sequence of program execution to respond to events that occur during processing.

8.2 Resets

A reset immediately stops the operation of the instruction being executed, initializes certain control and status bits, and loads the program counter with a user-defined reset vector address. The following sources can generate a reset:

- Power-on reset (POR) circuit
- $\overline{\text{RESET}}$ pin
- Computer operating properly (COP) watchdog
- Illegal address

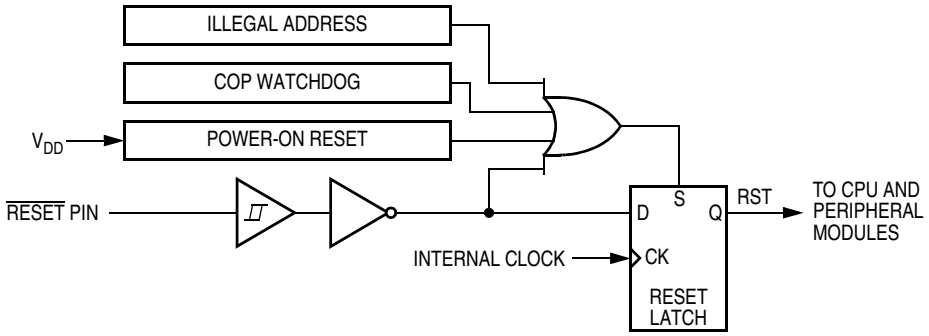


Figure 8-1. Reset Sources

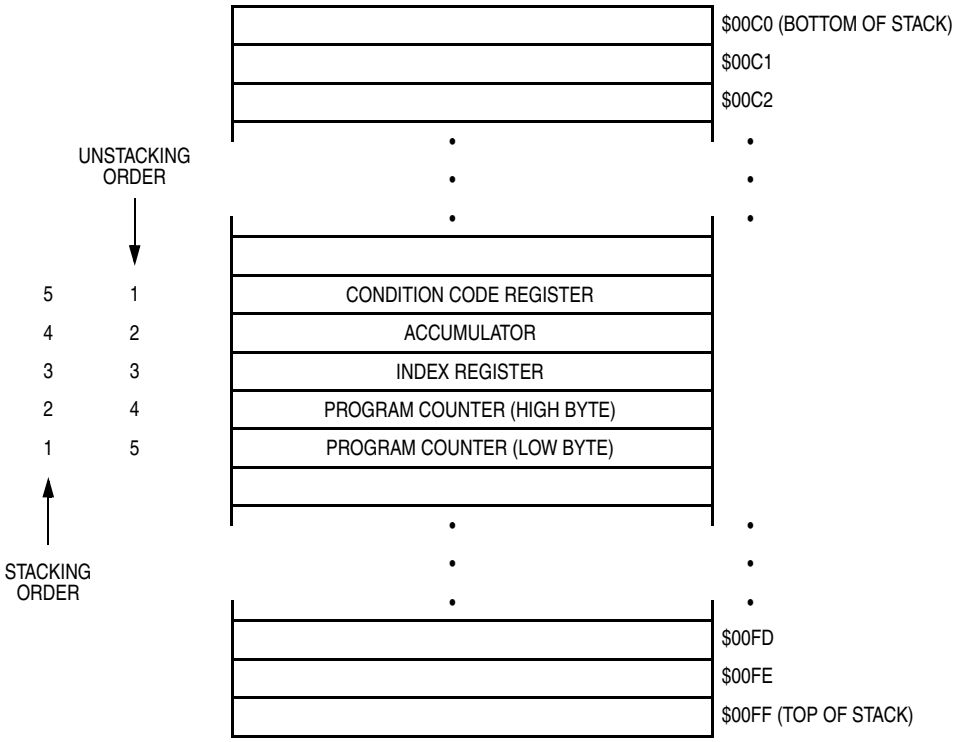


Figure 8-6. Interrupt Stacking Order

Table 8-4. Reset/Interrupt Vector Addresses

Function	Source	Local Mask	Global Mask	Priority (1 = Highest)	Vector Address
Reset	Power-On $\overline{\text{RESET}}$ Pin COP Watchdog(1) Illegal Address	None	None	1	$07FE–$07FF
Software Interrupt (SWI)	User Code	None	None	Same Priority as Instruction	$07FC–$07FD
External Interrupt	$\overline{\text{IRQ}}/V_{PP}$ Pin	IRQE	I Bit	2	$07FA–$07FB
Timer Interrupts	RTIF Bit TOF Bit	RTIE Bit TOIE Bit	I Bit	3	$07F8–$07F9

1. The COP watchdog is programmable in the mask option register.

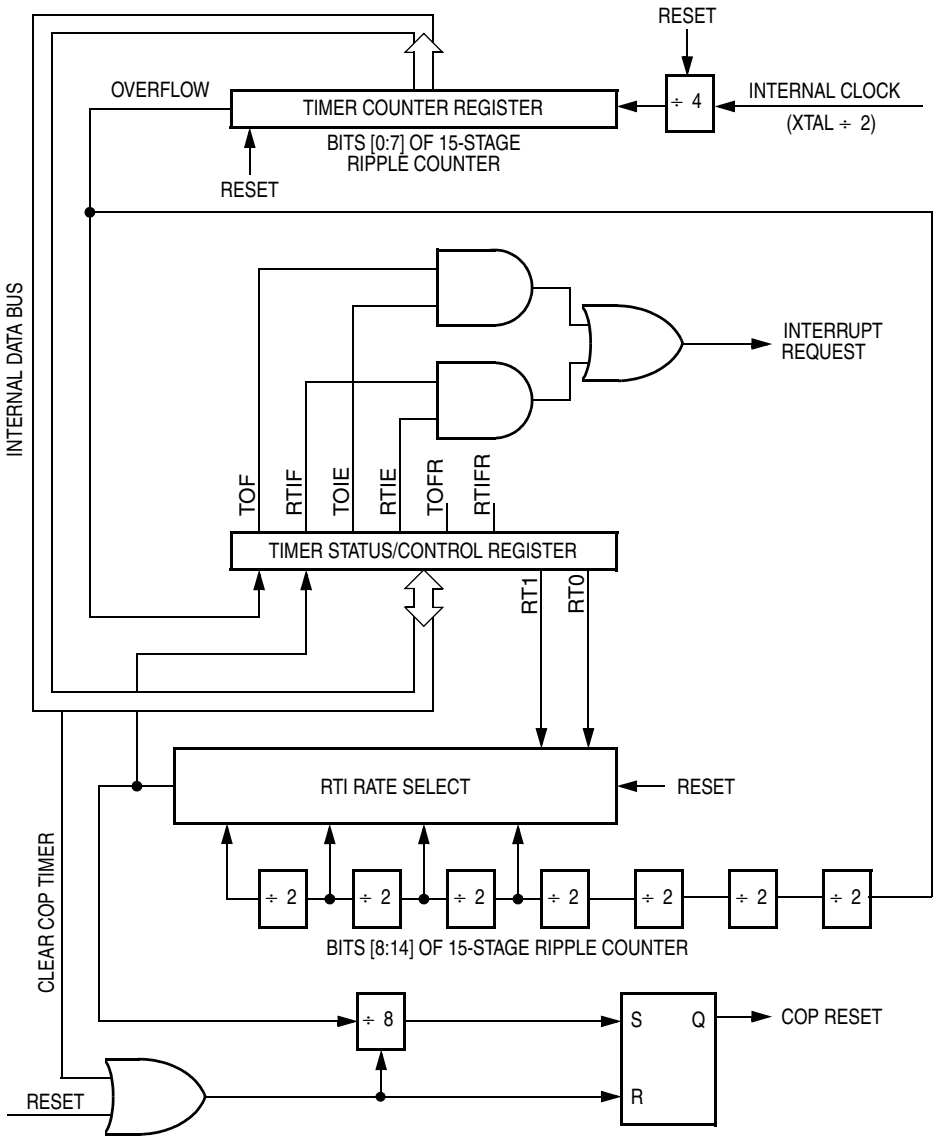


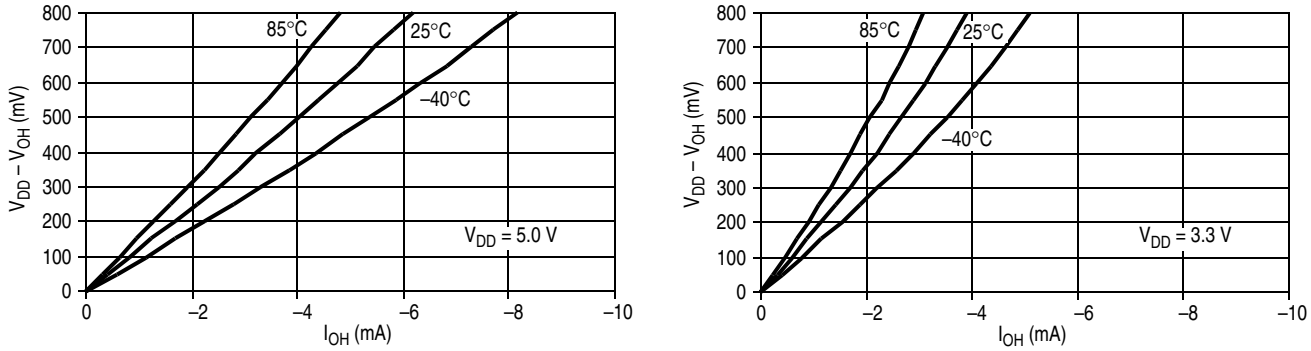
Figure 9-2. Multifunction Timer Block Diagram

9.4 Interrupts

The following timer sources can generate interrupts:

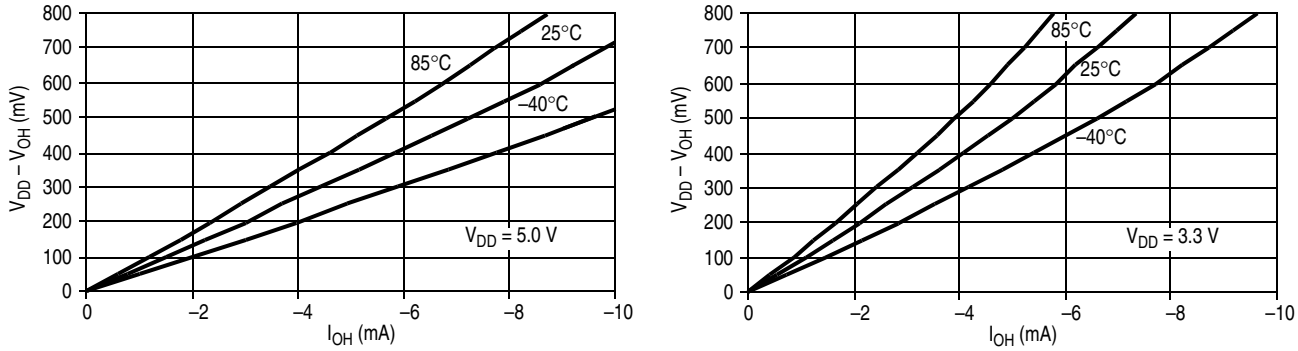
- Timer overflow flag (TOF) — The TOF bit is set when the first eight stages of the counter roll over from $FF to $00. The timer overflow interrupt enable bit, TOIE, enables TOF interrupt requests.
- Real-time interrupt flag (RTIF) — The RTIF bit is set when the selected RTI output becomes active. The real-time interrupt enable bit, RTIE, enables RTIF interrupt requests.

10.7 Driver Characteristics



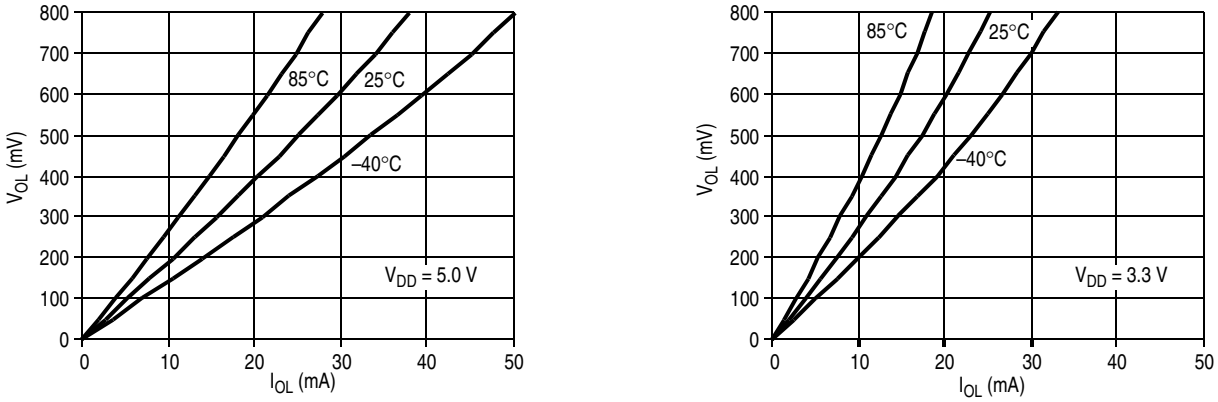
Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 800 mV @ I_{OH} = –2.5 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 300 mV @ I_{OH} = –0.8 mA.

Figure 10-1. PA4–PA7 Typical High-Side Driver Characteristics



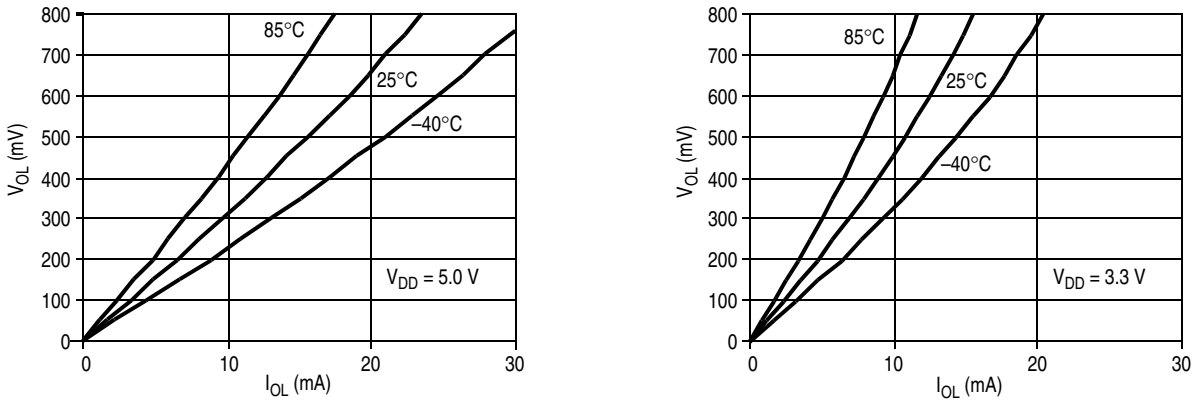
Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 800 mV @ I_{OH} = –5.5 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for (V_{DD} – V_{OH}) ≤ 300 mV @ I_{OH} = –1.5 mA.

Figure 10-2. PA0–PA3 and PB2–PB3 Typical High-Side Driver Characteristics



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 800$ mV @ I_{OL} = 10.0 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 500$ mV @ I_{OL} = 5.0 mA.

Figure 10-3. PA4–PA7 Typical Low-Side Driver Characteristics



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 800$ mV @ I_{OL} = 10.0 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 500$ mV @ I_{OL} = 3.5 mA.

Figure 10-4. PA0–PA3 and PB2–PB3 Typical Low-Side Driver Characteristics

Table 10-3. Control Timing (V_{DD} = 3.3 Vdc)(1)

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	— dc	4.2 4.2	MHz
Internal operating frequency ($f_{OSC} \div 2$) Crystal oscillator External clock	f_{OP}	— dc	2.1 2.1	MHz
Cycle time ($1 \div f_{OP}$)	t_{cyc}	476	—	ns
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note(2)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note(2)	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

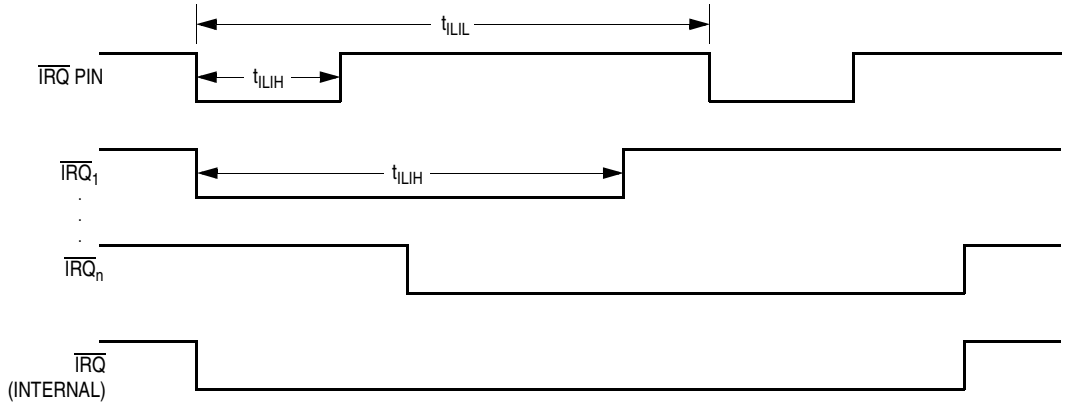


Figure 10-7. External Interrupt Timing

Chapter 11
Ordering Information and Mechanical Specifications

11.1 Introduction

The MC68HC705J1A, the RC oscillator, and low-speed option devices described in Appendix A MC68HRC705KJ1 and Appendix B MC68HLC705KJ1 are available in these packages:

- 648 — Plastic dual in-line package (PDIP)
- 751G — Small outline integrated circuit (SOIC)
- 620A — Ceramic DIP (Cerdip) (windowed)

This section contains ordering information and mechanical specifications for the available package types.

11.2 MCU Order Numbers

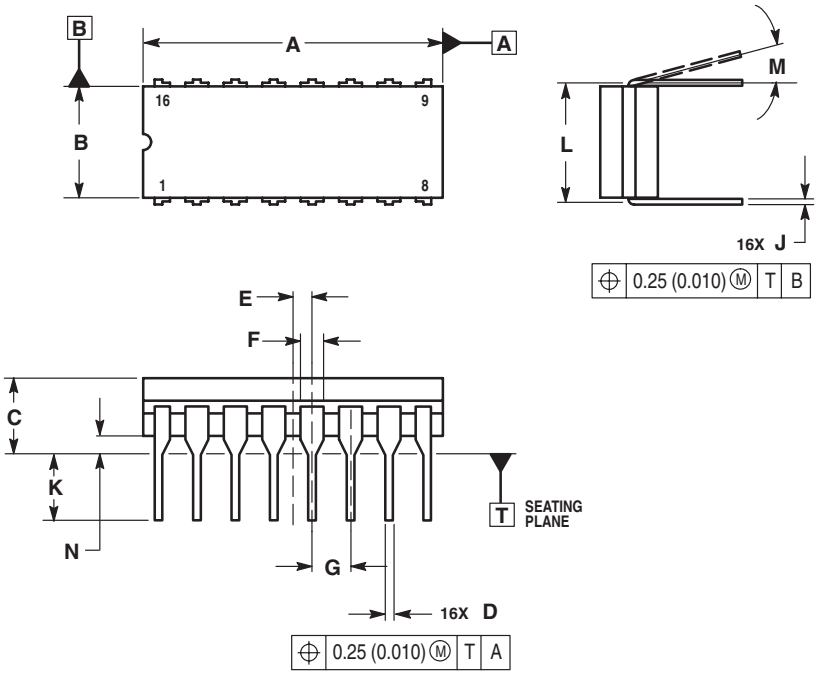
Table 11-1 lists the MC order numbers.

Table 11-1. Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	648	16	–40 to +85°C	MC68HC705KJ1C(2)
SOIC	751G	16	–40 to +85°C	MC68HC705KJ1CDW(3)
Cerdip	620A	16	–40 to +85°C	MC68HC705KJ1CS(4)

1. Refer to Appendix A MC68HRC705KJ1 and Appendix B MC68HLC705KJ1 for ordering information on optional low-speed and resistor-capacitor oscillator devices.
2. C = extended temperature range
3. DW = small outline integrated circuit (SOIC)
4. S = ceramic dual in-line package (Cerdip)

11.5 16-Pin Cerdip — Case #620A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

A.3 Typical Internal Operating Frequency for RC Oscillator Option

Figure A-2 shows typical internal operating frequencies at 25°C for the RC oscillator option.

NOTE

Tolerance for resistance is ± 50%. When selecting resistor size, consider the tolerance to ensure that the resulting oscillator frequency does not exceed the maximum operating frequency.

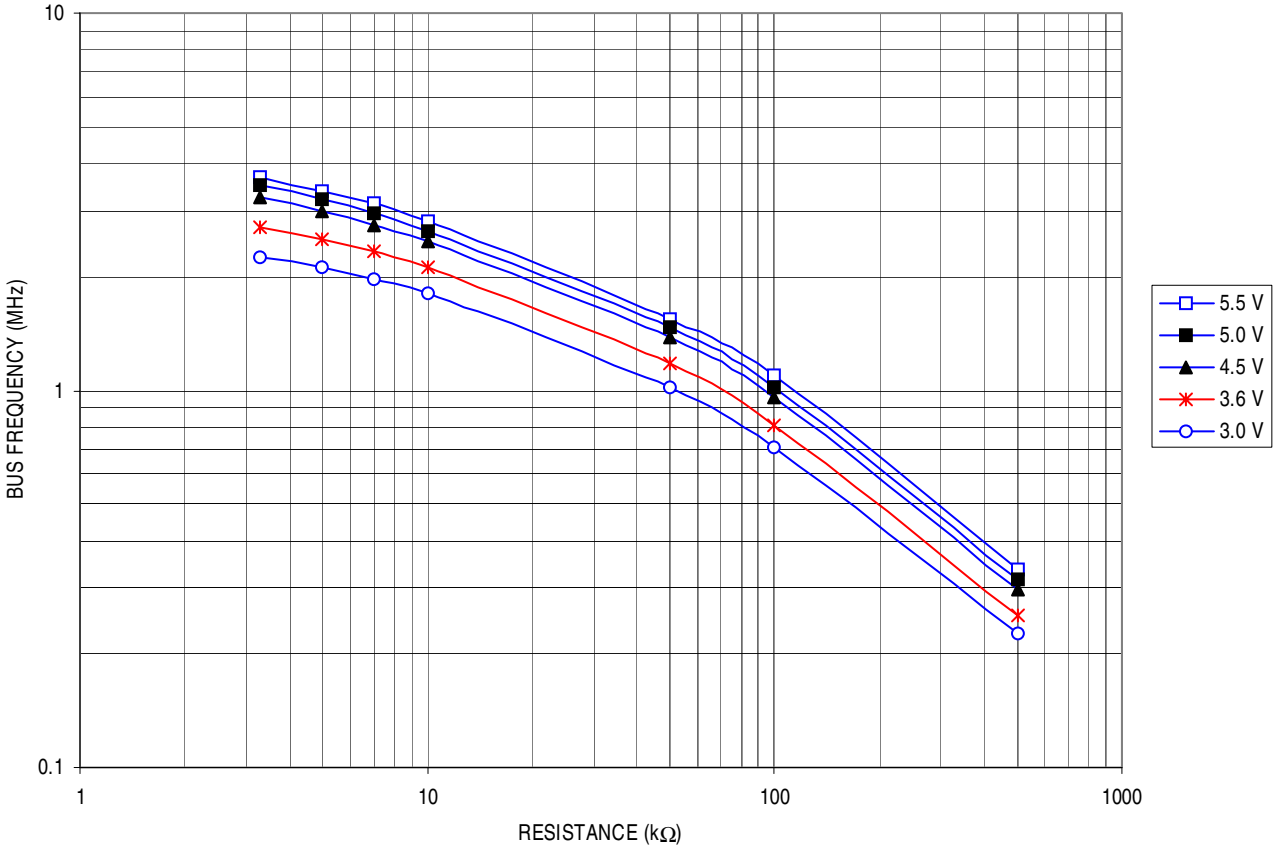


Figure A-2. Typical Internal Operating Frequency for Various V_{DD} at 25°C — RC Oscillator Option Only