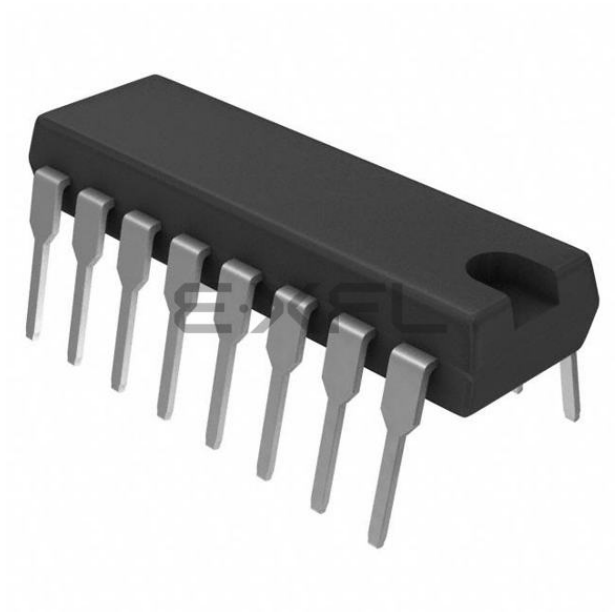

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	10
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mchc705kj1cpe

Table of Contents

Appendix A
MC68HRC705KJ1

Appendix B
MC68HLC705KJ1

Chapter 1
Introduction

1.1 Features

Features on the MC68HC705KJ1 include:

- Robust noise immunity
- 4.0-MHz internal operating frequency at 5.0 V
- 1240 Bytes of EPROM/OTPROM (electrically programmable read-only memory/one-time programmable read-only memory), including eight bytes for user vectors
- 64 bytes of user RAM
- Peripheral modules:
  - 15-stage multifunction timer
  - Computer operating properly (COP) watchdog
- 10 bidirectional input/output (I/O) lines, including:
  - 10-mA sink capability on all I/O pins
  - Software programmable pulldowns on all I/O pins
  - Keyboard scan with selectable interrupt on four I/O pins
  - 5.5-mA source capability on six I/O pins
- Selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with connections for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator (MC68HRC705KJ1) with or without external resistor
  - External clock
  - Low-speed (32-kHz) crystal (MC68HLC705KJ1)
- Memory-mapped I/O registers
- Fully static operation with no minimum clock speed
- Power-saving stop, halt, wait, and data-retention modes
- External interrupt mask bit and acknowledge bit
- Illegal address reset
- Internal steering diode and pullup resistor from $\overline{\text{RESET}}$ pin to V_{DD}
- Selectable EPROM security[1]
- Selectable oscillator bias resistor

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

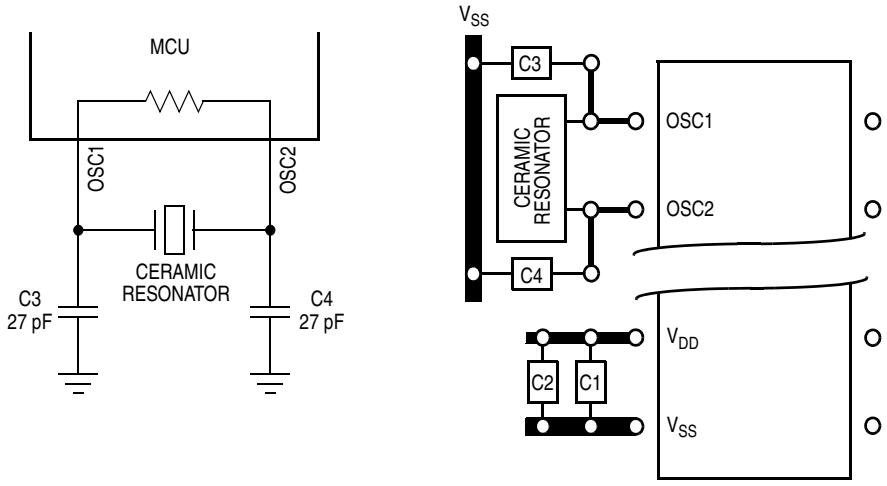


Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option

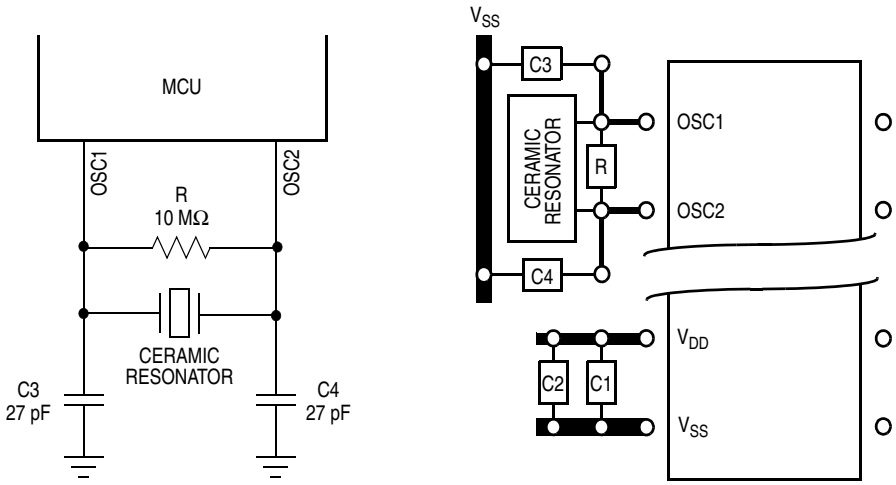


Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option

1.4.2.3 RC Oscillator

Refer to Appendix A MC68HRC705KJ1.

2.6 RAM

The 64 addresses from $00C0 to $00FF serve as both the user RAM and the stack RAM. Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements when the CPU stores a byte on the stack and increments when the CPU retrieves a byte from the stack.

NOTE

Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.

2.7 EPROM/OTPROM

An MCU with a quartz window has 1240 bytes of erasable, programmable ROM (EPROM). The quartz window allows EPROM erasure with ultraviolet light.

NOTE

Keep the quartz window covered with an opaque material except when erasing the MCU. Ambient light can affect MCU operation.

In an MCU without the quartz window, the EPROM cannot be erased and serves as 1240 bytes of one-time programmable ROM (OTPROM).

The following addresses are user EPROM/OTPROM locations:

- $0300–$07CF
- $07F8–$07FF, used for user-defined interrupt and reset vectors

The COP register (COPR) is an EPROM/OTPROM location at address $07F0.

The mask option register (MOR) is an EPROM/OTPROM location at address $07F1.

2.7.1 EPROM/OTPROM Programming

The two ways to program the EPROM/OTPROM are:

- Manipulating the control bits in the EPROM programming register to program the EPROM/OTPROM on a byte-by-byte basis
- Programming the EPROM/OTPROM with the M68HC705J In-Circuit Simulator (M68HC705JICS) available from Freescale

2.7.2 EPROM Programming Register

The EPROM programming register (EPROG) contains the control bits for programming the EPROM/OTPROM.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	ELAT	MPGM	EPGM
Write:		R	R	R	R			
Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 2-3. EPROM Programming Register (EPROG)

ELAT — EPROM Bus Latch Bit

This read/write bit latches the address and data buses for EPROM/OTPROM programming. Clearing the ELAT bit automatically clears the EPGM bit. EPROM/OTPROM data cannot be read while the ELAT bit is set. Reset clears the ELAT bit.

1 = Address and data buses configured for EPROM/OTPROM programming the EPROM
0 = Address and data buses configured for normal operation

MPGM — MOR Programming Bit

This read/write bit applies programming power from the $\overline{IRQ}/V_{PP}$ pin to the mask option register. Reset clears MPGM.

1 = Programming voltage applied to MOR
0 = Programming voltage not applied to MOR

EPGM — EPROM Programming Bit

This read/write bit applies the voltage from the $\overline{IRQ}/V_{PP}$ pin to the EPROM. To write the EPGM bit, the ELAT bit must be set already. Reset clears EPGM.

1 = Programming voltage ($\overline{IRQ}/V_{PP}$ pin) applied to EPROM
0 = Programming voltage ($\overline{IRQ}/V_{PP}$ pin) not applied to EPROM

NOTE

Writing logic 1s to both the ELAT and EPGM bits with a single instruction sets ELAT and clears EPGM. ELAT must be set first by a separate instruction.

Bits [7:3] — Reserved

Take the following steps to program a byte of EPROM/OTPROM:

1. Apply the programming voltage, V_{PP}, to the $\overline{IRQ}/V_{PP}$ pin.
2. Set the ELAT bit.
3. Write to any EPROM/OTPROM address.
4. Set the EPGM bit and wait for a time, t_{EPGM}.
5. Clear the ELAT bit.

2.7.3 EPROM Erasing

The erased state of an EPROM bit is logic 0. Erase the EPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wavelength of 2537 angstroms. Position the ultraviolet light source one inch from the EPROM. Do not use a shortwave filter.

Chapter 4
Central Processor Unit (CPU)

4.1 Introduction

The central processor unit (CPU) consists of a CPU control unit, an arithmetic/logic unit (ALU), and five CPU registers. The CPU control unit fetches and decodes instructions. The ALU executes the instructions. The CPU registers contain data, addresses, and status bits that reflect the results of CPU operations.

4.2 Features

Features of the CPU include:

- 4.0-MHz bus frequency on standard part
- 8-bit accumulator
- 8-bit index register
- 11-bit program counter
- 6-bit stack pointer
- Condition code register with five status flags
- 62 instructions
- 8 addressing modes
- Power-saving stop, wait, halt, and data-retention modes

The programming model is shown in Figure 4-1.

4.3 CPU Control Unit

The CPU control unit fetches and decodes instructions during program operation. The control unit selects the memory locations to read and write and coordinates the timing of all CPU operations.

4.4 Arithmetic/Logic Unit

The arithmetic/logic unit (ALU) performs the arithmetic, logic, and manipulation operations decoded from the instruction set by the CPU control unit. The ALU produces the results called for by the program and sets or clears status and control bits in the condition code register (CCR).

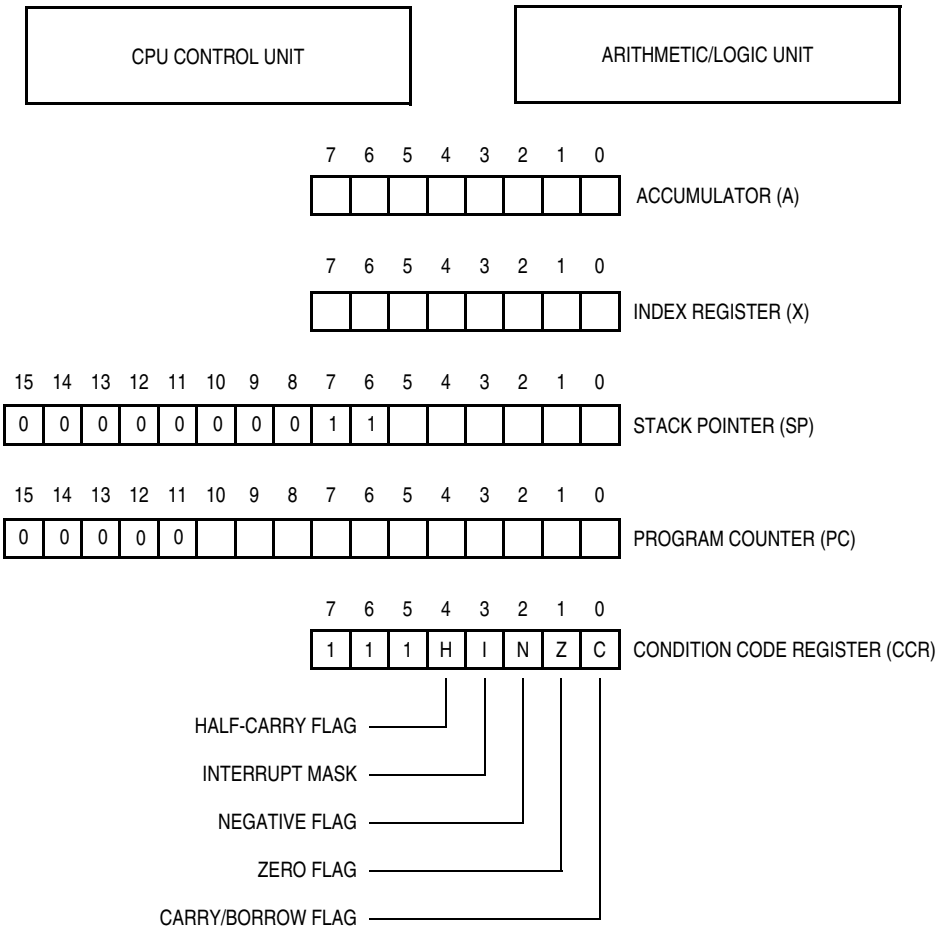


Figure 4-1. Programming Model

4.6.2.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 4-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

NOTE

Do not use bit manipulation instructions on registers with write-only bits.

4.6.2.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 4-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

Table 4-6. Instruction Set Summary (Sheet 5 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	—	—	—	—	—	INH	81		6
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff	4 5 6 5 4
STOP	Stop Oscillator and Enable IRQ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		1 0
TAX	Transfer Accumulator to Index Register	X ← (A)	—	—	—	—	—	INH	97		2
TST *opr* TSTA TSTX TST *opr*,X TST ,X	Test Memory Byte for Negative or Zero	(M) – $00	—	—	↕	↕	—	DIR INH INH IX1 IX	3D 4D 5D 6D 7D	dd ff	4 3 3 5 4

6.3 Effects of Stop and Wait Modes

The STOP and WAIT instructions have the following effects on MCU modules.

6.3.1 Clock Generation

Effects of STOP and WAIT on clock generation are discussed here.

6.3.1.1 STOP

The STOP instruction disables the internal oscillator, stopping the CPU clock and all peripheral clocks.

After exiting stop mode, the CPU clock and all enabled peripheral clocks begin running after the oscillator stabilization delay.

NOTE

The oscillator stabilization delay holds the MCU in reset for the first 4064 internal clock cycles.

6.3.1.2 WAIT

The WAIT instruction disables the CPU clock.

After exiting wait mode, the CPU clock and all enabled peripheral clocks immediately begin running.

6.3.2 CPU

Effects of STOP and WAIT on the CPU are discussed here.

6.3.2.1 STOP

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

After exit from stop mode by external interrupt, the I bit remains clear.

After exit from stop mode by reset, the I bit is set.

6.3.2.2 WAIT

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts
- Disables the CPU clock

After exit from wait mode by interrupt, the I bit remains clear.

After exit from wait mode by reset, the I bit is set.

6.3.3 COP Watchdog

Effects of STOP and WAIT on the COP watchdog are discussed here.

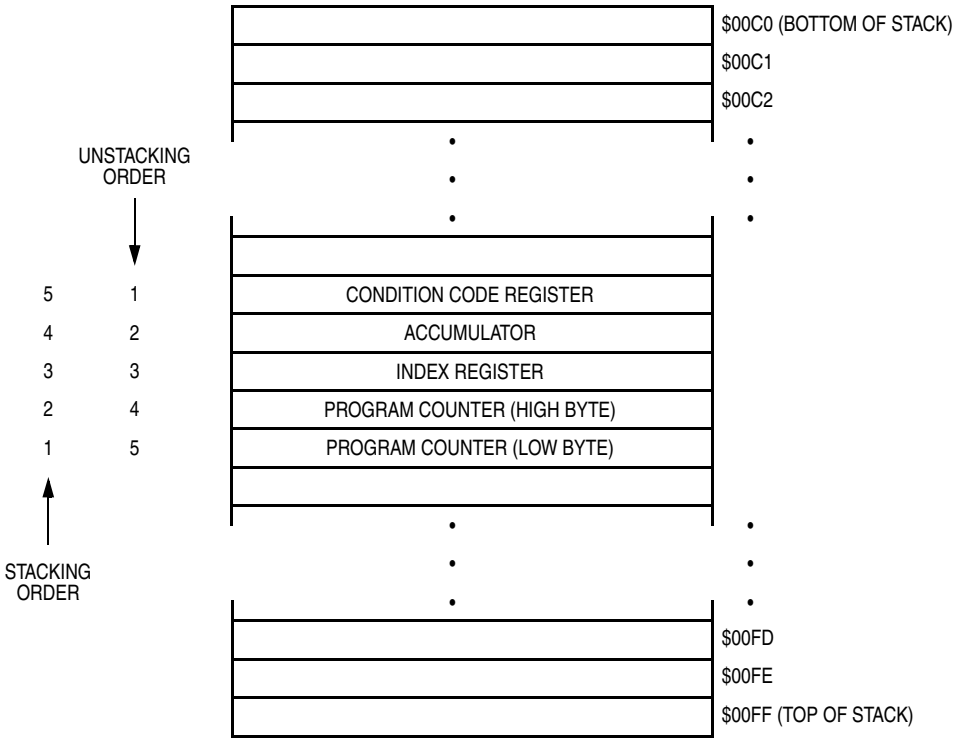


Figure 8-6. Interrupt Stacking Order

Table 8-4. Reset/Interrupt Vector Addresses

Function	Source	Local Mask	Global Mask	Priority (1 = Highest)	Vector Address
Reset	Power-On $\overline{\text{RESET}}$ Pin COP Watchdog(1) Illegal Address	None	None	1	$07FE–$07FF
Software Interrupt (SWI)	User Code	None	None	Same Priority as Instruction	$07FC–$07FD
External Interrupt	$\overline{\text{IRQ}}/V_{PP}$ Pin	IRQE	I Bit	2	$07FA–$07FB
Timer Interrupts	RTIF Bit TOF Bit	RTIE Bit TOIE Bit	I Bit	3	$07F8–$07F9

1. The COP watchdog is programmable in the mask option register.

9.5 I/O Registers

The following registers control and monitor the timer operation:

- Timer status and control register (TSCR)
- Timer counter register (TCR)

9.5.1 Timer Status and Control Register

The read/write timer status and control register performs the following functions:

- Flags timer interrupts
- Enables timer interrupts
- Resets timer interrupt flags
- Selects real-time interrupt rates

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
Write:					TOFR	RTIFR		
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 9-3. Timer Status and Control Register (TSCR)

TOF — Timer Overflow Flag

This read-only flag becomes set when the first eight stages of the counter roll over from $FF to $00. TOF generates a timer overflow interrupt request if TOIE is also set. Clear TOF by writing a logic 1 to the TOFR bit. Writing to TOF has no effect. Reset clears TOF.

RTIF — Real-Time Interrupt Flag

This read-only flag becomes set when the selected RTI output becomes active. RTIF generates a real-time interrupt request if RTIE is also set. Clear RTIF by writing a logic 1 to the RTIFR bit. Writing to RTIF has no effect. Reset clears RTIF.

TOIE — Timer Overflow Interrupt Enable Bit

This read/write bit enables timer overflow interrupts. Reset clears TOIE.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

RTIE — Real-Time Interrupt Enable Bit

This read/write bit enables real-time interrupts. Reset clears RTIE.

1 = Real-time interrupts enabled
0 = Real-time interrupts disabled

TOFR — Timer Overflow Flag Reset Bit

Writing a logic 1 to this write-only bit clears the TOF bit. TOFR always reads as logic 0. Reset clears TOFR.

RTIFR — Real-Time Interrupt Flag Reset Bit

Writing a logic 1 to this write-only bit clears the RTIF bit. RTIFR always reads as logic 0. Reset clears RTIFR.

10.9 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{IRQ}/V_{PP}$	I_{PP}	—¡	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.

10.10 Control Timing

Table 10-2. Control Timing (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	 — dc	 8.0 8.0	MHz
Internal operating frequency (f_{OSC} ÷ 2) Crystal oscillator External clock	f_{OP}	 — dc	 4.0 4.0	MHz
Cycle time (1 ÷ f_{OP})	t_{cyc}	250	—	ns
$\overline{RESET}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 Interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	100	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

Table 10-3. Control Timing (V_{DD} = 3.3 Vdc)(1)

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	— dc	4.2 4.2	MHz
Internal operating frequency ($f_{OSC} \div 2$) Crystal oscillator External clock	f_{OP}	— dc	2.1 2.1	MHz
Cycle time ($1 \div f_{OP}$)	t_{cyc}	476	—	ns
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note(2)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note(2)	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

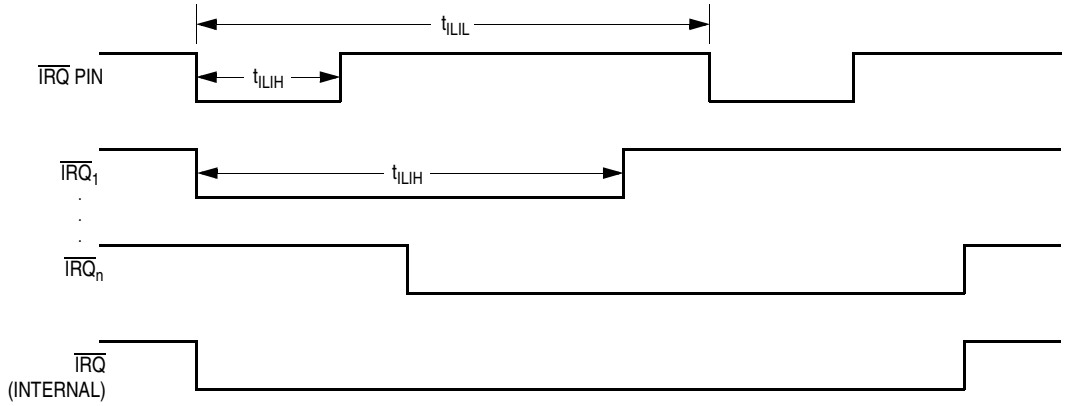
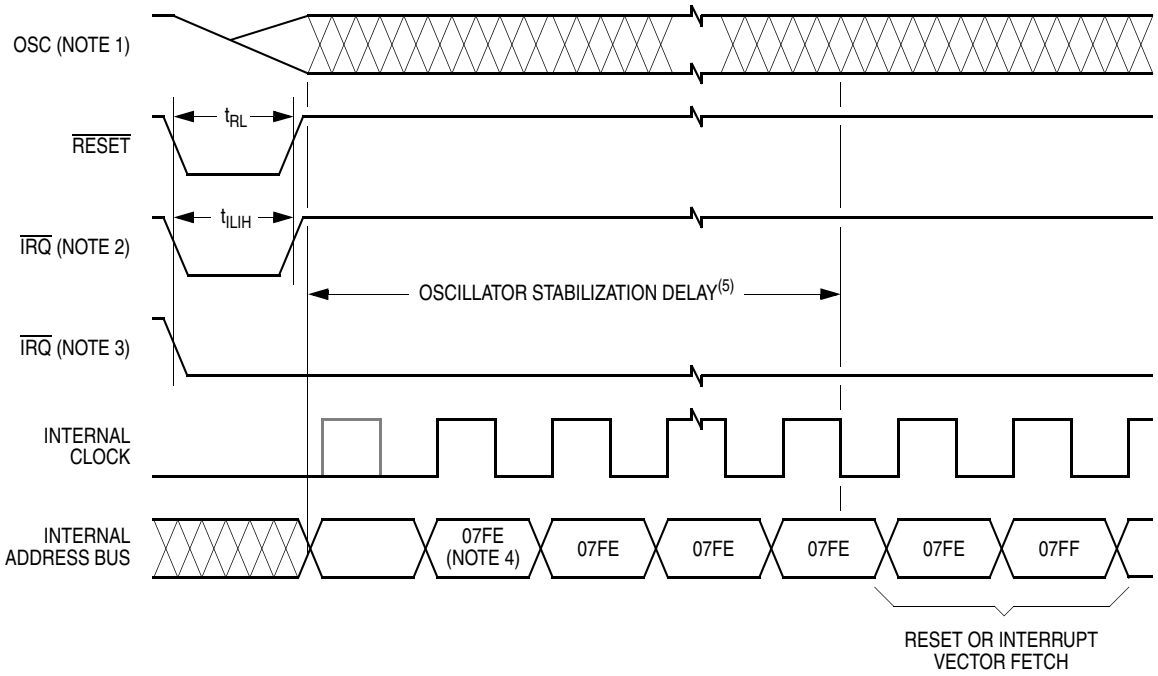


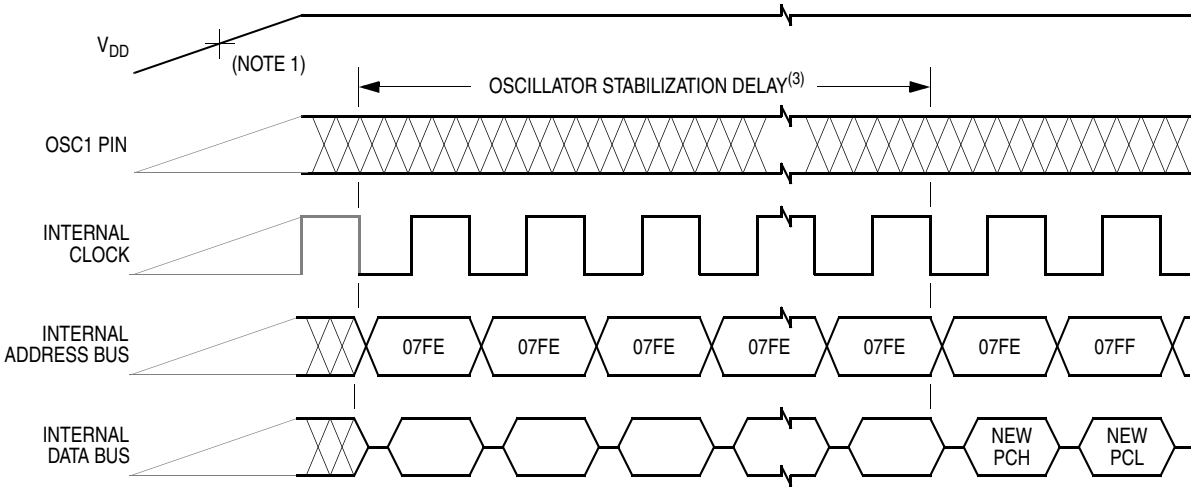
Figure 10-7. External Interrupt Timing



Notes:

1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example
5. 4064 t_{cyc} or 128 t_{cyc}, depending on the state of SOSCD bit in MOR

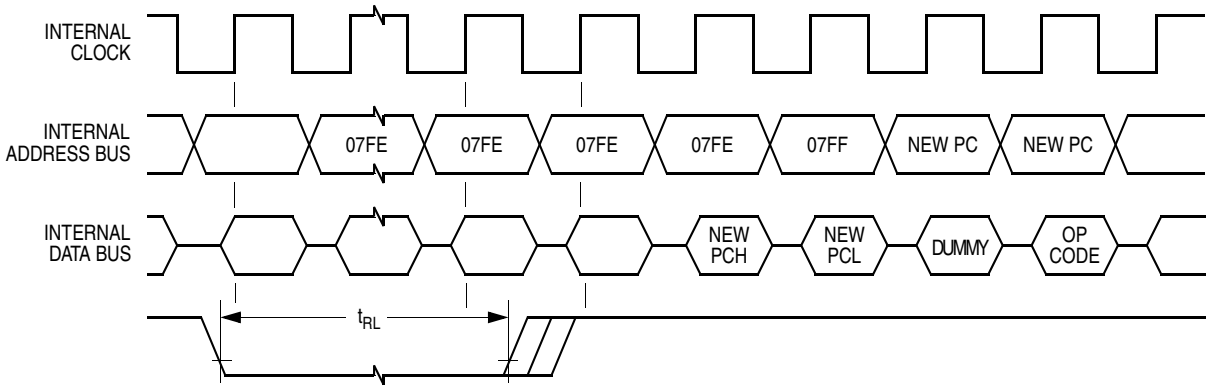
Figure 10-8. Stop Mode Recovery Timing



NOTES:

1. Power-on reset threshold is typically between 1 V and 2 V.
2. Internal clock, internal address bus, and internal data bus are not available externally.
3. 4064 t_{cyc} or 128 t_{cyc} depending on the state of SOSCD bit in MOR

Figure 10-9. Power-On Reset Timing



NOTES:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 10-10. External Reset Timing

Chapter 11
Ordering Information and Mechanical Specifications

11.1 Introduction

The MC68HC705J1A, the RC oscillator, and low-speed option devices described in Appendix A MC68HRC705KJ1 and Appendix B MC68HLC705KJ1 are available in these packages:

- 648 — Plastic dual in-line package (PDIP)
- 751G — Small outline integrated circuit (SOIC)
- 620A — Ceramic DIP (Cerdip) (windowed)

This section contains ordering information and mechanical specifications for the available package types.

11.2 MCU Order Numbers

Table 11-1 lists the MC order numbers.

Table 11-1. Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	648	16	–40 to +85°C	MC68HC705KJ1C(2)
SOIC	751G	16	–40 to +85°C	MC68HC705KJ1CDW(3)
Cerdip	620A	16	–40 to +85°C	MC68HC705KJ1CS(4)

1. Refer to Appendix A MC68HRC705KJ1 and Appendix B MC68HLC705KJ1 for ordering information on optional low-speed and resistor-capacitor oscillator devices.
2. C = extended temperature range
3. DW = small outline integrated circuit (SOIC)
4. S = ceramic dual in-line package (Cerdip)

A.4 RC Oscillator Connections (No External Resistor)

For maximum cost reduction, the RC oscillator mask connections shown in Figure A-3 allow the on-chip oscillator to be driven with **no** external components. This can be accomplished by programming the oscillator internal resistor (OSCRES) bit in the mask option register to a logic 1. When programming the OSCRES bit for the MC68HRC705KJ1, an internal resistor is selected which yields typical internal oscillator frequencies as shown in Figure A-4. The internal resistance for this device is different than the resistance of the selectable internal resistor on the MC68HC705KJ1 and the MC68HRC705KJ1 devices.

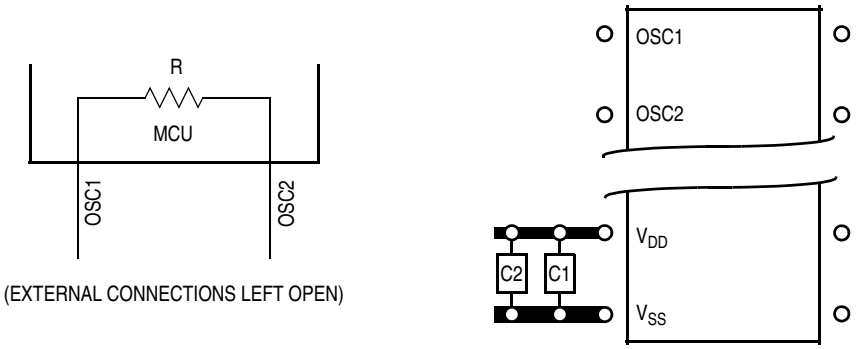


Figure A-3. RC Oscillator Connections (No External Resistor)