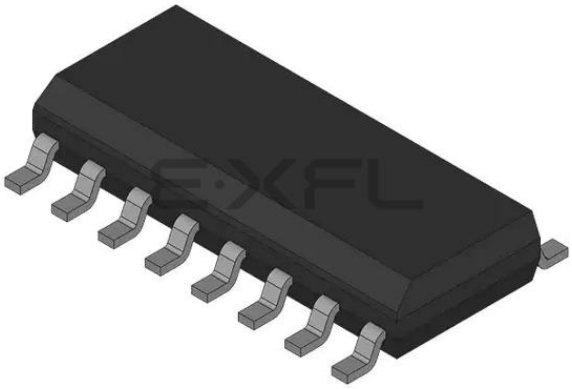

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	10
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchlc705kj1cdwe

Chapter 1
Introduction

1.1 Features

Features on the MC68HC705KJ1 include:

- Robust noise immunity
- 4.0-MHz internal operating frequency at 5.0 V
- 1240 Bytes of EPROM/OTPROM (electrically programmable read-only memory/one-time programmable read-only memory), including eight bytes for user vectors
- 64 bytes of user RAM
- Peripheral modules:
  - 15-stage multifunction timer
  - Computer operating properly (COP) watchdog
- 10 bidirectional input/output (I/O) lines, including:
  - 10-mA sink capability on all I/O pins
  - Software programmable pulldowns on all I/O pins
  - Keyboard scan with selectable interrupt on four I/O pins
  - 5.5-mA source capability on six I/O pins
- Selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with connections for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator (MC68HRC705KJ1) with or without external resistor
  - External clock
  - Low-speed (32-kHz) crystal (MC68HLC705KJ1)
- Memory-mapped I/O registers
- Fully static operation with no minimum clock speed
- Power-saving stop, halt, wait, and data-retention modes
- External interrupt mask bit and acknowledge bit
- Illegal address reset
- Internal steering diode and pullup resistor from $\overline{\text{RESET}}$ pin to V_{DD}
- Selectable EPROM security[1]
- Selectable oscillator bias resistor

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

2.7.2 EPROM Programming Register

The EPROM programming register (EPROG) contains the control bits for programming the EPROM/OTPROM.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	ELAT	MPGM	EPGM
Write:		R	R	R	R			
Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 2-3. EPROM Programming Register (EPROG)

ELAT — EPROM Bus Latch Bit

This read/write bit latches the address and data buses for EPROM/OTPROM programming. Clearing the ELAT bit automatically clears the EPGM bit. EPROM/OTPROM data cannot be read while the ELAT bit is set. Reset clears the ELAT bit.

1 = Address and data buses configured for EPROM/OTPROM programming the EPROM
0 = Address and data buses configured for normal operation

MPGM — MOR Programming Bit

This read/write bit applies programming power from the $\overline{IRQ}/V_{PP}$ pin to the mask option register. Reset clears MPGM.

1 = Programming voltage applied to MOR
0 = Programming voltage not applied to MOR

EPGM — EPROM Programming Bit

This read/write bit applies the voltage from the $\overline{IRQ}/V_{PP}$ pin to the EPROM. To write the EPGM bit, the ELAT bit must be set already. Reset clears EPGM.

1 = Programming voltage ($\overline{IRQ}/V_{PP}$ pin) applied to EPROM
0 = Programming voltage ($\overline{IRQ}/V_{PP}$ pin) not applied to EPROM

NOTE

Writing logic 1s to both the ELAT and EPGM bits with a single instruction sets ELAT and clears EPGM. ELAT must be set first by a separate instruction.

Bits [7:3] — Reserved

Take the following steps to program a byte of EPROM/OTPROM:

1. Apply the programming voltage, V_{PP}, to the $\overline{IRQ}/V_{PP}$ pin.
2. Set the ELAT bit.
3. Write to any EPROM/OTPROM address.
4. Set the EPGM bit and wait for a time, t_{EPGM}.
5. Clear the ELAT bit.

2.7.3 EPROM Erasing

The erased state of an EPROM bit is logic 0. Erase the EPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wavelength of 2537 angstroms. Position the ultraviolet light source one inch from the EPROM. Do not use a shortwave filter.

SWAIT — Stop-to-Wait Conversion Bit

The SWAIT bit enables halt mode. When the SWAIT bit is set, the CPU interprets the STOP instruction as a WAIT instruction, and the MCU enters halt mode. Halt mode is the same as wait mode, except that an oscillator stabilization delay of 1 to 4064 t_{cyc} occurs after exiting halt mode.

1 = Halt mode enabled
0 = Halt mode not enabled

SWPDI — Software Pulldown Inhibit Bit

The SWPDI bit inhibits software control of the I/O port pulldown devices. The SWPDI bit overrides the pulldown inhibit bits in the port pulldown inhibit registers.

1 = Software pulldown control inhibited
0 = Software pulldown control not inhibited

PIRQ — Port A External Interrupt Bit

The PIRQ bit enables the PA0–PA3 pins to function as external interrupt pins.

1 = PA0–PA3 enabled as external interrupt pins
0 = PA0–PA3 not enabled as external interrupt pins

LEVEL —External Interrupt Sensitivity Bit

The LEVEL bit controls external interrupt triggering sensitivity.

1 = External interrupts triggered by active edges and active levels
0 = External interrupts triggered only by active edges

COPEN — COP Enable Bit

The COPEN bit enables the COP watchdog.

1 = COP watchdog enabled
0 = COP watchdog disabled

2.9 EPROM Programming Characteristics

Table 2-1. EPROM Programming Characteristics(1)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming Current $\overline{IRQ}/V_{PP}$	I_{PP}	—¦	3.0	10.0	mA
Programming Time Per Array Byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C

4.6.2.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE

Do not use read-modify-write instructions on registers with write-only bits.

Table 4-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR(1)
Bit Set	BSET(1)
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST(2)

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

4.6.2.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the

4.6.2.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 4-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

NOTE

Do not use bit manipulation instructions on registers with write-only bits.

4.6.2.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 4-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

Table 4-6. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff 	5 6 7 6 5

Table 4-6. Instruction Set Summary (Sheet 4 of 6)

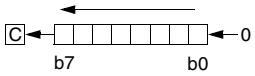
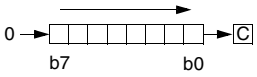
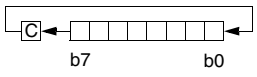
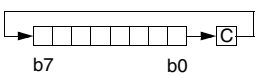
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		1 1
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2

Table 4-6. Instruction Set Summary (Sheet 6 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	0	—	—	—	INH	8F		2

A	Accumulator	*opr*	Operand (one or two bytes)
C	Carry/borrow flag	PC	Program counter
CCR	Condition code register	PCH	Program counter high byte
dd	Direct address of operand	PCL	Program counter low byte
dd rr	Direct address of operand and relative offset of branch instruction	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	rr	Relative program counter offset byte
EXT	Extended addressing mode	SP	Stack pointer
ff	Offset byte in indexed, 8-bit offset addressing	X	Index register
H	Half-carry flag	Z	Zero flag
hh ll	High and low bytes of operand address in extended addressing	#	Immediate value
I	Interrupt mask	∧	Logical AND
ii	Immediate operand byte	∨	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX2	Indexed, 16-bit offset addressing mode	?	If
M	Memory location	:	Concatenated with
N	Negative flag	↕	Set or cleared
n	Any bit	—	Not affected

4.7 Opcode Map

See Table 4-7.

Chapter 7
Parallel I/O Ports (PORTS)

7.1 Introduction

Ten bidirectional pins form one 8-bit input/output (I/O) port and one 2-bit I/O port. All the bidirectional port pins are programmable as inputs or outputs.

NOTE

Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.

Addr.	Register Name:		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 64.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 66.	Read:	0	0	See Note		PB3	PB2	See Note	
		Write:								
		Reset:	Unaffected by reset							
$0004	Data Direction Register A (DDRA) See page 64.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 67.	Read:	0	0	See Note		DDRB3	DDRB2	See Note	
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0010	Port A Pulldown Register (PDRA) See page 65.	Read:								
		Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
		Reset:	0	0	0	0	0	0	0	0
$0011	Port B Pulldown Register (PDRB) See page 68.	Read:								
		Write:			See Note		PDIB3	PDIB2	See Note	
		Reset:			0	0	0	0	0	0

= Unimplemented

Note:
PB5, PB4, PB1, and PB0 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

Figure 7-1. Parallel I/O Port Register Summary

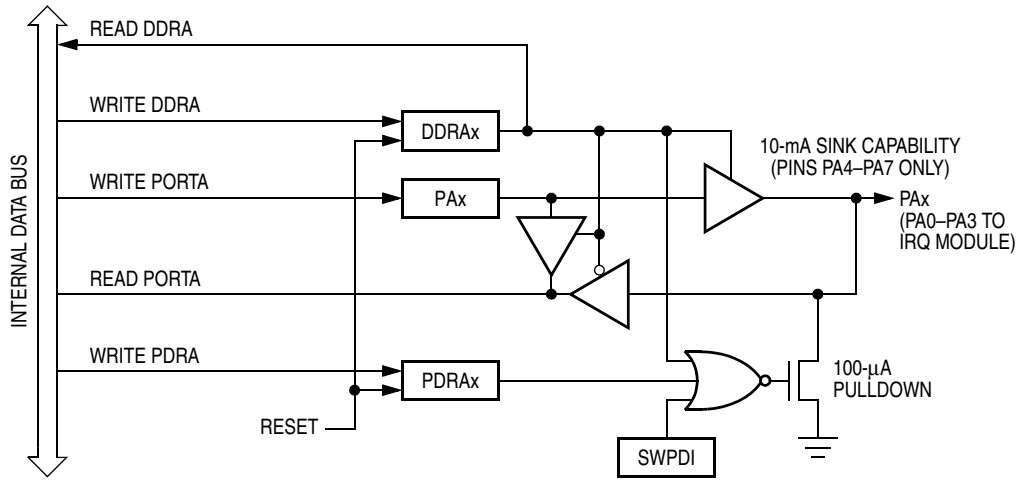


Figure 7-4. Port A I/O Circuitry

Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

When bit DDRAx is a logic 1, reading address $0000 reads the PAx data latch. When bit DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 7-1 summarizes the operation of the port A pins.

Table 7-1. Port A Pin Operation

Data Direction Bit	I/O Pin Mode	Accesses to Data Bit	
		Read	Write
0	Input, high-impedance	Pin	Latch(1)
1	Output	Latch	Latch

1. Writing affects the data register but does not affect input.

7.2.3 Pulldown Register A

Pulldown register A inhibits the pulldown devices on port A pins programmed as inputs.

NOTE

If the SWPDI bit in the mask option register is programmed to logic 1, reset initializes all port A pins as inputs with disabled pulldown devices.

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-5. Pulldown Register A (PDRA)

PDIA[7:0] — Pulldown Inhibit A Bits

PDIA[7:0] disable the port A pulldown devices. Reset clears PDIA[7:0].

1 = Corresponding port A pulldown device disabled

0 = Corresponding port A pulldown device not disabled

Table 7-2. Port B Pin Operation

Data Direction Bit	I/O Pin Mode	Accesses to Data Bit	
		Read	Write
0	Input, high-impedance	Pin	Latch(1)
1	Output	Latch	Latch

1. Writing affects the data register, but does not affect input.

7.3.3 Pulldown Register B

Pulldown register B inhibits the pulldown devices on port B pins programmed as inputs.

NOTE

If the SWPDI bit in the mask option register is programmed to logic 1, reset initializes all port B pins as inputs with disabled pulldown devices.

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:			See Note		PDIB3	PDIB2	See Note	
Reset:			0	0	0	0	0	0

= Unimplemented

Note:
These pulldown devices are permanently enabled when PB5, PB4, PB1 and PB0 are configured as inputs.

Figure 7-9. Pulldown Register B (PDRB)

PDIB[3:2] — Pulldown Inhibit B Bits

PDIB[3:2] disable the port B pulldown devices. Reset clears PDIB[3:2].

1 = Corresponding port B pulldown device disabled
0 = Corresponding port B pulldown device not disabled

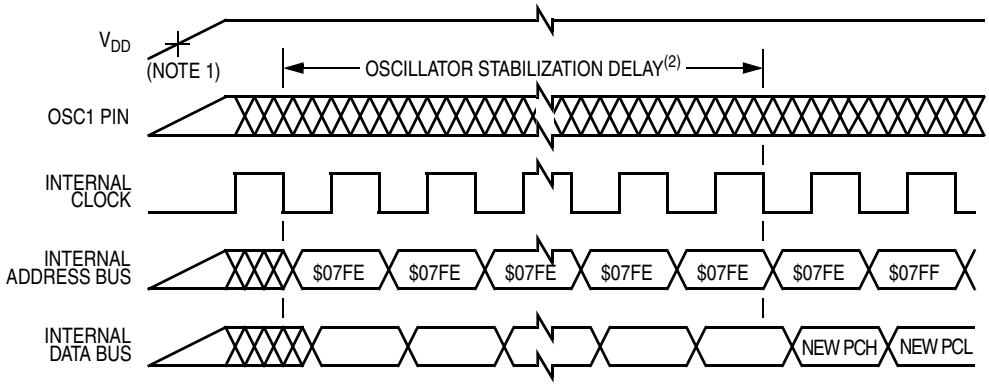
8.2.1 Power-On Reset

A positive transition on the V_{DD} pin generates a power-on reset.

NOTE

The power-on reset is strictly for power-up conditions and cannot be used to detect drops in power supply voltage.

A 4064-t_{cyc} (internal clock cycle) delay after the oscillator becomes active allows the clock generator to stabilize. If any reset source is active at the end of this delay, the MCU remains in the reset condition until all reset sources are inactive.

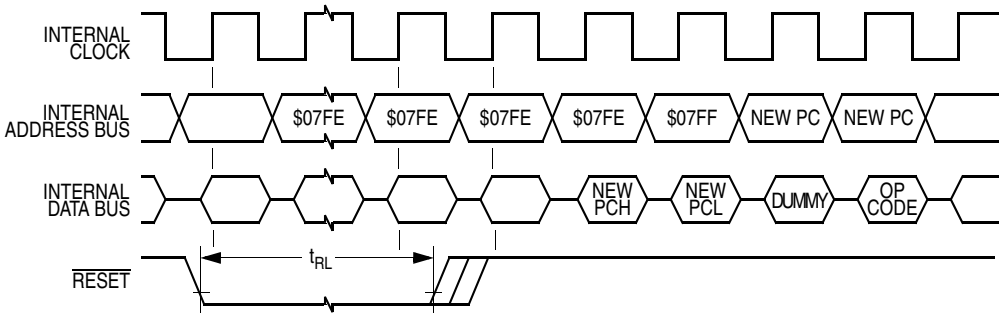


Notes:
1. Power-on reset threshold is typically between 1 V and 2 V.
2. 4064 cycles or 128 cycles, depending on state of SOSCD bit in MOR
3. Internal clock, internal address bus, and internal data bus are not available externally.

Figure 8-2. Power-On Reset Timing

8.2.2 External Reset

A logic 0 applied to the $\overline{\text{RESET}}$ pin for 1 1/2 t_{cyc} generates an external reset. A Schmitt trigger senses the logic level at the $\overline{\text{RESET}}$ pin.



Notes:
1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 8-3. External Reset Timing

Table 8-1. External Reset Timing

Characteristic	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{cyc}

8.3.3 Timer Interrupts

The timer can generate the following interrupt requests:

- Real time
- Timer overflow

Setting the I bit in the condition code register disables timer interrupts.

8.3.3.1 Real-Time Interrupt

A real-time interrupt occurs if the real-time interrupt flag, RTIF, becomes set while the real-time interrupt enable bit, RTIE, is also set. RTIF and RTIE are in the timer status and control register.

8.3.3.2 Timer Overflow Interrupt

A timer overflow interrupt request occurs if the timer overflow flag, TOF, becomes set while the timer overflow interrupt enable bit, TOIE, is also set. TOF and TOIE are in the timer status and control register.

8.3.4 Interrupt Processing

The CPU takes the following actions to begin servicing an interrupt:

- Stores the CPU registers on the stack in the order shown in Figure 8-6
- Sets the I bit in the condition code register to prevent further interrupts
- Loads the program counter with the contents of the appropriate interrupt vector locations:
  - $07FC and $07FD (software interrupt vector)
  - $07FA and $07FB (external interrupt vector)
  - $07F8 and $07F9 (timer interrupt vector)

The return-from-interrupt (RTI) instruction causes the CPU to recover the CPU registers from the stack as shown in Figure 8-6.

Chapter 10
Electrical Specifications

10.1 Maximum Ratings

Maximum ratings are the extreme limits to which the microcontroller unit (MCU) can be exposed without permanently damaging it.

NOTE

This device is not guaranteed to operate properly at the maximum ratings. For guaranteed operating conditions, refer to 10.5 5.0-V DC Electrical Characteristics and 10.6 3.3-V DC Electrical Characteristics

Table 10-1. Maximum Ratings(1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	25	mA
Input Voltage	V_{In}	V_{SS} – 0.3 to V_{DD} + 0.3	V
$\overline{IRQ}$/V_{PP} Pin	V_{PP}	V_{SS} – 0.3 to 2 x V_{DD} + 0.3	V
Storage Temperature Range	T_{STG}	–65 to +150	°C

1. Voltages are referenced to V_{SS}.

10.2 Operating Temperature Range

Package Type	Symbol	Value (T_L to T_H)	Unit
MC68HC705KJ1C(1)P(2), CDW(3), CS(4)	T_A	–40 to +85	°C

1. C = extended temperature range
2. P = plastic dual in-line package (PDIP)
3. DW = small outline integrated circuit (SOIC)
4. S = ceramic DIP (Cerdip)

10.3 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance MC68HC705KJ1P(1) MC68HC705KJ1DW(2) MC68HC705KJ1S(3)	θ_{JA}	60	°C/W

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (Cerdip)

10.6 3.3-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –0.8 mA) PA4–PA7 (I_{Load} = –1.5 mA) PA0–PA3, PB2–PB3	V_{OH}	V_{DD} –0.3 V_{DD} –0.3	— —	— —	V
Output low voltage (I_{Load} = 5.0 mA) PA4–PA7 (I_{Load} = 3.5 mA) PA0–PA3, PB2–PB3	V_{OL}	— —	— —	0.5 0.5	V
Input high voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (f_{OP} = 1.0 MHz; f_{OSC} = 2.0 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 1.2 0.3 0.1	 2.5 0.8 5.0	 mA mA µA
Supply current (f_{OP} = 2.1 MHz; f_{OSC} = 4.2 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 1.4 0.3 0.1	 3.0 1.0 5.0	 mA mA µA
I/O ports hi-z leakage current PA0–PA7, PB2–PB3 (without individual pulldown activated)	I_{IL}	—	0.1	±1	µA
Input pulldown current PA0–PA7, PB2–PB3 (with individual pulldown activated)	I_{IL}	12	30	100	µA
Input pullup current $\overline{RESET}$	I_{IL}	–10	–25	–45	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.1	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{OSC}	1.0	2.0	3.0	MΩ

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{OSC} value selected for RC oscillator versions of this device is unspecified.

10.9 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{IRQ}/V_{PP}$	I_{PP}	—¡	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

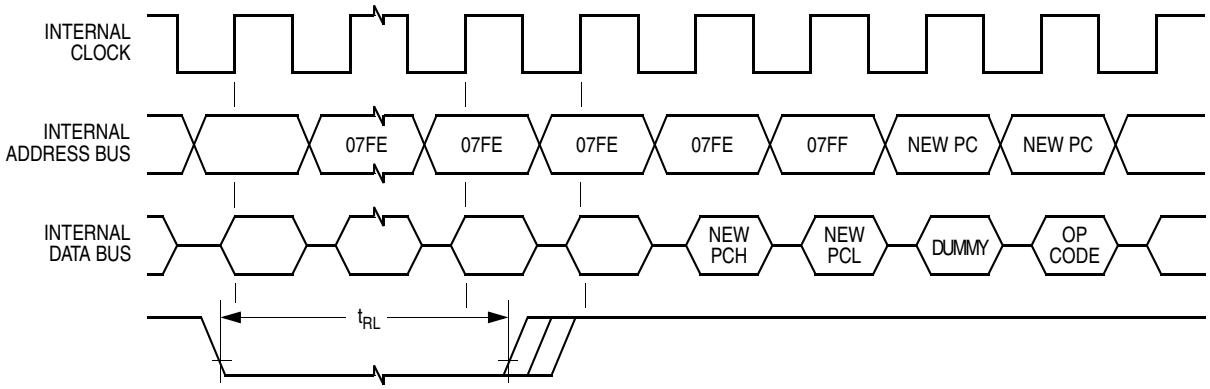
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.

10.10 Control Timing

Table 10-2. Control Timing (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	 — dc	 8.0 8.0	MHz
Internal operating frequency (f_{OSC} ÷ 2) Crystal oscillator External clock	f_{OP}	 — dc	 4.0 4.0	MHz
Cycle time (1 ÷ f_{OP})	t_{cyc}	250	—	ns
$\overline{RESET}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 Interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	100	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.



NOTES:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 10-10. External Reset Timing

A.4 RC Oscillator Connections (No External Resistor)

For maximum cost reduction, the RC oscillator mask connections shown in Figure A-3 allow the on-chip oscillator to be driven with **no** external components. This can be accomplished by programming the oscillator internal resistor (OSCRES) bit in the mask option register to a logic 1. When programming the OSCRES bit for the MC68HRC705KJ1, an internal resistor is selected which yields typical internal oscillator frequencies as shown in Figure A-4. The internal resistance for this device is different than the resistance of the selectable internal resistor on the MC68HC705KJ1 and the MC68HRC705KJ1 devices.

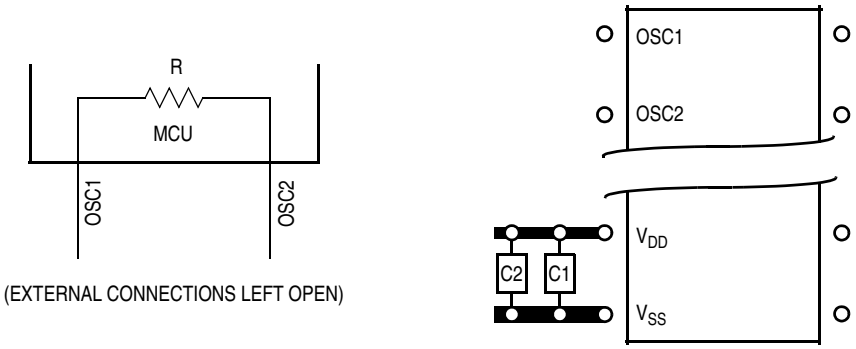


Figure A-3. RC Oscillator Connections (No External Resistor)

A.5 Typical Internal Operating Frequency Versus Temperature (No External Resistor)

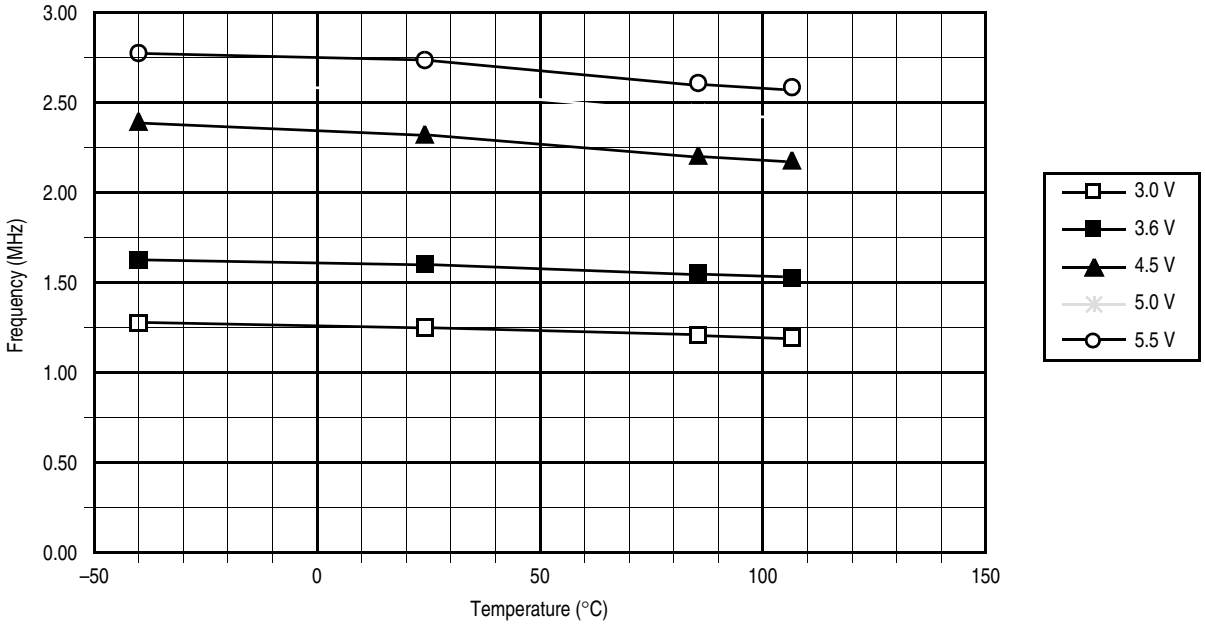


Figure A-4. Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)

NOTE

Due to process variations, operating voltages, and temperature requirements, the internal resistance and tolerance are unspecified. Typically for a given voltage and temperature, the frequency should not vary more than ± 500 kHz. However, this data is not guaranteed. It is the user's responsibility to ensure that the resulting internal operating frequency meets user's requirements.

A.6 Package Types and Order Numbers

Table A-1. MC68HRC705KJ1 (RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	648	16	–40 to +85°C	MC68HRC705KJ1C(2)P(3)
SOIC	751G	16	–40 to +85°C	MC68HRC705KJ1CDW(4)
Cerdip	620A	16	–40 to +85°C	MC68HRC705KJ1CS(5)

1. Refer to Chapter 11 Ordering Information and Mechanical Specifications for standard part ordering information.
2. C = extended temperature range
3. P = plastic dual in-line package (PDIP)
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (Cerdip)