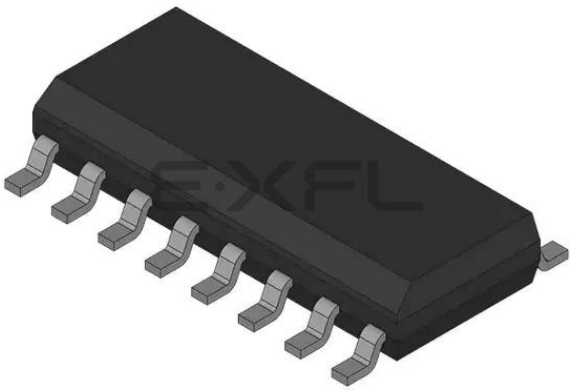

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	10
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchrc705kj1cdwe

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
April, 2002	3.0	Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places	17
		Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places	17
		Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places	18
		Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option — changed PA7 designator to OSC1 in two places	18
		Figure 1-8. External Clock Connections — changed PA7 designator to OSC1 in two places	19
		Figure B-1. Crystal Connections — added OSC2 designation	105
		Table B-3. MC68HLC705KJ1 (Low Frequency) Order Numbers — Corrected table title	106
May, 2003	4.0	Reformatted to new publications standards.	Throughout
		Figure A-2. Typical Internal Operating Frequency for Various VDD at 25°C — RC Oscillator Option Only — replaced graph	102
July, 2005	4.1	Updated to meet Freescale identity guidelines.	Throughout

Chapter 6
Low-Power Modes

Chapter 7
Parallel I/O Ports (PORTS)

Chapter 8
Resets and Interrupts

1.3 Programmable Options

The options in Table 1-1 are programmable in the mask option register.

Table 1-1. Programmable Options

Feature	Option
COP watchdog timer	Enabled or disabled
External interrupt triggering	Edge-sensitive only or edge- and level-sensitive
Port A $\overline{IRQ}$ pin interrupts	Enabled or disabled
Port pulldown resistors	Enabled or disabled
STOP instruction mode	Stop mode or halt mode
Crystal oscillator internal resistor	Enabled or disabled
EPROM security	Enabled or disabled
Short oscillator delay counter	Enabled or disabled

1.4 Pin Functions

Pin assignments are shown in Figure 1-2 with the functions described in the following subsections.

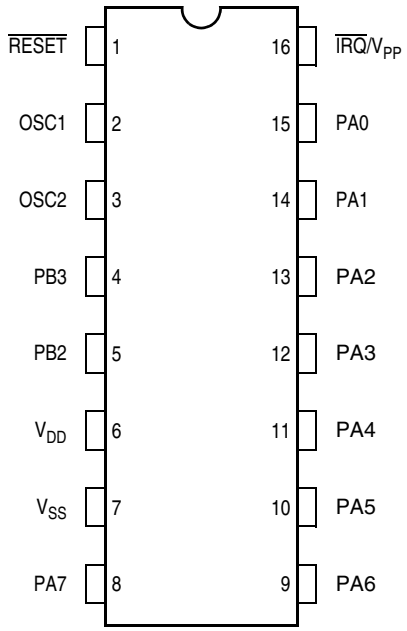


Figure 1-2. Pin Assignments

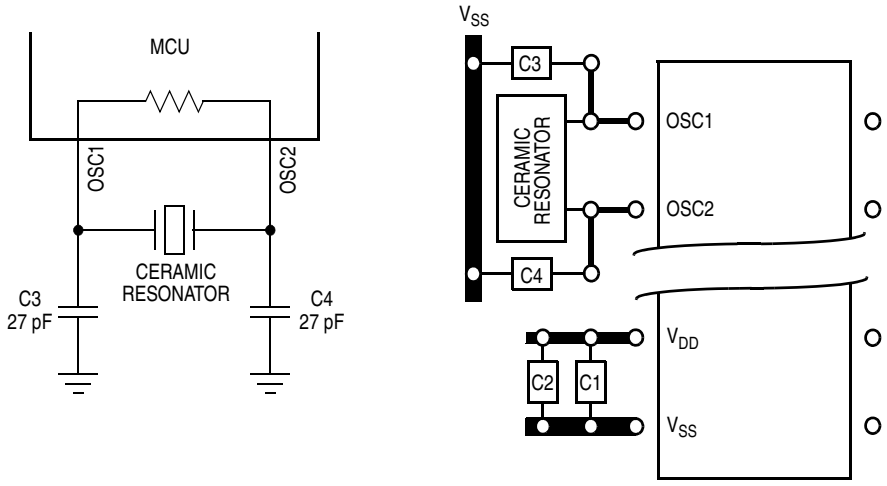


Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option

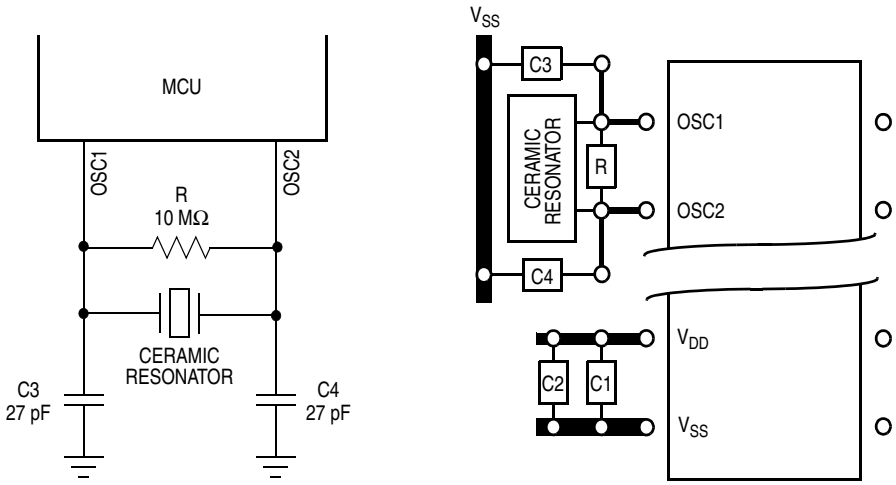


Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option

1.4.2.3 RC Oscillator

Refer to Appendix A MC68HRC705KJ1.

1.4.2.4 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in Figure 1-8. This configuration is possible regardless of whether the crystal/ceramic resonator or the RC oscillator is enabled.

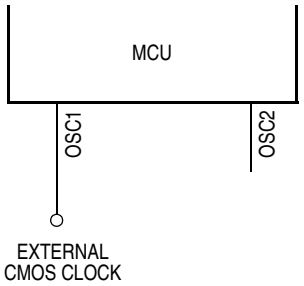


Figure 1-8. External Clock Connections

1.4.3 $\overline{\text{RESET}}$

Applying a logic 0 to the $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. An internal reset also pulls the $\overline{\text{RESET}}$ pin low. An internal resistor to V_{DD} pulls the $\overline{\text{RESET}}$ pin high. A steering diode between the $\overline{\text{RESET}}$ and V_{DD} pins discharges any $\overline{\text{RESET}}$ pin voltage when power is removed from the MCU. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. Refer to Chapter 8 Resets and Interrupts for more information.

1.4.4 $\overline{\text{IRQ}}/V_{PP}$

The external interrupt/programming voltage pin ($\overline{\text{IRQ}}/V_{PP}$) drives the asynchronous IRQ interrupt function of the CPU. Additionally, it is used to program the user EPROM and mask option register. (See Chapter 2 Memory and Chapter 5 External Interrupt Module (IRQ).)

The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If level-sensitive triggering is selected, the $\overline{\text{IRQ}}/V_{PP}$ input requires an external resistor to V_{DD} for wired-OR operation. If the $\overline{\text{IRQ}}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply.

The $\overline{\text{IRQ}}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin should not exceed V_{DD} except when the pin is being used for programming the EPROM.

NOTE

The mask option register can enable the PA0–PA3 pins to function as external interrupt pins.

1.4.5 PA0–PA7

These eight input/output (I/O) lines comprise port A, a general-purpose bidirectional I/O port. (See Chapter 5 External Interrupt Module (IRQ) for information on PA0–PA3 external interrupts.)

1.4.6 PB2 and PB3

These two I/O lines comprise port B, a general-purpose bidirectional I/O port.

Chapter 2
Memory

2.1 Introduction

This section provides:

- Memory map (Figure 2-1)
- Summary of the input/output registers (Figure 2-2)
- Description of:
  - Random-access memory (RAM)
  - EPROM/OTPROM (electrically programmable read-only memory/one-time programmable read-only memory)
  - Mask option register

Memory features include:

- 1232 Bytes of User EPROM, Plus Eight Bytes for User Vectors
- 64 Bytes of User RAM

2.2 Unimplemented Memory Locations

Accessing an unimplemented location can have unpredictable effects on MCU operation. In Figure 2-2 and in register figures in this document, unimplemented locations are shaded.

2.3 Reserved Memory Locations

Accessing a reserved location can have unpredictable effects on MCU operation. In Figure 2-2 and in register figures in this document, reserved locations are marked with the word Reserved or with the letter R.

2.4 Memory Map

See Figure 2-1.

2.6 RAM

The 64 addresses from $00C0 to $00FF serve as both the user RAM and the stack RAM. Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements when the CPU stores a byte on the stack and increments when the CPU retrieves a byte from the stack.

NOTE

Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.

2.7 EPROM/OTPROM

An MCU with a quartz window has 1240 bytes of erasable, programmable ROM (EPROM). The quartz window allows EPROM erasure with ultraviolet light.

NOTE

Keep the quartz window covered with an opaque material except when erasing the MCU. Ambient light can affect MCU operation.

In an MCU without the quartz window, the EPROM cannot be erased and serves as 1240 bytes of one-time programmable ROM (OTPROM).

The following addresses are user EPROM/OTPROM locations:

- $0300–$07CF
- $07F8–$07FF, used for user-defined interrupt and reset vectors

The COP register (COPR) is an EPROM/OTPROM location at address $07F0.

The mask option register (MOR) is an EPROM/OTPROM location at address $07F1.

2.7.1 EPROM/OTPROM Programming

The two ways to program the EPROM/OTPROM are:

- Manipulating the control bits in the EPROM programming register to program the EPROM/OTPROM on a byte-by-byte basis
- Programming the EPROM/OTPROM with the M68HC705J In-Circuit Simulator (M68HC705JICS) available from Freescale

2.7.2 EPROM Programming Register

The EPROM programming register (EPROG) contains the control bits for programming the EPROM/OTPROM.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	ELAT	MPGM	EPGM
Write:		R	R	R	R			
Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 2-3. EPROM Programming Register (EPROG)

ELAT — EPROM Bus Latch Bit

This read/write bit latches the address and data buses for EPROM/OTPROM programming. Clearing the ELAT bit automatically clears the EPGM bit. EPROM/OTPROM data cannot be read while the ELAT bit is set. Reset clears the ELAT bit.

1 = Address and data buses configured for EPROM/OTPROM programming the EPROM
0 = Address and data buses configured for normal operation

MPGM — MOR Programming Bit

This read/write bit applies programming power from the $\overline{IRQ}/V_{PP}$ pin to the mask option register. Reset clears MPGM.

1 = Programming voltage applied to MOR
0 = Programming voltage not applied to MOR

EPGM — EPROM Programming Bit

This read/write bit applies the voltage from the $\overline{IRQ}/V_{PP}$ pin to the EPROM. To write the EPGM bit, the ELAT bit must be set already. Reset clears EPGM.

1 = Programming voltage ($\overline{IRQ}/V_{PP}$ pin) applied to EPROM
0 = Programming voltage ($\overline{IRQ}/V_{PP}$ pin) not applied to EPROM

NOTE

Writing logic 1s to both the ELAT and EPGM bits with a single instruction sets ELAT and clears EPGM. ELAT must be set first by a separate instruction.

Bits [7:3] — Reserved

Take the following steps to program a byte of EPROM/OTPROM:

1. Apply the programming voltage, V_{PP}, to the $\overline{IRQ}/V_{PP}$ pin.
2. Set the ELAT bit.
3. Write to any EPROM/OTPROM address.
4. Set the EPGM bit and wait for a time, t_{EPGM}.
5. Clear the ELAT bit.

2.7.3 EPROM Erasing

The erased state of an EPROM bit is logic 0. Erase the EPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wavelength of 2537 angstroms. Position the ultraviolet light source one inch from the EPROM. Do not use a shortwave filter.

SWAIT — Stop-to-Wait Conversion Bit

The SWAIT bit enables halt mode. When the SWAIT bit is set, the CPU interprets the STOP instruction as a WAIT instruction, and the MCU enters halt mode. Halt mode is the same as wait mode, except that an oscillator stabilization delay of 1 to 4064 t_{cyc} occurs after exiting halt mode.

1 = Halt mode enabled
0 = Halt mode not enabled

SWPDI — Software Pulldown Inhibit Bit

The SWPDI bit inhibits software control of the I/O port pulldown devices. The SWPDI bit overrides the pulldown inhibit bits in the port pulldown inhibit registers.

1 = Software pulldown control inhibited
0 = Software pulldown control not inhibited

PIRQ — Port A External Interrupt Bit

The PIRQ bit enables the PA0–PA3 pins to function as external interrupt pins.

1 = PA0–PA3 enabled as external interrupt pins
0 = PA0–PA3 not enabled as external interrupt pins

LEVEL —External Interrupt Sensitivity Bit

The LEVEL bit controls external interrupt triggering sensitivity.

1 = External interrupts triggered by active edges and active levels
0 = External interrupts triggered only by active edges

COPEN — COP Enable Bit

The COPEN bit enables the COP watchdog.

1 = COP watchdog enabled
0 = COP watchdog disabled

2.9 EPROM Programming Characteristics

Table 2-1. EPROM Programming Characteristics(1)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming Current $\overline{IRQ}/V_{PP}$	I_{PP}	—¦	3.0	10.0	mA
Programming Time Per Array Byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C

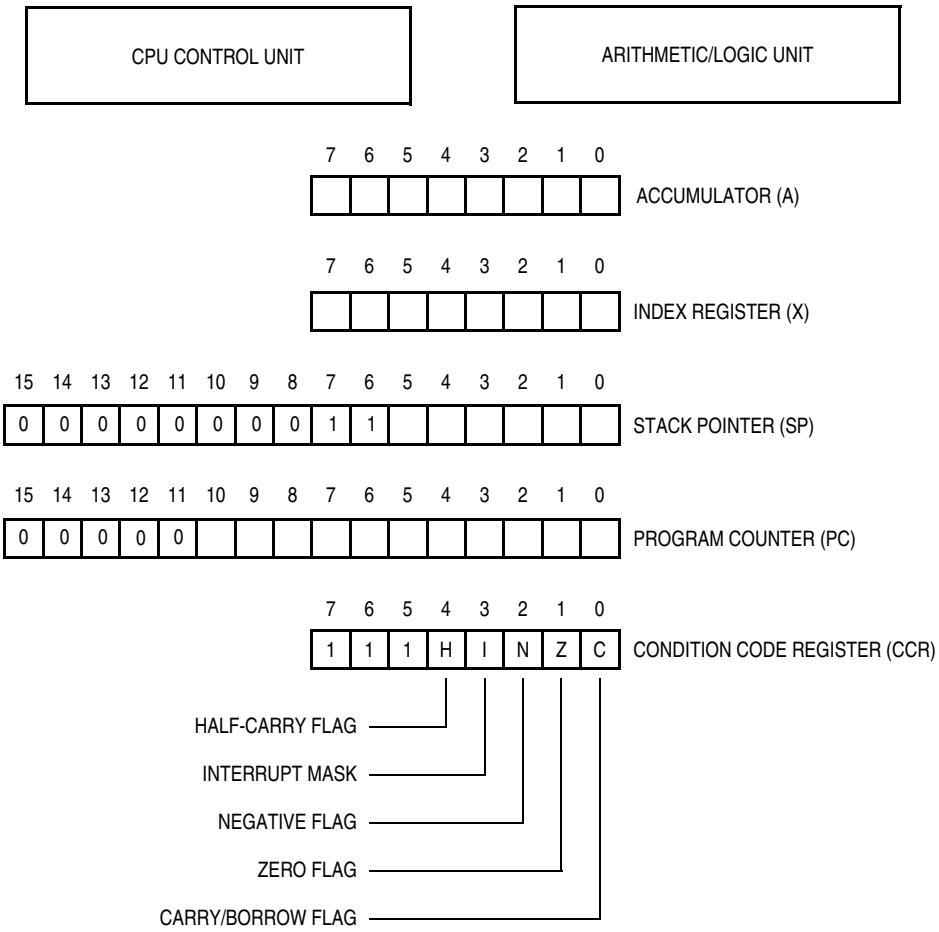


Figure 4-1. Programming Model

Table 4-7. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended

REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

LSB of Opcode in Hexadecimal

MSB / LSB	0
0	5 BRSET0 3 DIR

MSB of Opcode in Hexadecimal

Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

6.3.3.1 STOP

The STOP instruction:

- Clears the COP watchdog counter
- Disables the COP watchdog clock

NOTE

To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.

After exit from stop mode by external interrupt, the COP watchdog counter immediately begins counting from $0000 and continues counting throughout the oscillator stabilization delay.

NOTE

Immediately after exiting stop mode by external interrupt, service the COP to ensure a full COP timeout period.

After exit from stop mode by reset:

- The COP watchdog counter immediately begins counting from $0000.
- The COP watchdog counter is cleared at the end of the oscillator stabilization delay and begins counting from $0000 again.

6.3.3.2 WAIT

The WAIT instruction has no effect on the COP watchdog.

NOTE

To prevent a COP timeout during wait mode, exit wait mode periodically to service the COP.

6.3.4 Timer

Effects of STOP and WAIT on the timer are discussed here.

6.3.4.1 STOP

The STOP instruction:

- Clears the RTIE, TOFE, RTIF, and TOF bits in the timer status and control register, disabling timer interrupt requests and removing any pending timer interrupt requests
- Disables the clock to the timer

After exiting stop mode by external interrupt, the timer immediately resumes counting from the last value before the STOP instruction and continues counting throughout the oscillator stabilization delay.

After exiting stop mode by reset and after the oscillator stabilization delay, the timer resumes operation from its reset state.

6.3.4.2 WAIT

The WAIT instruction has no effect on the timer.

6.3.5 EPROM/OTPROM

Effects of STOP and WAIT on the EPROM/OTPROM are discussed here.

7.2.4 Port LED Drive Capability

All outputs can drive light-emitting diodes (LEDs). These pins can sink approximately 10 mA of current to V_{SS}.

7.2.5 Port A I/O Pin Interrupts

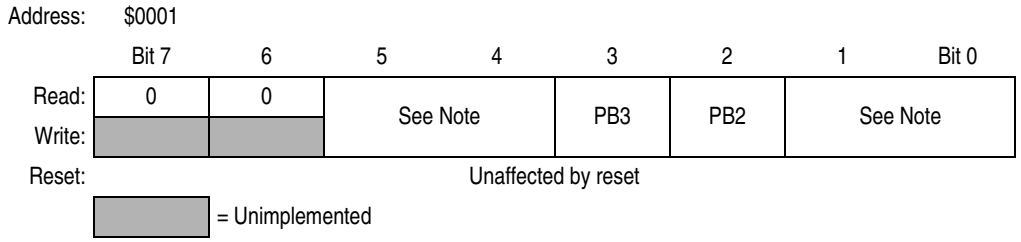
If the PIRQ bit in the mask option register is programmed to logic 1, PA0–PA3 pins function as external interrupt pins. (See Chapter 5 External Interrupt Module (IRQ).)

7.3 Port B

Port B is a 2-bit bidirectional port.

7.3.1 Port B Data Register

The port B data register contains a latch for each port B pin.



Note:
PB5, PB4, PB1, and PB0 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

Figure 7-6. Port B Data Register (PORTB)

PB[3:2] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

NOTE

PB4–PB5 and PB0–PB1 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

10.5 5.0-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –2.5 mA) PA4–PA7 (I_{Load} = –5.5 mA) PB2–PB3, PA0–PA3	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output low voltage[8] (I_{Load} = 10.0 mA) PA0–PA7, PB2–PB3	V_{OL}	—	—	0.8	V
Input high voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (f_{OP} = 2.1 MHz; f_{OSC} = 4.2 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 4.0 1.0 0.1	 6.0 2.8 5.0	 mA mA µA
Supply current (f_{OP} = 4.0 MHz; f_{OSC} = 8.0 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 5.2 1.1 0.1	 7.0 3.3 5.0	 mA mA µA
I/O Ports Hi-Z leakage current PA0–PA7, PB2–PB3 (without individual pulldown activated)	I_{IL}	—	0.2	±1	µA
Input pulldown current PA0–PA7, PB2–PB3 (with individual pulldown activated)	I_{IL}	35	80	200	µA
Input pullup current $\overline{RESET}$	I_{IL}	–15	–35	–85	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.2	±1	µA
Capacitance Ports (As Inputs or Outputs) $\overline{RESET}$, $\overline{IRQ}$, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{OSC}	1.0	2.0	3.0	MΩ

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{OSC} value selected for RC oscillator versions of this device is unspecified.
8. Maximum current drain for all I/O pins combined should not exceed 100 mA.

10.9 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{IRQ}/V_{PP}$	I_{PP}	—¡	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

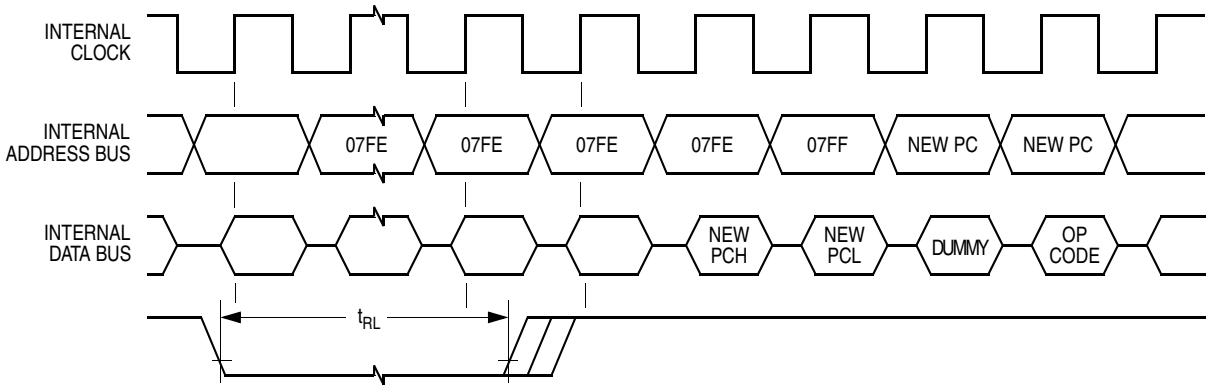
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.

10.10 Control Timing

Table 10-2. Control Timing (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	 — dc	 8.0 8.0	MHz
Internal operating frequency (f_{OSC} ÷ 2) Crystal oscillator External clock	f_{OP}	 — dc	 4.0 4.0	MHz
Cycle time (1 ÷ f_{OP})	t_{cyc}	250	—	ns
$\overline{RESET}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 Interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	100	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.



NOTES:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 10-10. External Reset Timing

A.5 Typical Internal Operating Frequency Versus Temperature (No External Resistor)

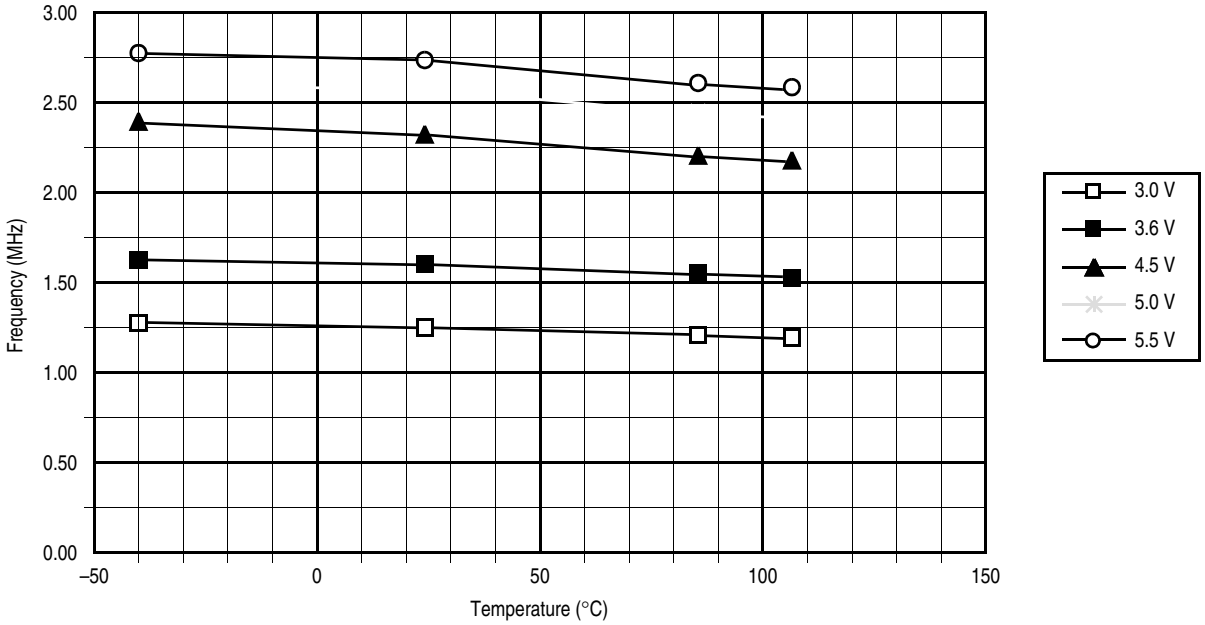


Figure A-4. Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)

NOTE

Due to process variations, operating voltages, and temperature requirements, the internal resistance and tolerance are unspecified. Typically for a given voltage and temperature, the frequency should not vary more than ± 500 kHz. However, this data is not guaranteed. It is the user's responsibility to ensure that the resulting internal operating frequency meets user's requirements.

A.6 Package Types and Order Numbers

Table A-1. MC68HRC705KJ1 (RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	648	16	–40 to +85°C	MC68HRC705KJ1C(2)P(3)
SOIC	751G	16	–40 to +85°C	MC68HRC705KJ1CDW(4)
Cerdip	620A	16	–40 to +85°C	MC68HRC705KJ1CS(5)

1. Refer to Chapter 11 Ordering Information and Mechanical Specifications for standard part ordering information.
2. C = extended temperature range
3. P = plastic dual in-line package (PDIP)
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (Cerdip)