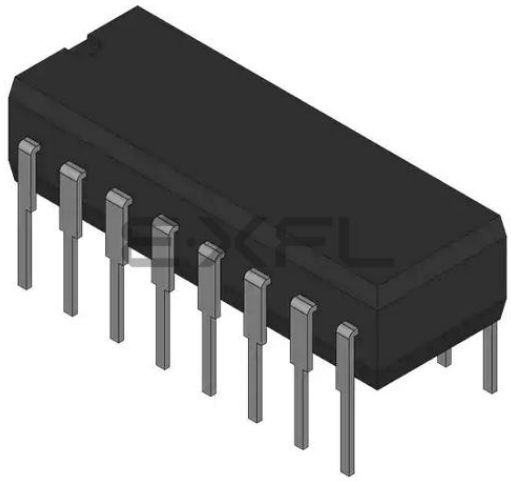

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	10
Program Memory Size	1.2KB (1.2K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	16-DIP (0.300", 7.62mm)
Supplier Device Package	16-PDIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mchrc705kj1cpe

1.4.1 V_{DD} and V_{SS}

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins, placing high, short-duration current demands on the power supply. To prevent noise problems, take special care, as Figure 1-3 shows, by placing the bypass capacitors as close as possible to the MCU. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.

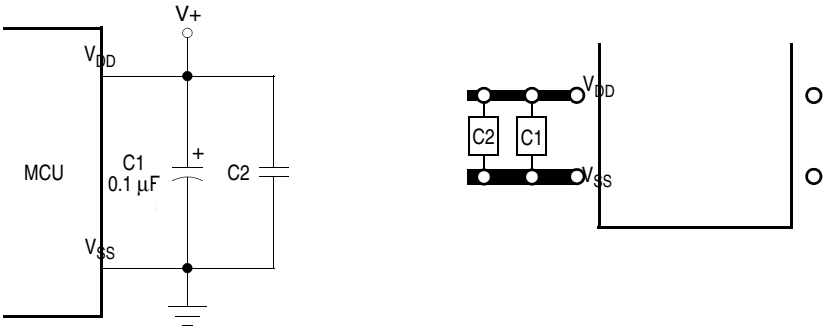


Figure 1-3. Bypassing Layout Recommendation

1.4.2 OSC1 and OSC2

The OSC1 and OSC2 pins are the connections for the on-chip oscillator. The oscillator can be driven by any of the following:

1. Standard crystal (See Figure 1-4 and Figure 1-5.)
2. Ceramic resonator (See Figure 1-6 and Figure 1-7.)
3. Resistor/capacitor (RC) oscillator (Refer to Appendix A MC68HRC705KJ1.)
4. External clock signal as shown in (See Figure 1-8.)
5. Low speed (32 kHz) crystal connections (Refer to Appendix B MC68HLC705KJ1.)

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{OP}.

1.4.2.1 Crystal Oscillator

Figure 1-4 and Figure 1-5 show a typical crystal oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal supplier's recommendations, as the crystal parameters determine the external component values required to provide reliable startup and maximum stability. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances.

To minimize output distortion, mount the crystal and capacitors as close as possible to the pins. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 for the crystal oscillator as a programmable mask option.

NOTE

Use an AT-cut crystal and not an AT-strip crystal because the MCU can overdrive an AT-strip crystal.

3.3.3 Clearing the COP Watchdog

To clear the COP watchdog and prevent a COP reset, write a logic 0 to bit 0 (COPC) of the COP register at location $07F0 (see Figure 3-1). Clearing the COP bit disables the COP watchdog timer regardless of the $\overline{IRQ}/V_{PP}$ pin voltage.

If the main program executes within the COP timeout period, the clearing routine should be executed only once. If the main program takes longer than the COP timeout period, the clearing routine must be executed more than once.

NOTE

Place the clearing routine in the main program and not in an interrupt routine. Clearing the COP watchdog in an interrupt routine might prevent COP watchdog timeouts even though the main program is not operating properly.

3.4 Interrupts

The COP watchdog does not generate interrupts.

3.5 COP Register

The COP register (COPR) is a write-only register that returns the contents of EPROM location $07F0 when read.

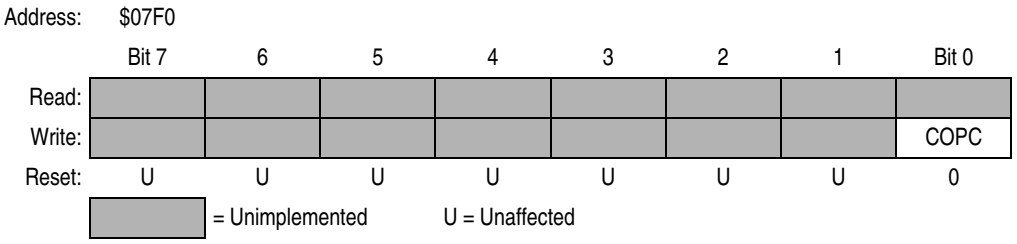


Figure 3-1. COP Register (COPR)

COPC — COP Clear Bit

This write-only bit resets the COP watchdog. Reading address $07F0 returns undefined results.

3.6 Low-Power Modes

The STOP and WAIT instructions have the following effects on the COP watchdog.

3.6.1 Stop Mode

The STOP instruction clears the COP watchdog counter and disables the clock to the COP watchdog.

NOTE

To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.

Chapter 4
Central Processor Unit (CPU)

4.1 Introduction

The central processor unit (CPU) consists of a CPU control unit, an arithmetic/logic unit (ALU), and five CPU registers. The CPU control unit fetches and decodes instructions. The ALU executes the instructions. The CPU registers contain data, addresses, and status bits that reflect the results of CPU operations.

4.2 Features

Features of the CPU include:

- 4.0-MHz bus frequency on standard part
- 8-bit accumulator
- 8-bit index register
- 11-bit program counter
- 6-bit stack pointer
- Condition code register with five status flags
- 62 instructions
- 8 addressing modes
- Power-saving stop, wait, halt, and data-retention modes

The programming model is shown in Figure 4-1.

4.3 CPU Control Unit

The CPU control unit fetches and decodes instructions during program operation. The control unit selects the memory locations to read and write and coordinates the timing of all CPU operations.

4.4 Arithmetic/Logic Unit

The arithmetic/logic unit (ALU) performs the arithmetic, logic, and manipulation operations decoded from the instruction set by the CPU control unit. The ALU produces the results called for by the program and sets or clears status and control bits in the condition code register (CCR).

4.6.2 Instruction Types

The MCU instructions fall into the following five categories:

- Register/memory instructions
- Read-modify-write instructions
- Jump/branch instructions
- Bit manipulation instructions
- Control instructions

4.6.2.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 4-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

4.6.2.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 4-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

NOTE

Do not use bit manipulation instructions on registers with write-only bits.

4.6.2.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 4-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

Table 4-6. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff 	5 6 7 6 5

6.3 Effects of Stop and Wait Modes

The STOP and WAIT instructions have the following effects on MCU modules.

6.3.1 Clock Generation

Effects of STOP and WAIT on clock generation are discussed here.

6.3.1.1 STOP

The STOP instruction disables the internal oscillator, stopping the CPU clock and all peripheral clocks.

After exiting stop mode, the CPU clock and all enabled peripheral clocks begin running after the oscillator stabilization delay.

NOTE

The oscillator stabilization delay holds the MCU in reset for the first 4064 internal clock cycles.

6.3.1.2 WAIT

The WAIT instruction disables the CPU clock.

After exiting wait mode, the CPU clock and all enabled peripheral clocks immediately begin running.

6.3.2 CPU

Effects of STOP and WAIT on the CPU are discussed here.

6.3.2.1 STOP

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

After exit from stop mode by external interrupt, the I bit remains clear.

After exit from stop mode by reset, the I bit is set.

6.3.2.2 WAIT

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts
- Disables the CPU clock

After exit from wait mode by interrupt, the I bit remains clear.

After exit from wait mode by reset, the I bit is set.

6.3.3 COP Watchdog

Effects of STOP and WAIT on the COP watchdog are discussed here.

7.3.2 Data Direction Register B

Data direction register B determines whether each port B pin is an input or an output.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	See Notes		DDRB3	DDRB2	See Note	
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Note:
DDRB5, DDRB4, DDRB1, and DDRB0 should be configured as inputs at all times. These bits are available for read/write but are not available externally. Configuring them as inputs will ensure that the pulldown devices are enabled, thus properly terminating them.

Figure 7-7. Data Direction Register B (DDRB)

DDRB[3:2] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[3:2], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE

Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.

Figure 7-8 shows the I/O logic of port B.

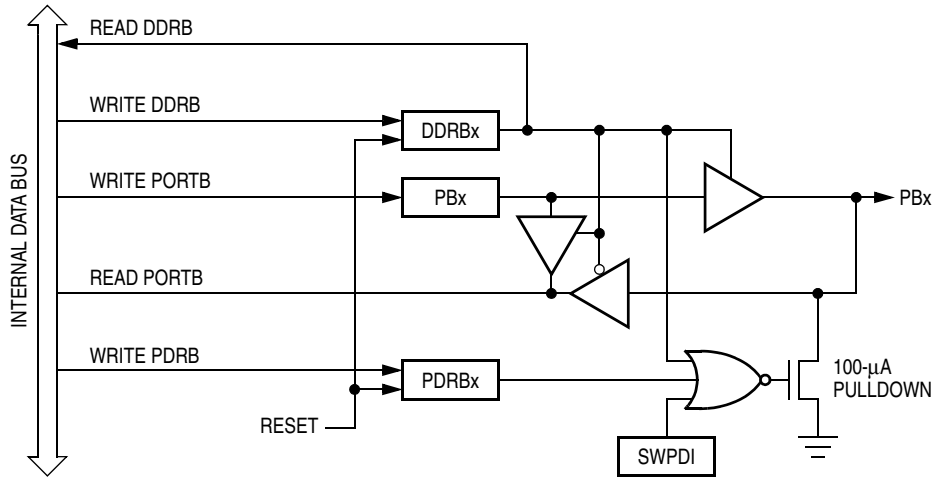


Figure 7-8. Port B I/O Circuitry

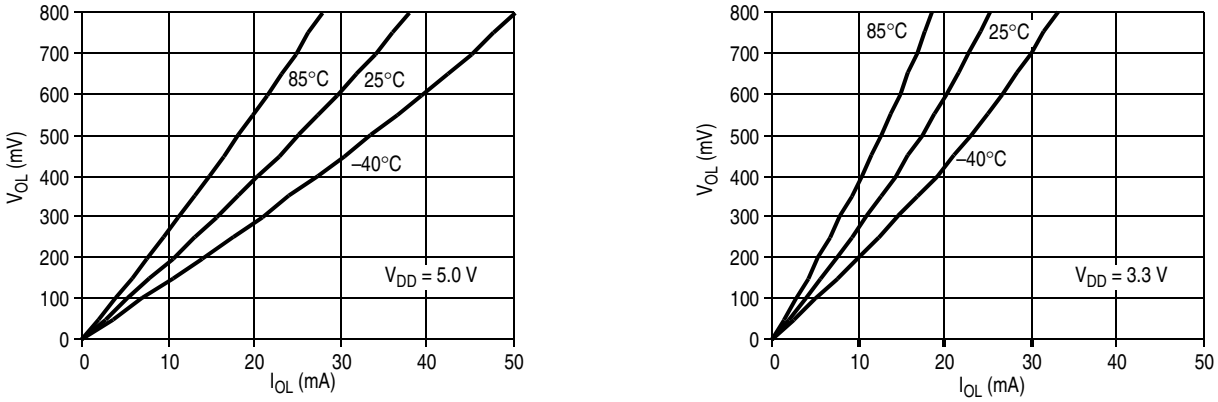
Writing a logic 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a logic 0 disables the output buffer.

When bit DDRBx is a logic 1, reading address $0001 reads the PBx data latch. When bit DDRBx is a logic 0, reading address $0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. Table 7-2 summarizes the operation of the port B pins.

10.5 5.0-V DC Electrical Characteristics

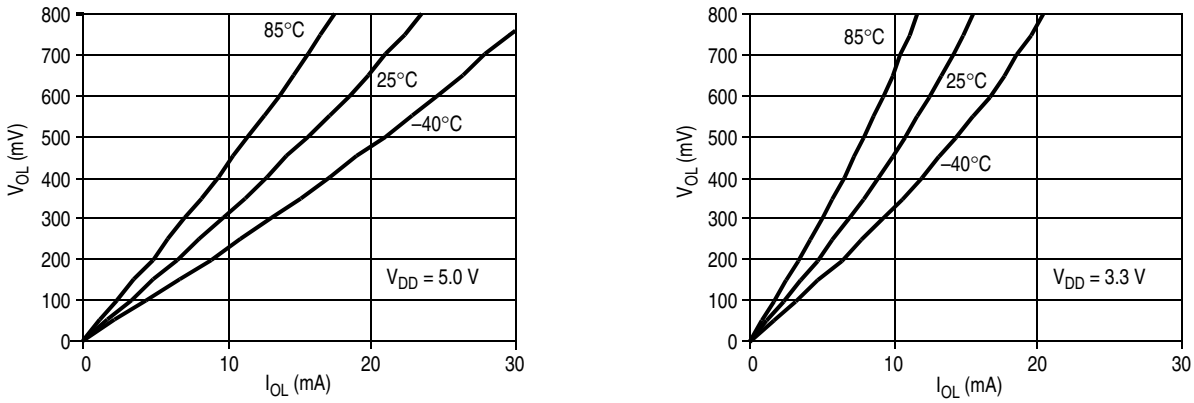
Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –2.5 mA) PA4–PA7 (I_{Load} = –5.5 mA) PB2–PB3, PA0–PA3	V_{OH}	V_{DD} –0.8 V_{DD} –0.8	— —	— —	V
Output low voltage[8] (I_{Load} = 10.0 mA) PA0–PA7, PB2–PB3	V_{OL}	—	—	0.8	V
Input high voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB2–PB3, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (f_{OP} = 2.1 MHz; f_{OSC} = 4.2 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 4.0 1.0 0.1	 6.0 2.8 5.0	 mA mA µA
Supply current (f_{OP} = 4.0 MHz; f_{OSC} = 8.0 MHz) Run mode[3] Wait mode[4] Stop mode[5]	I_{DD}	 — — —	 5.2 1.1 0.1	 7.0 3.3 5.0	 mA mA µA
I/O Ports Hi-Z leakage current PA0–PA7, PB2–PB3 (without individual pulldown activated)	I_{IL}	—	0.2	±1	µA
Input pulldown current PA0–PA7, PB2–PB3 (with individual pulldown activated)	I_{IL}	35	80	200	µA
Input pullup current $\overline{RESET}$	I_{IL}	–15	–35	–85	µA
Input current[6] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{In}	—	0.2	±1	µA
Capacitance Ports (As Inputs or Outputs) $\overline{RESET}$, $\overline{IRQ}$, OSC1, OSC2	 C_{Out} C_{In}	 — —	 — —	 12 8	 pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{OSC}	1.0	2.0	3.0	MΩ

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source; all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V.
6. Only input high current rated to +1 µA on $\overline{RESET}$.
7. The R_{OSC} value selected for RC oscillator versions of this device is unspecified.
8. Maximum current drain for all I/O pins combined should not exceed 100 mA.



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 800$ mV @ I_{OL} = 10.0 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 500$ mV @ I_{OL} = 5.0 mA.

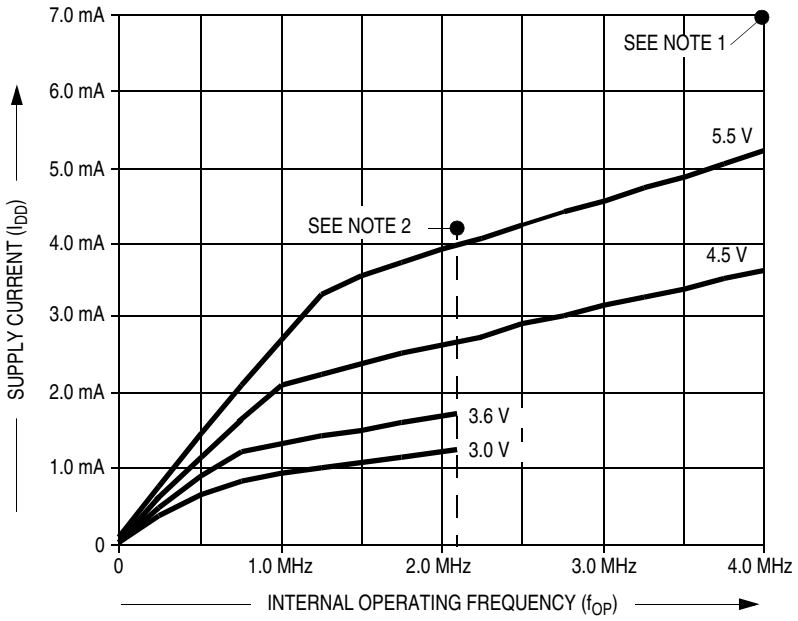
Figure 10-3. PA4–PA7 Typical Low-Side Driver Characteristics



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 800$ mV @ I_{OL} = 10.0 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 500$ mV @ I_{OL} = 3.5 mA.

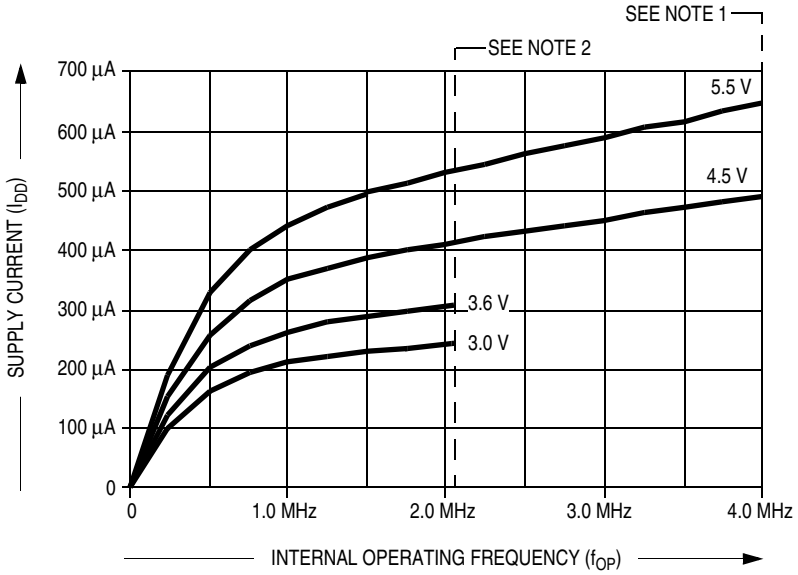
Figure 10-4. PA0–PA3 and PB2–PB3 Typical Low-Side Driver Characteristics

10.8 Typical Supply Currents



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for $I_{DD} \leq 7.0$ mA @ f_{OP} = 4.0 MHz.
2. At V_{DD} = 3.3 V, devices are specified and tested for $I_{DD} \leq 4.25$ mA @ f_{OP} = 2.1 MHz.

Figure 10-5. Typical Operating I_{DD} (25°C)



Notes:
1. At V_{DD} = 5.0 V, devices are specified and tested for $I_{DD} \leq 3.25$ mA @ f_{OP} = 4.0 MHz.
2. At V_{DD} = 3.3 V, devices are specified and tested for $I_{DD} \leq 1.75$ mA @ f_{OP} = 2.1 MHz.

Figure 10-6. Typical Wait Mode I_{DD} (25°C)

10.9 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{IRQ}/V_{PP}$	I_{PP}	—¡	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.

10.10 Control Timing

Table 10-2. Control Timing (V_{DD} = 5.0 Vdc)[1]

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	 — dc	 8.0 8.0	MHz
Internal operating frequency (f_{OSC} ÷ 2) Crystal oscillator External clock	f_{OP}	 — dc	 4.0 4.0	MHz
Cycle time (1 ÷ f_{OP})	t_{cyc}	250	—	ns
$\overline{RESET}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{IRQ}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 Interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	100	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

Table 10-3. Control Timing (V_{DD} = 3.3 Vdc)(1)

Characteristic	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{OSC}	— dc	4.2 4.2	MHz
Internal operating frequency ($f_{OSC} \div 2$) Crystal oscillator External clock	f_{OP}	— dc	2.1 2.1	MHz
Cycle time ($1 \div f_{OP}$)	t_{cyc}	476	—	ns
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note(2)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note(2)	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted.
2. The maximum width t_{ILIL} or t_{ILIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

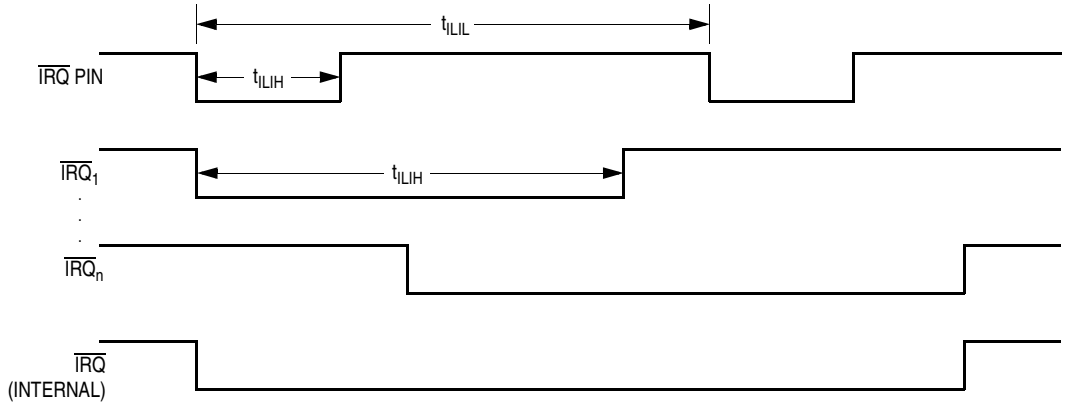


Figure 10-7. External Interrupt Timing

A.5 Typical Internal Operating Frequency Versus Temperature (No External Resistor)

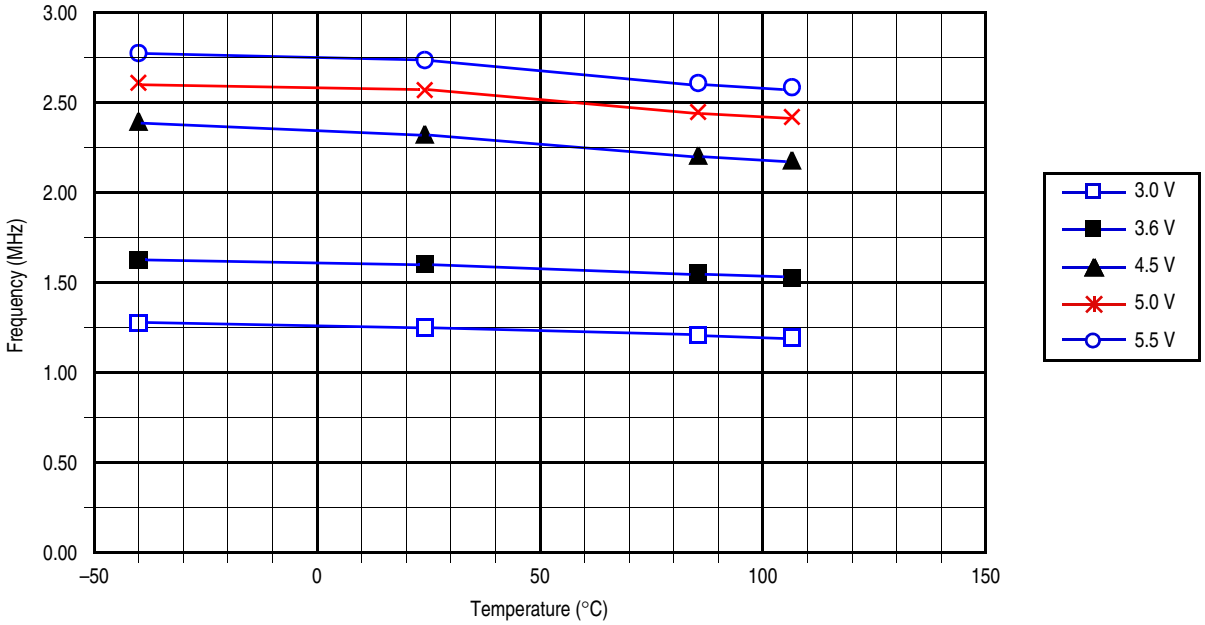


Figure A-4. Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)

NOTE

Due to process variations, operating voltages, and temperature requirements, the internal resistance and tolerance are unspecified. Typically for a given voltage and temperature, the frequency should not vary more than ± 500 kHz. However, this data is not guaranteed. It is the user's responsibility to ensure that the resulting internal operating frequency meets user's requirements.

A.6 Package Types and Order Numbers

Table A-1. MC68HRC705KJ1 (RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	648	16	–40 to +85°C	MC68HRC705KJ1C(2)P(3)
SOIC	751G	16	–40 to +85°C	MC68HRC705KJ1CDW(4)
Cerdip	620A	16	–40 to +85°C	MC68HRC705KJ1CS(5)

1. Refer to Chapter 11 Ordering Information and Mechanical Specifications for standard part ordering information.
2. C = extended temperature range
3. P = plastic dual in-line package (PDIP)
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (Cerdip)

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MC68HC705KJ1
Rev. 4.1, 07/2005

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