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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	19
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-WFQFN Exposed Pad
Supplier Device Package	24-HWQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f213g4mnnp-u0

1.1.2   Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3GM Group.

Table 1.1   Specifications for R8C/3GM Group (1)

Item	Function	Specification

CPU	Central processing unit	R8C CPU core
		• Number of fundamental instructions: 89
		• Minimum instruction execution time:
		    50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V)
		    200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V)
		• Multiplier: 16 bits × 16 bits → 32 bits
		• Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits
		• Operation mode: Single-chip mode (address space: 1 Mbyte)

Memory	ROM, RAM, Data flash	Refer to **Table 1.3 Product List for R8C/3GM Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 19, selectable pull-up resistor • High current drive ports: 19

Clock	Clock generation circuits	4 circuits: XIN clock oscillation circuit,
		              XCIN clock oscillation circuit (32 kHz),
		              High-speed on-chip oscillator (with frequency adjustment function),
		              Low-speed on-chip oscillator
		• Oscillation stop detection: XIN clock oscillation stop detection function
		• Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16
		• Low power consumption modes:
		  Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode

		Real-time clock (timer RE)
Interrupts		• Number of interrupt vectors: 69 • External Interrupt: 7 (INT × 3, Key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 23 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week)

1.4   Pin Assignment

Figure 1.3 shows Pin Assignment (Top View) of PWQN0024KC-A Package. Table 1.4 outlines the Pin Name Information by Pin Number.
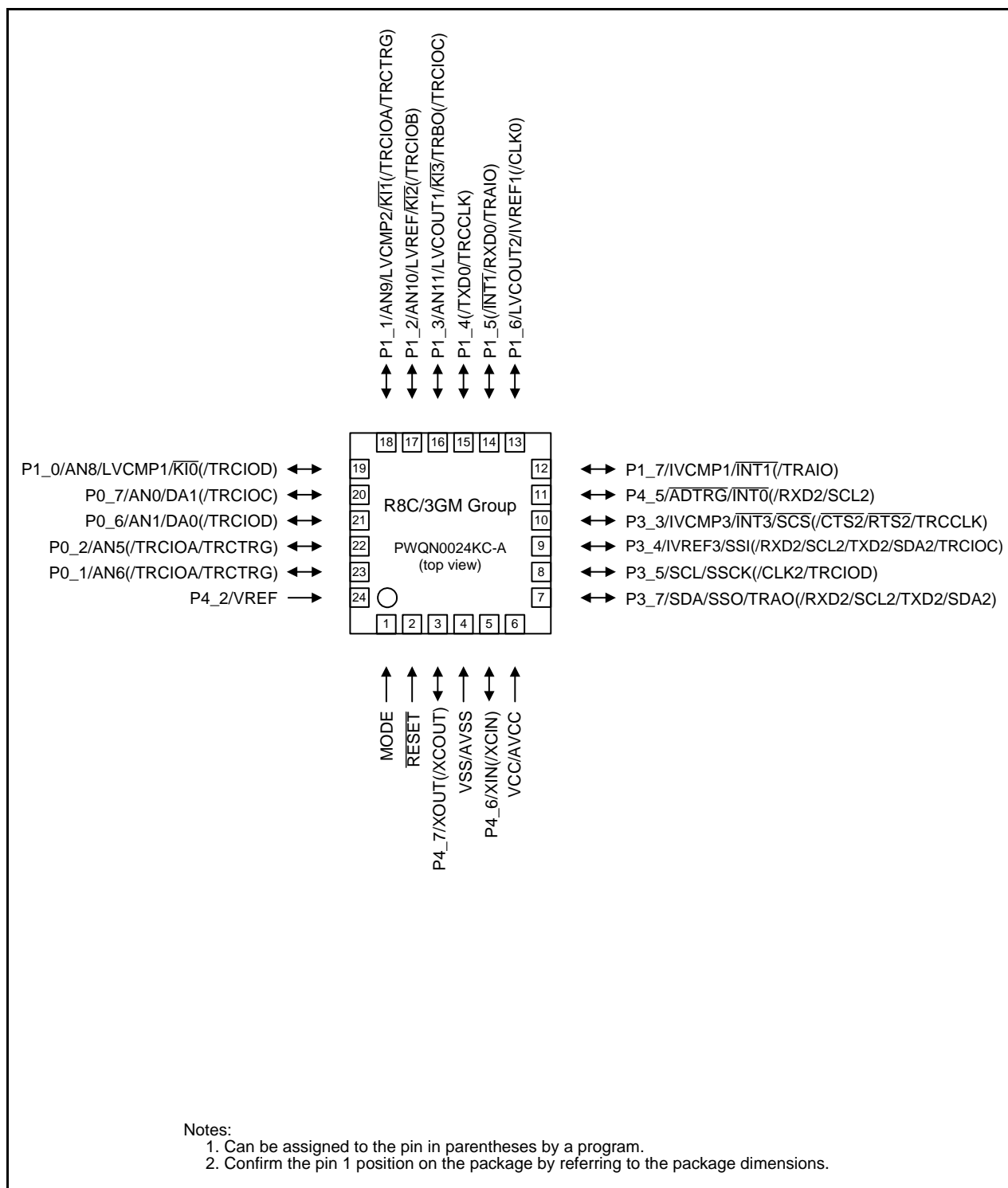

Figure 1.3   Pin Assignment (Top View) of PWQN0024KC-A Package

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7   Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0
when an interrupt request is acknowledged.

2.8.8   Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software
interrupt numbers 0 to 31 is executed.

2.8.9   Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10   Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/3GM Group

Figure 3.1 is a Memory Map of R8C/3GM Group. The R8C/3GM Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte) and block D (1 Kbyte).
2. The blank areas are reserved and cannot be accessed by users.

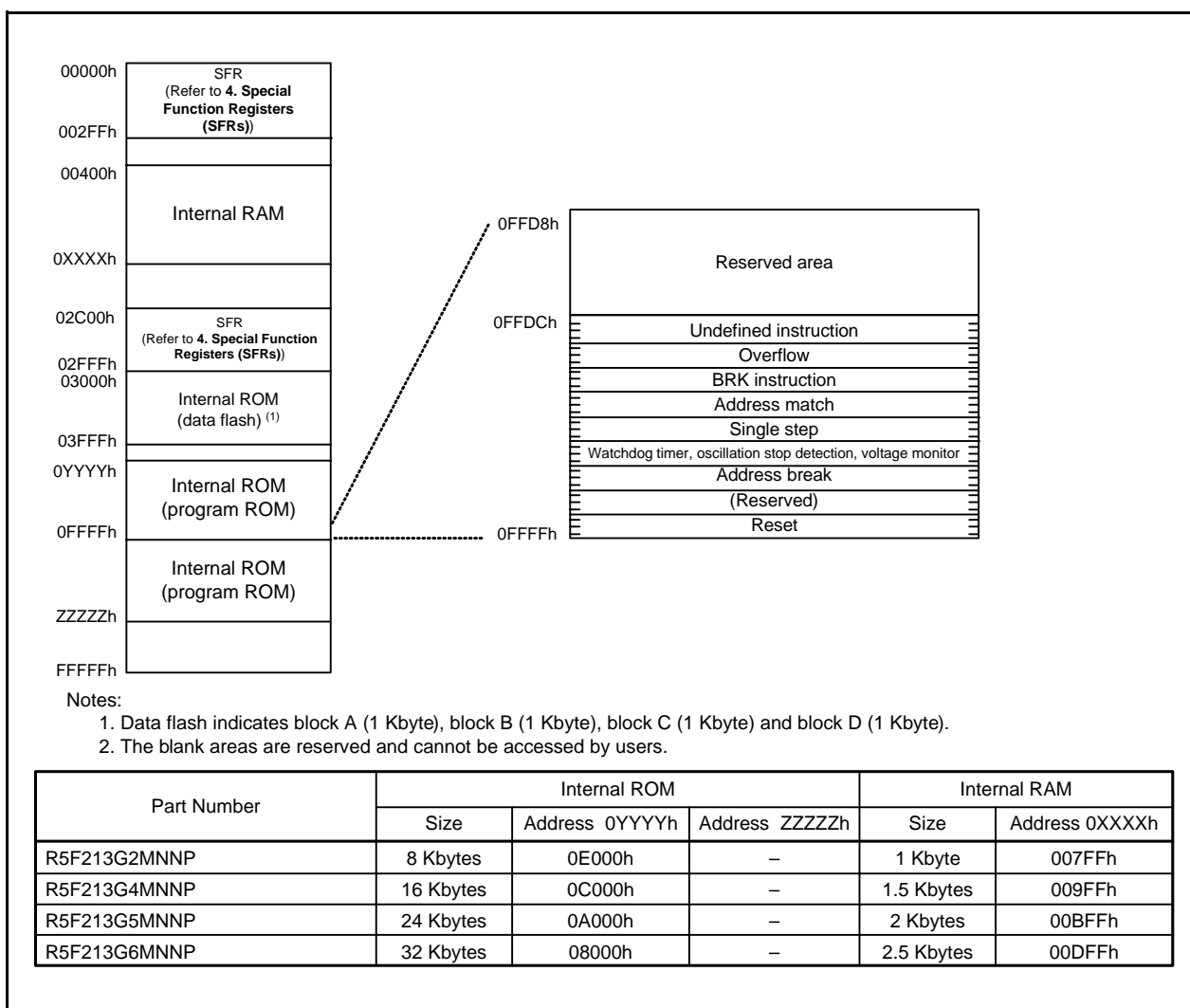| Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F213G2MNNP	8 Kbytes	0E000h	–	1 Kbyte	007FFh
R5F213G4MNNP	16 Kbytes	0C000h	–	1.5 Kbytes	009FFh
R5F213G5MNNP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F213G6MNNP	32 Kbytes	08000h	–	2.5 Kbytes	00DFFh

Figure 3.1   Memory Map of R8C/3GM Group

4.   Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers. Table 4.13 lists the ID Code Areas and Option Function Select Area.

Table 4.1   SFR Information (1) [1]

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb [2]
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h / 10000000b [3]
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit/Comparator A Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h [4] / 00100000b [5]
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b [4] / 1100X011b [5]
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined
Notes:
1.   The blank areas are reserved and cannot be accessed by users.
2.   The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3.   The CSPROINI bit in the OFS register is set to 0.
4.   The LVDAS bit in the OFS register is set to 1.
5.   The LVDAS bit in the OFS register is set to 0.

Table 4.2   SFR Information (2) [1]

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register [2]	SSUIC / IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage Monitor 1/Comparator A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage Monitor 2/Comparator A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1.   The blank areas are reserved and cannot be accessed by users.
2.   Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.4 SFR Information (4) [(1)]

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A0 Register	DA0	00h
00D9h	D/A1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			

Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) [(1)]

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.10   SFR Information (10) [1]

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
    1.   The blank areas are reserved and cannot be accessed by users.

Table 5.2   Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
Vcc/AVcc	Supply voltage					1.8	–	5.5	V
Vss/AVss	Supply voltage					–	0	–	V
VIH	Input "H" voltage	Other than CMOS input				0.8 Vcc	–	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	–	Vcc	V
				Input level selection: 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	–	Vcc	V
				Input level selection: 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	–	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	–	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	–	Vcc	V
		External clock input (XOUT)				1.2	–	Vcc	V
VIL	Input "L" voltage	Other than CMOS input				0	–	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection: 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.2 Vcc	V
				Input level selection: 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	–	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	–	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	–	0.35 Vcc	V
		External clock input (XOUT)				0	–	0.4	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)				–	–	−160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)				–	–	−80	mA
IOH(peak)	Peak output "H" current	Drive capacity Low				–	–	−10	mA
		Drive capacity High				–	–	−40	mA
IOH(avg)	Average output "H" current	Drive capacity Low				–	–	−5	mA
		Drive capacity High				–	–	−20	mA
IOL(sum)	Peak sum output "L" current	Sum of all pins IOL(peak)				–	–	160	mA
IOL(sum)	Average sum output "L" current	Sum of all pins IOL(avg)				–	–	80	mA
IOL(peak)	Peak output "L" current	Drive capacity Low				–	–	10	mA
		Drive capacity High				–	–	40	mA
IOL(avg)	Average output "L" current	Drive capacity Low				–	–	5	mA
		Drive capacity High				–	–	20	mA
f(XIN)	XIN clock input oscillation frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
f(XCIN)	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC [3]				2.7 V ≤ Vcc ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
–	System clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz
f(BCLK)	CPU clock frequency				2.7 V ≤ Vcc ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ Vcc < 2.7 V	–	–	5	MHz

Notes:
1. Vcc = 1.8 to 5.5 V and Topr = −20 to 85°C (N version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC in the range of Vcc = 2.7 V to 5.5V.

Table 5.15   Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on [2]		–	–	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 5.5 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.16   Timing Requirements of Synchronous Serial Communication Unit (SSU) [1]

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
tSUCYC	SSCK clock cycle time			4	–	–	tCYC [2]
tHI	SSCK clock "H" width			0.4	–	0.6	tSUCYC
tLO	SSCK clock "L" width			0.4	–	0.6	tSUCYC
tRISE	SSCK clock rising time	Master		–	–	1	tCYC [2]
		Slave		–	–	1	µs
tFALL	SSCK clock falling time	Master		–	–	1	tCYC [2]
		Slave		–	–	1	µs
tSU	SSO, SSI data input setup time			100	–	–	ns
tH	SSO, SSI data input hold time			1	–	–	tCYC [2]
tLEAD	$\overline{SCS}$ setup time	Slave		1tCYC + 50	–	–	ns
tLAG	$\overline{SCS}$ hold time	Slave		1tCYC + 50	–	–	ns
tOD	SSO, SSI data output delay time			–	–	1	tCYC [2]
tSA	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5tCYC + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5tCYC + 200	ns
tOR	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	1.5tCYC + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	–	–	1.5tCYC + 200	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = −20 to 85°C (N version), unless otherwise specified.
2. $1t_{CYC}$ = 1/f1(s)

Table 5.19   Electrical Characteristics (2) [3.3 V $\leq$ Vcc $\leq$ 5.5 V]
(T$_{opr}$ = $-$20 to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	6.5	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	5.3	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	3.6	−	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	3.0	−	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	2.2	−	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.5	−	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	3.0	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16, MSTIIC = MSTTRD = MSTTRC = 1	−	1	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	−	90	400	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	−	85	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	−	47	−	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	15	100	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	4	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	3.5	−	μA
		Stop mode	XIN clock off, T$_{opr}$ = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1, Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	2.0	5.0	μA
			XIN clock off, T$_{opr}$ = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1, Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	5.0	−	μA

Table 5.25   Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
**(Topr = −20 to 85°C (N version), unless otherwise specified.)**

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	3.0	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	4.0	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.5	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	−	1	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	−	90	390	μA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	−	80	400	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	−	40	−	μA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	−	15	90	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	−	4	80	μA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	−	3.5	−	μA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	2.0	5.0	μA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	5.0	−	μA

Table 5.31   Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = −20 to 85°C (N version), unless otherwise specified.)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	−	2.2	−	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	0.8	−	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	−	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	−	1.7	−	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	−	1	−	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	−	90	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, FMR27 = 1, VCA20 = 0	−	80	350	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division, Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	−	40	−	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	−	3.5	−	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	2.0	5	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	−	5.0	−	µA

Timing Requirements
(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C)

Table 5.32   External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	200	–	ns
$t_{WH(XOUT)}$	XOUT input "H" width	90	–	ns
$t_{WL(XOUT)}$	XOUT input "L" width	90	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	μs
$t_{WH(XCIN)}$	XCIN input "H" width	7	–	μs
$t_{WL(XCIN)}$	XCIN input "L" width	7	–	μs
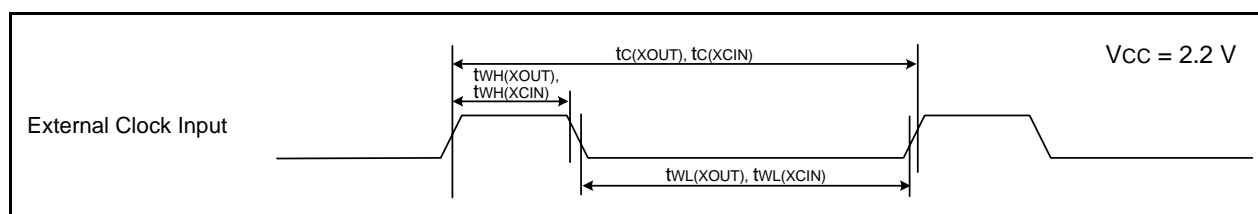
Figure 5.16   External Clock Input Timing Diagram when Vcc = 2.2 V

Table 5.33   TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	–	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	200	–	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	200	–	ns
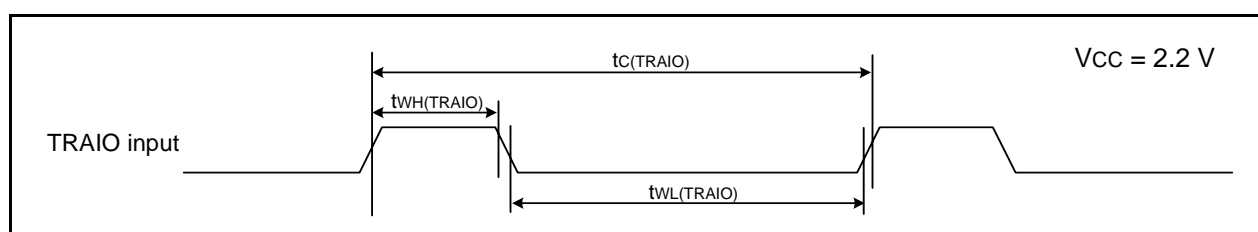
Figure 5.17   TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.34   Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
t$_{C(CK)}$	CLKi input cycle time	When external clock is selected	800	–	ns
t$_{W(CKH)}$	CLKi input "H" width		400	–	ns
t$_{W(CKL)}$	CLKi input "L" width		400	–	ns
t$_{d(C-Q)}$	TXDi output delay time		–	200	ns
t$_{h(C-Q)}$	TXDi hold time		0	–	ns
t$_{su(D-C)}$	RXDi input setup time		150	–	ns
t$_{h(C-D)}$	RXDi input hold time		90	–	ns
t$_{d(C-Q)}$	TXDi output delay time	When internal clock is selected	–	200	ns
t$_{su(D-C)}$	RXDi input setup time		150	–	ns
t$_{h(C-D)}$	RXDi input hold time		90	–	ns

i = 0 or 2

Note:
1. Vcc = 2.2 V and Topr = −20 to 85°C (N version), unless otherwise specified.
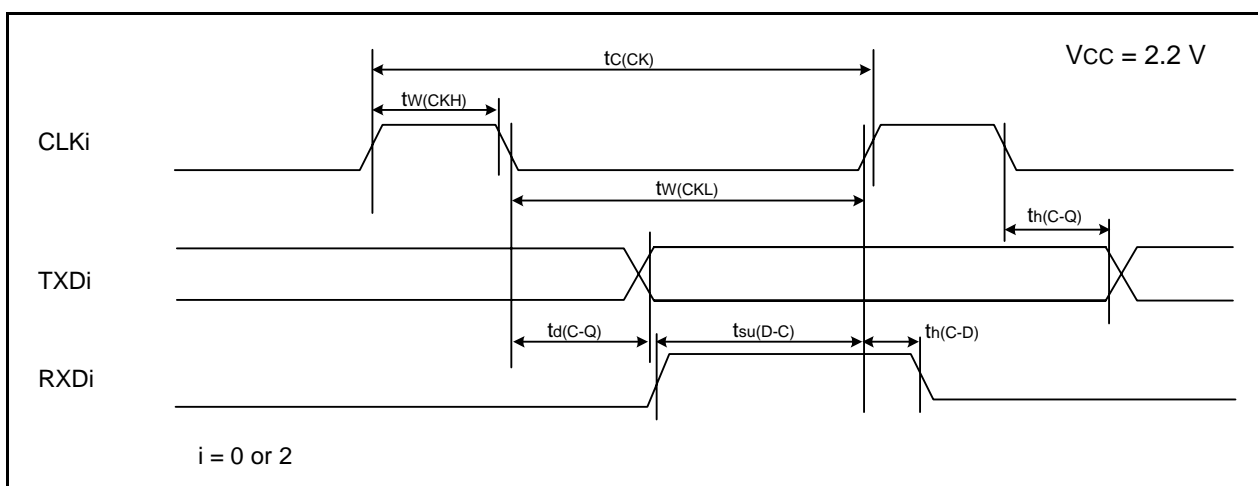
Figure 5.18   Serial Interface Timing Diagram when V$_{CC}$ = 2.2 V

Table 5.35   External Interrupt INTi (i = 0, 1, 3) Input, Key Input Interrupt KIi (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{W(INH)}$	INTi input "H" width, KIi input "H" width	1000 [1]	–	ns
t$_{W(INL)}$	INTi input "L" width, KIi input "L" width	1000 [2]	–	ns

Notes:
1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
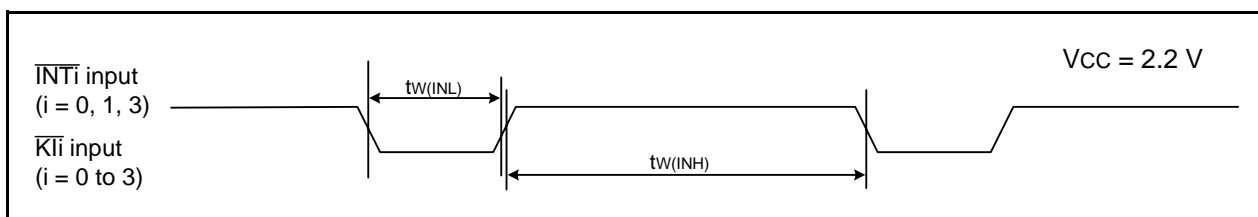
Figure 5.19   Input Timing Diagram for External Interrupt INTi and Key Input Interrupt KIi when Vcc = 2.2 V

REVISION HISTORY		R8C/3GM Group Datasheet		

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

    Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

    — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

    The state of the product is undefined at the moment when power is supplied.

    — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

    Access to reserved addresses is prohibited.

    — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

    After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

    — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

    Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

    — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.