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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.25K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4585-i-pt

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PIC18F2585/2680/4585/4680

TABLE 1-3: PIC18F4585/4680 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RA0/AN0/CVREF RA0 AN0 CVREF	2	19	19	I/O I O	TTL Analog Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog input 0. Analog comparator reference output.
RA1/AN1 RA1 AN1	3	20	20	I/O I	TTL Analog	Digital I/O. Analog input 1.
RA2/AN2/VREF- RA2 AN2 VREF-	4	21	21	I/O I I	TTL Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	22	22	I/O I I	TTL Analog Analog	Digital I/O. Analog input 3. A/D reference voltage (high) input.
RA4/T0CKI RA4 T0CKI	6	23	23	I/O I	TTL ST	Digital I/O. Timer0 external clock input.
RA5/AN4/ $\overline{SS}$ /HLVDIN RA5 AN4 $\overline{SS}$ HLVDIN	7	24	24	I/O I I I	TTL Analog TTL Analog	Digital I/O. Analog input 4. SPI slave select input. High/Low-Voltage Detect input.
RA6						See the OSC2/CLKO/RA6 pin.
RA7						See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels I = Input
O = Output P = Power

PIC18F2585/2680/4585/4680

3.1.3 CLOCK TRANSITIONS AND STATUS INDICATORS

The length of the transition between clock sources is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Three bits indicate the current clock source and its status. They are:

- OSTS (OSCCON<3>)
- IOFS (OSCCON<2>)
- T1RUN (T1CON<6>)

In general, only one of these bits will be set while in a given power managed mode. When the OSTS bit is set, the primary clock is providing the device clock. When the IOFS bit is set, the INTOSC output is providing a stable 8 MHz clock source to a divider that actually drives the device clock. When the T1RUN bit is set, the Timer1 oscillator is providing the clock. If none of these bits are set, then either the INTRC clock source is clocking the device, or the INTOSC source is not yet stable.

If the internal oscillator block is configured as the primary clock source by the FOSC3:FOSC0 Configuration bits, then both the OSTS and IOFS bits may be set when in PRI_RUN or PRI_IDLE modes. This indicates that the primary clock (INTOSC output) is generating a stable 8 MHz output. Entering another RC power managed mode at the same frequency would clear the OSTS bit.

Note 1: Caution should be used when modifying a single IRCF bit. If VDD is less than 3V, it is possible to select a higher clock speed than is supported by the low VDD. Improper device operation may result if the VDD/FOSC specifications are violated.

- 2: Executing a `SLEEP` instruction does not necessarily place the device into Sleep mode. It acts as the trigger to place the controller into either the Sleep mode or one of the Idle modes, depending on the setting of the IDLEN bit.

3.1.4 MULTIPLE SLEEP COMMANDS

The power managed mode that is invoked with the `SLEEP` instruction is determined by the setting of the IDLEN bit at the time the instruction is executed. If another `SLEEP` instruction is executed, the device will enter the power managed mode specified by IDLEN at that time. If IDLEN has changed, the device will enter the new power managed mode specified by the new setting.

3.2 Run Modes

In the Run modes, clocks to both the core and peripherals are active. The difference between these modes is the clock source.

3.2.1 PRI_RUN MODE

The PRI_RUN mode is the normal, full power execution mode of the microcontroller. This is also the default mode upon a device Reset, unless Two-Speed Start-up is enabled (see **Section 24.3 “Two-Speed Start-up”** for details). In this mode, the OSTS bit is set. The IOFS bit may be set if the internal oscillator block is the primary clock source (see **Section 2.7.1 “Oscillator Control Register”**).

3.2.2 SEC_RUN MODE

The SEC_RUN mode is the compatible mode to the “clock switching” feature offered in other PIC18 devices. In this mode, the CPU and peripherals are clocked from the Timer1 oscillator. This gives users the option of lower power consumption while still using a high accuracy clock source.

SEC_RUN mode is entered by setting the SCS1:SCS0 bits to ‘01’. The device clock source is switched to the Timer1 oscillator (see Figure 3-1), the primary oscillator is shut down, the T1RUN bit (T1CON<6>) is set and the OSTS bit is cleared.

Note: The Timer1 oscillator should already be running prior to entering SEC_RUN mode. If the T1OSCEN bit is not set when the SCS1:SCS0 bits are set to ‘01’, entry to SEC_RUN mode will not occur. If the Timer1 oscillator is enabled but not yet running, device clocks will be delayed until the oscillator has started. In such situations, initial oscillator operation is far from stable and unpredictable operation may result.

On transitions from SEC_RUN mode to PRI_RUN, the peripherals and CPU continue to be clocked from the Timer1 oscillator while the primary clock is started. When the primary clock becomes ready, a clock switch back to the primary clock occurs (see Figure 3-2). When the clock switch is complete, the T1RUN bit is cleared, the OSTS bit is set and the primary clock is providing the clock. The IDLEN and SCS bits are not affected by the wake-up; the Timer1 oscillator continues to run.

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5.1.2.4 Stack Full and Underflow Resets

Device Resets on stack overflow and stack underflow conditions are enabled by setting the STVREN bit in Configuration Register 4L. When STVREN is set, a full or underflow will set the appropriate STKFUL or STKUNF bit and then cause a device Reset. When STVREN is cleared, a full or underflow condition will set the appropriate STKFUL or STKUNF bit, but not cause a device Reset. The STKFUL or STKUNF bits are cleared by the user software or a Power-on Reset.

5.1.3 FAST REGISTER STACK

A fast register stack is provided for the STATUS, WREG and BSR registers, to provide a “fast return” option for interrupts. Each stack is only one level deep and is neither readable nor writable. It is loaded with the current value of the corresponding register when the processor vectors for an interrupt. All interrupt sources will push values into the stack registers. The values in the registers are then loaded back into their associated registers, if the RETFIE, FAST instruction is used to return from the interrupt.

If both low and high priority interrupts are enabled, the stack registers cannot be used reliably to return from low priority interrupts. If a high priority interrupt occurs while servicing a low priority interrupt, the stack register values stored by the low priority interrupt will be overwritten. In these cases, users must save the key registers in software during a low priority interrupt.

If interrupt priority is not used, all interrupts may use the fast register stack for returns from interrupt. If no interrupts are used, the fast register stack can be used to restore the STATUS, WREG and BSR registers at the end of a subroutine call. To use the fast register stack for a subroutine call, a CALL label, FAST instruction must be executed to save the STATUS, WREG and BSR registers to the fast register stack. A RETURN, FAST instruction is then executed to restore these registers from the fast register stack.

Example 5-1 shows a source code example that uses the fast register stack during a subroutine call and return.

EXAMPLE 5-1: FAST REGISTER STACK CODE EXAMPLE

```
CALL SUB1, FAST      ;STATUS, WREG, BSR
                     ;SAVED IN FAST REGISTER
                     ;STACK
    .
    .
SUB1  .
    .
    RETURN, FAST     ;RESTORE VALUES SAVED
                     ;IN FAST REGISTER STACK
```

5.1.4 LOOK-UP TABLES IN PROGRAM MEMORY

There may be programming situations that require the creation of data structures, or look-up tables, in program memory. For PIC18 devices, look-up tables can be implemented in two ways:

- Computed GOTO
- Table Reads

5.1.4.1 Computed GOTO

A computed GOTO is accomplished by adding an offset to the program counter. An example is shown in Example 5-2.

A look-up table can be formed with an ADDWF PCL instruction and a group of RETLW nn instructions. The W register is loaded with an offset into the table before executing a CALL to that table. The first instruction of the called routine is the ADDWF PCL instruction. The next instruction executed will be one of the RETLW nn instructions, that returns the value ‘nn’ to the calling function.

The offset value (in WREG) specifies the number of bytes that the program counter should advance and should be multiples of 2 (LSb = 0).

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

EXAMPLE 5-2: COMPUTED GOTO USING AN OFFSET VALUE

```
MOVWF OFFSET, W
CALL TABLE
ORG nn00h
TABLE ADDWF PCL
      RETLW nnh
      RETLW nnh
      RETLW nnh
      .
      .
      .
```

5.1.4.2 Table Reads and Table Writes

A better method of storing data in program memory allows two bytes of data to be stored in each instruction location.

Look-up table data may be stored two bytes per program word by using table reads and writes. The Table Pointer (TBLPTR) register specifies the byte address and the Table Latch (TABLAT) register contains the data that is read from or written to program memory. Data is transferred to or from program memory one byte at a time.

Table read and table write operations are discussed further in **Section 6.1 “Table Reads and Table Writes”**.

5.4.3.1 FSR Registers and the INDF Operand

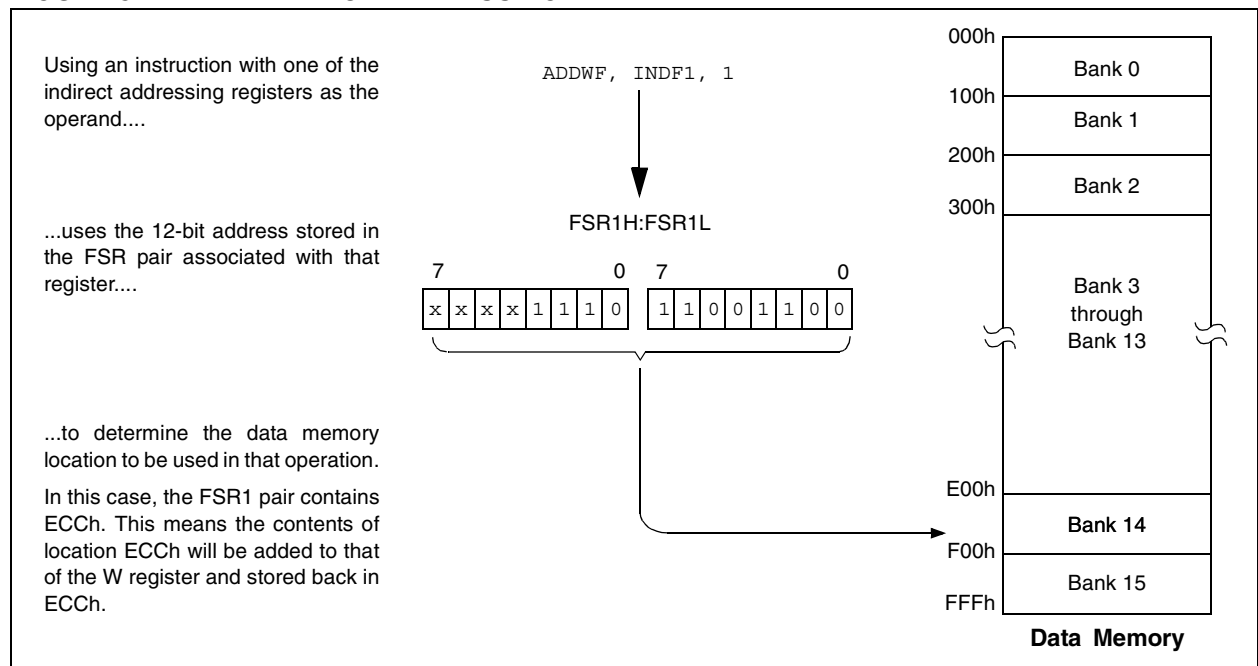
At the core of indirect addressing are three sets of registers: FSR0, FSR1 and FSR2. Each represents a pair of 8-bit registers, FSRnH and FSRnL. The four upper bits of the FSRnH register are not used, so each FSR pair holds a 12-bit value. This represents a value that can address the entire range of the data memory in a linear fashion. The FSR register pairs, then, serve as pointers to data memory locations.

Indirect addressing is accomplished with a set of Indirect File Operands, INDF0 through INDF2. These can be thought of as “virtual” registers: they are

mapped in the SFR space, but are not physically implemented. Reading or writing to a particular INDF register actually accesses its corresponding FSR register pair. A read from INDF1, for example, reads the data at the address indicated by FSR1H:FSR1L. Instructions that use the INDF registers as operands actually use the contents of their corresponding FSR as a pointer to the instruction’s target. The INDF operand is just a convenient way of using the pointer.

Because indirect addressing uses a full 12-bit address, data RAM banking is not necessary. Thus, the current contents of the BSR and the Access RAM bit have no effect on determining the target address.

FIGURE 5-7: INDIRECT ADDRESSING



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The ECCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the ECCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation.

EQUATION 15-3:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{F_{\text{OSC}}}{F_{\text{PWM}}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period, the ECCP1 pin will not be cleared.

TABLE 15-4: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	14	12	10	8	7	6.58

15.4.3 PWM AUTO-SHUTDOWN (ECCP1 ONLY)

The PWM auto-shutdown features of the Enhanced CCP1 module are available to ECCP1 in PIC18F4585/4680 (40/44-pin) devices. The operation of this feature is discussed in detail in **Section 16.4.7 “Enhanced PWM Auto-Shutdown”**.

Auto-shutdown features are not available for CCP1.

15.4.4 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP1 module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the appropriate TRIS bit.
4. Set the TMR2 prescale value, then enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

17.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

17.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)
 - Full Master mode
 - Slave mode (with general address call)

The I²C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- Slave mode

17.2 Control Registers

The MSSP module has three associated registers. These include a status register (SSPSTAT) and two control registers (SSPCON1 and SSPCON2). The use of these registers and their individual configuration bits differ significantly depending on whether the MSSP module is operated in SPI or I²C mode.

Additional details are provided under the individual sections.

17.3 SPI Mode

The SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) – RC5/SDO
- Serial Data In (SDI) – RC4/SDI/SDA
- Serial Clock (SCK) – RC3/SCK/SCL

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$) – RA5/AN4/ $\overline{SS}$ /HLVDIN

Figure 17-1 shows the block diagram of the MSSP module when operating in SPI mode.

FIGURE 17-1: MSSP BLOCK DIAGRAM (SPI MODE)

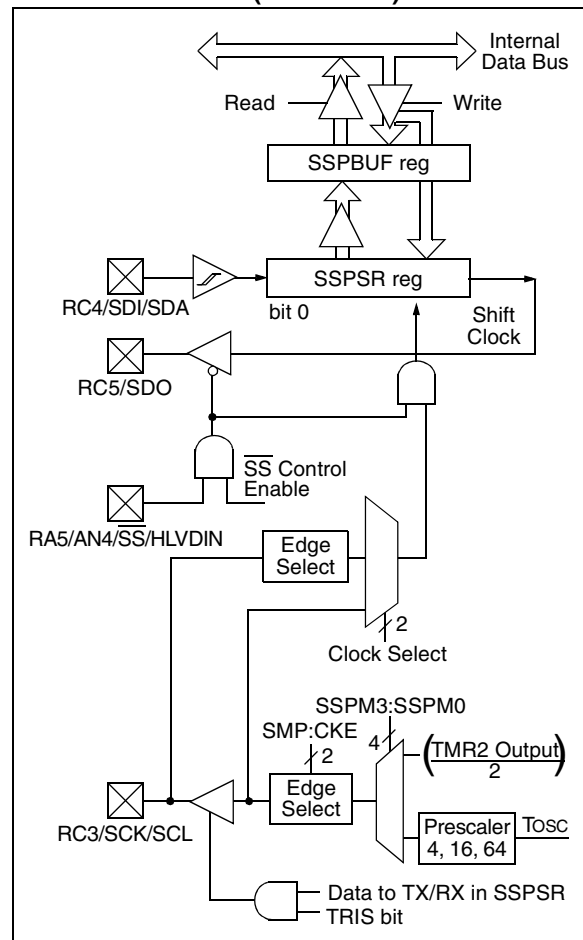


FIGURE 18-4: ASYNCHRONOUS TRANSMISSION

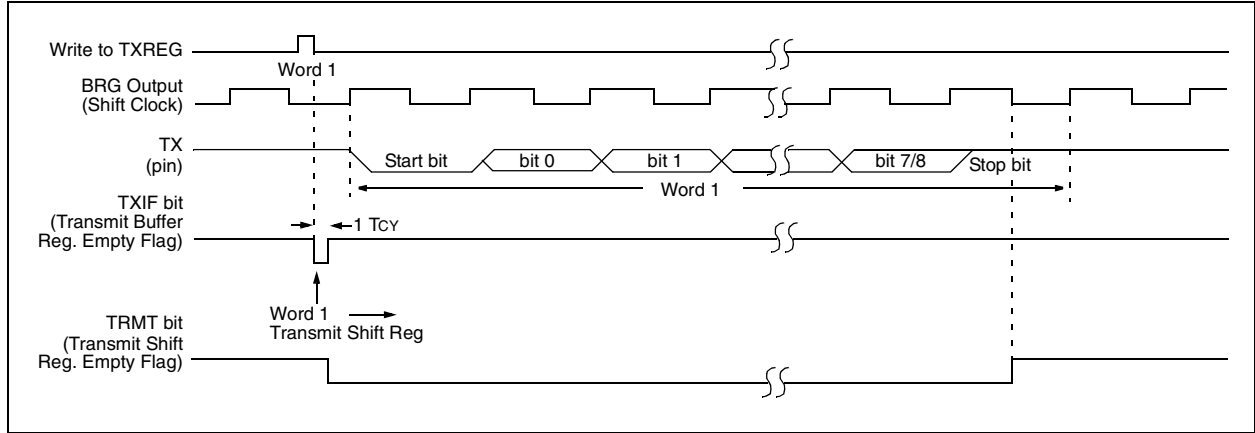


FIGURE 18-5: ASYNCHRONOUS TRANSMISSION (BACK TO BACK)

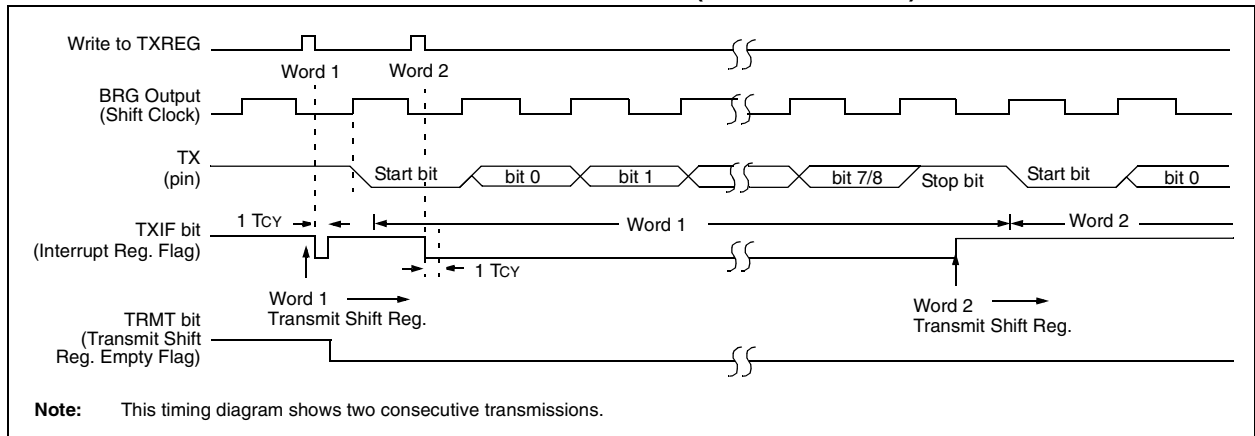


TABLE 18-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	49
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	52
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	52
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	52
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	51
TXREG	EUSART Transmit Register								51
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	51
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	51
SPBRGH	EUSART Baud Rate Generator Register High Byte								51
SPBRG	EUSART Baud Rate Generator Register Low Byte								51

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: Reserved in PIC18F2X8X devices; always maintain these bits clear.

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18.2.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper byte reception cannot be performed. The auto-wake-up feature allows the controller to wake-up due to activity on the RX/DT line while the EUSART is operating in Asynchronous mode.

The auto-wake-up feature is enabled by setting the WUE bit (BAUDCON<1>). Once set, the typical receive sequence on RX/DT is disabled and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a Wake-up Signal character for the LIN protocol.)

Following a wake-up event, the module generates an RCIF interrupt. The interrupt is generated synchronously to the Q clocks in normal operating modes (Figure 18-8) and asynchronously, if the device is in Sleep mode (Figure 18-9). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared once a low-to-high transition is observed on the RX line following the wake-up event. At this point, the EUSART module is in Idle mode and returns to normal operation. This signals to the user that the Sync Break event is over.

18.2.4.1 Special Considerations Using Auto-Wake-up

Since auto-wake-up functions by sensing rising edge transitions on RX/DT, information with any state changes before the Stop bit may signal a false

end-of-character and cause data or framing errors. To work properly, therefore, the initial character in the transmission must be all '0's. This can be 00h (8 bytes) for standard RS-232 devices or 000h (12 bits) for LIN bus.

Oscillator start-up time must also be considered, especially in applications using oscillators with longer start-up intervals (i.e., XT or HS mode). The Sync Break (or Wake-up Signal) character must be of sufficient length and be followed by a sufficient interval to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

18.2.4.2 Special Considerations Using the WUE Bit

The timing of WUE and RCIF events may cause some confusion when it comes to determining the validity of received data. As noted, setting the WUE bit places the EUSART in an Idle mode. The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared after this when a rising edge is seen on RX/DT. The interrupt condition is then cleared by reading the RCREG register. Ordinarily, the data in RCREG will be dummy data and should be discarded.

The fact that the WUE bit has been cleared (or is still set) and the RCIF flag is set should not be used as an indicator of the integrity of the data in RCREG. Users should consider implementing a parallel method in firmware to verify received data integrity.

To assure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

FIGURE 18-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING NORMAL OPERATION

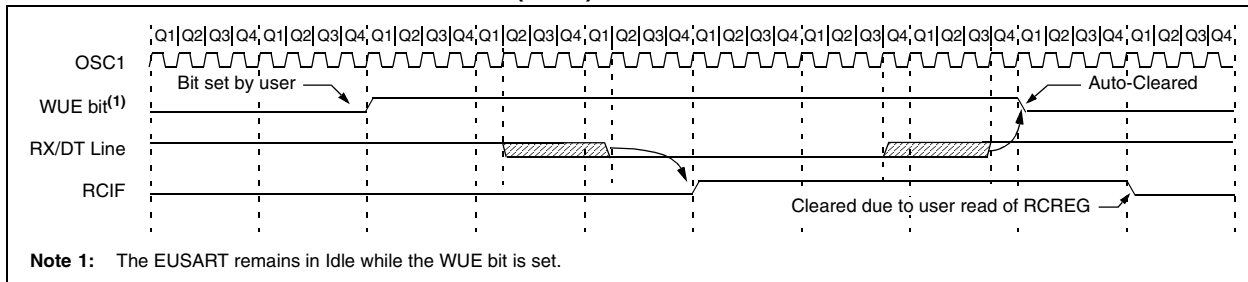
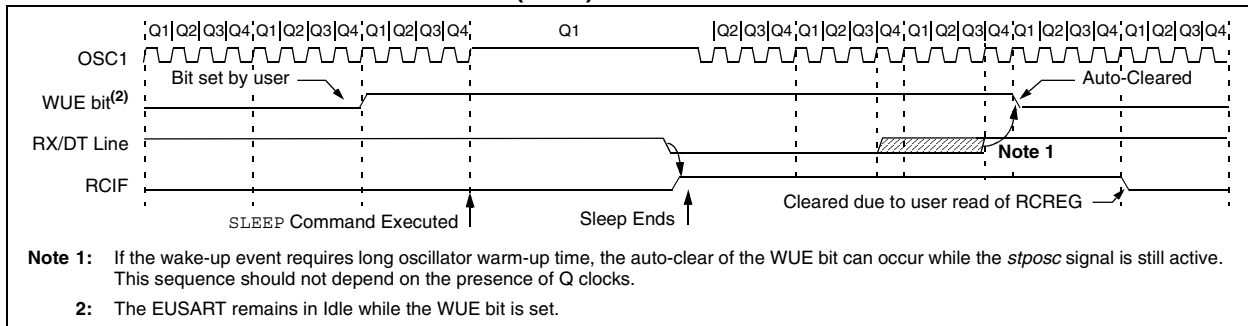


FIGURE 18-9: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP



PIC18F2585/2680/4585/4680

REGISTER 23-14: RXB1CON: RECEIVE BUFFER 1 CONTROL REGISTER (CONTINUED)

bit 2-0

Mode 0:

FILHIT2:FILHIT0: Filter Hit bits

These bits indicate which acceptance filter enabled the last message reception into Receive Buffer 1.

111 = Reserved

110 = Reserved

101 = Acceptance Filter 5 (RXF5)

100 = Acceptance Filter 4 (RXF4)

011 = Acceptance Filter 3 (RXF3)

010 = Acceptance Filter 2 (RXF2)

001 = Acceptance Filter 1 (RXF1), only possible when RXB0DBEN bit is set

000 = Acceptance Filter 0 (RXF0), only possible when RXB0DBEN bit is set

Mode 1, 2:

FILHIT2:FILHIT0 Filter Hit bits <2:0>

These bits, in combination with FILHIT<4:3>, indicate which acceptance filter enabled the message reception into this receive buffer.

01111 = Acceptance Filter 15 (RXF15)

01110 = Acceptance Filter 14 (RXF14)

...

00000 = Acceptance Filter 0 (RXF0)

Legend:

C = Clearable bit

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 23-15: RXBnSIDH: RECEIVE BUFFER n STANDARD IDENTIFIER REGISTERS, HIGH BYTE [0 ≤ n ≤ 1]

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 7							bit 0

bit 7-0

SID10:SID3: Standard Identifier bits (if EXID (RXBnSIDL<3>) = 0)

Extended Identifier bits EID28:EID21 (if EXID = 1).

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

PIC18F2585/2680/4585/4680

REGISTER 23-16: RXBnSIDL: RECEIVE BUFFER n STANDARD IDENTIFIER REGISTERS, LOW BYTE [$0 \leq n \leq 1$]

R-x	R-x	R-x	R-x	R-x	U-0	R-x	R-x
SID2	SID1	SID0	SRR	EXID	—	EID17	EID16
bit 7						bit 0	

- bit 7-5 **SID2:SID0:** Standard Identifier bits (if EXID = 0)
Extended Identifier bits EID20:EID18 (if EXID = 1).
- bit 4 **SRR:** Substitute Remote Request bit
This bit is always '0' when EXID = 1 or equal to the value of RXRTRRO (RBXnCON<3>) when EXID = 0.
- bit 3 **EXID:** Extended Identifier bit
1 = Received message is an extended data frame, SID10:SID0 are EID28:EID18
0 = Received message is a standard data frame
- bit 2 **Unimplemented:** Read as '0'
- bit 1-0 **EID17:EID16:** Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 23-17: RXBnEIDH: RECEIVE BUFFER n EXTENDED IDENTIFIER REGISTERS, HIGH BYTE [$0 \leq n \leq 1$]

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
EID15	EID14	EID13	EID12	EID11	EID10	EID9	EID8
bit 7						bit 0	

- bit 7-0 **EID15:EID8:** Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

REGISTER 23-18: RXBnEIDL: RECEIVE BUFFER n EXTENDED IDENTIFIER REGISTERS, LOW BYTE [$0 \leq n \leq 1$]

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
EID7	EID6	EID5	EID4	EID3	EID2	EID1	EID0
bit 7						bit 0	

- bit 7-0 **EID7:EID0:** Extended Identifier bits

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

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REGISTER 23-45: RXFCONn: RECEIVE FILTER CONTROL REGISTER n [0 ≤ n ≤ 1]⁽¹⁾

RXFCON0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RXF7EN	RXF6EN	RXF5EN	RXF4EN	RXF3EN	RXF2EN	RXF1EN	RXF0EN

RXFCON1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
	RXF15EN	RXF14EN	RXF13EN	RXF12EN	RXF11EN	RXF10EN	RXF9EN	RXF8EN

bit 7

bit 0

bit 7-0 **RXF_nEN:** Receive Filter n Enable bits

0 = Filter is disabled

1 = Filter is enabled

Note 1: This register is available in Mode 1 and 2 only.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

Note: Registers 23-46 through 23-51 are writable in Configuration mode only.

REGISTER 23-46: SDFLC: STANDARD DATA BYTES FILTER LENGTH COUNT REGISTER⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FLC4	FLC3	FLC2	FLC1	FLC0

bit 7

bit 0

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **FLC4:FLC0:** Filter Length Count bits

Mode 0:

Not used; forced to '00000'.

00000-10010 = 0

18 bits are available for standard data byte filter. Actual number of bits used depends on DLC3:DLC0 bits (RXBnDLC<3:0> or BnDLC<3:0> if configured as RX buffer) of message being received.

If DLC3:DLC0 = 0000 No bits will be compared with incoming data bits

If DLC3:DLC0 = 0001 Up to 8 data bits of RXFnEID<7:0>, as determined by FLC2:FLC0, will be compared with the corresponding number of data bits of the incoming message

If DLC3:DLC0 = 0010 Up to 16 data bits of RXFnEID<15:0>, as determined by FLC3:FLC0, will be compared with the corresponding number of data bits of the incoming message

If DLC3:DLC0 = 0011 Up to 18 data bits of RXFnEID<17:0>, as determined by FLC4:FLC0, will be compared with the corresponding number of data bits of the incoming message

Note 1: This register is available in Mode 1 and 2 only.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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23.9 Baud Rate Setting

All nodes on a given CAN bus must have the same nominal bit rate. The CAN protocol uses Non-Return-to-Zero (NRZ) coding which does not encode a clock within the data stream. Therefore, the receive clock must be recovered by the receiving nodes and synchronized to the transmitter's clock.

As oscillators and transmission time may vary from node to node, the receiver must have some type of Phase Lock Loop (PLL) synchronized to data transmission edges to synchronize and maintain the receiver clock. Since the data is NRZ coded, it is necessary to include bit stuffing to ensure that an edge occurs at least every six bit times to maintain the Digital Phase Lock Loop (DPLL) synchronization.

The bit timing of the PIC18F2585/2680/4585/4680 is implemented using a DPLL that is configured to synchronize to the incoming data and provides the nominal timing for the transmitted data. The DPLL breaks each bit time into multiple segments made up of minimal periods of time called the *Time Quanta* (TQ).

Bus timing functions executed within the bit time frame, such as synchronization to the local oscillator, network transmission delay compensation and sample point positioning, are defined by the programmable bit timing logic of the DPLL.

All devices on the CAN bus must use the same bit rate. However, all devices are not required to have the same master oscillator clock frequency. For the different clock frequencies of the individual devices, the bit rate has to be adjusted by appropriately setting the baud rate prescaler and number of Time Quanta in each segment.

The *Nominal Bit Rate* is the number of bits transmitted per second, assuming an ideal transmitter with an ideal oscillator, in the absence of resynchronization. The nominal bit rate is defined to be a maximum of 1 Mb/s.

The *Nominal Bit Time* is defined as:

EQUATION 23-1:

$$T_{BIT} = 1/\text{Nominal Bit Rate}$$

The Nominal Bit Time can be thought of as being divided into separate, non-overlapping time segments. These segments (Figure 23-4) include:

- Synchronization Segment (Sync_Seg)
- Propagation Time Segment (Prop_Seg)
- Phase Buffer Segment 1 (Phase_Seg1)
- Phase Buffer Segment 2 (Phase_Seg2)

The time segments (and thus the Nominal Bit Time) are in turn made up of integer units of time called Time Quanta or TQ (see Figure 23-4). By definition, the Nominal Bit Time is programmable from a minimum of 8 TQ to a maximum of 25 TQ. Also by definition, the minimum Nominal Bit Time is 1 μ s, corresponding to a maximum 1 Mb/s rate. The actual duration is given by the following relationship.

EQUATION 23-2:

$$\text{Nominal Bit Time} = TQ * (\text{Sync_Seg} + \text{Prop_Seg} + \text{Phase_Seg1} + \text{Phase_Seg2})$$

The Time Quantum is a fixed unit derived from the oscillator period. It is also defined by the programmable baud rate prescaler, with integer values from 1 to 64, in addition to a fixed divide-by-two for clock generation. Mathematically, this is:

EQUATION 23-3:

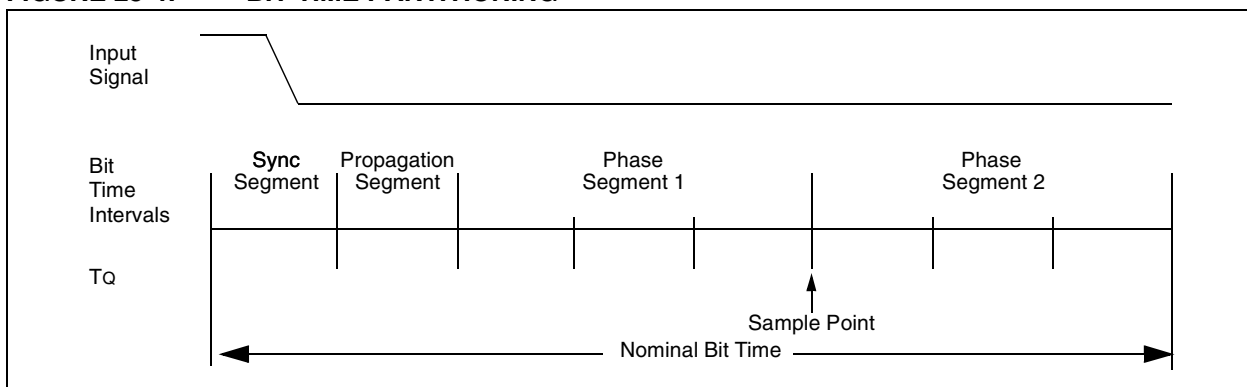
$$TQ (\mu s) = (2 * (BRP + 1)) / F_{OSC} (\text{MHz})$$

or

$$TQ (\mu s) = (2 * (BRP + 1)) * T_{OSC} (\mu s)$$

where F_{OSC} is the clock frequency, T_{OSC} is the corresponding oscillator period and BRP is an integer (0 through 63) represented by the binary values of BRGCON1<5:0>. The equation above refers to the effective clock frequency used by the microcontroller. If, for example, a 10 MHz crystal in HS mode is used, then the $F_{OSC} = 10 \text{ MHz}$ and $T_{OSC} = 100 \text{ ns}$. If the same 10 MHz crystal is used in HS-PLL mode, then the effective frequency is $F_{OSC} = 40 \text{ MHz}$ and $T_{OSC} = 25 \text{ ns}$.

FIGURE 23-4: BIT TIME PARTITIONING



PIC18F2585/2680/4585/4680

BTFSC Bit Test File, Skip if Clear

Syntax:	BTFSC f, b {,a}				
Operands:	$0 \leq f \leq 255$ $0 \leq b \leq 7$ $a \in [0,1]$				
Operation:	skip if ($f < b$) = 0				
Status Affected:	None				
Encoding:	<table><tr><td>1011</td><td>bbba</td><td>ffff</td><td>ffff</td></tr></table>	1011	bbba	ffff	ffff
1011	bbba	ffff	ffff		
Description:	If bit 'b' in register 'f' is '0', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 25.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.				
Words:	1				
Cycles:	1(2)				
	Note: 3 cycles if skip and followed by a 2-word instruction.				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```

HERE    BTFSC    FLAG, 1, 0
FALSE   :
TRUE    :
```

Before Instruction

PC = address (HERE)

After Instruction

```

If FLAG<1> = 0;
PC = address (TRUE)
If FLAG<1> = 1;
PC = address (FALSE)
```

BTFSS Bit Test File, Skip if Set

Syntax:	BTFSS f, b {,a}			
Operands:	$0 \leq f \leq 255$ $0 \leq b < 7$ $a \in [0,1]$			
Operation:	skip if ($f < b$) = 1			
Status Affected:	None			
Encoding:	1010	bbba	ffff	ffff
Description:	If bit 'b' in register 'f' is '1', then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See Section 25.2.3 “Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode” for details.			
Words:	1			
Cycles:	1(2)			
	Note: 3 cycles if skip and followed by a 2-word instruction.			

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:

```

HERE    BTFSS    FLAG, 1, 0
FALSE   :
TRUE    :
```

Before Instruction

PC = address (HERE)

After Instruction

```

If FLAG<1> = 0;
PC = address (FALSE)
If FLAG<1> = 1;
PC = address (TRUE)
```

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SLEEP Enter Sleep mode

Syntax:	SLEEP				
Operands:	None				
Operation:	00h → WDT, 0 → WDT postscaler, 1 → $\overline{TO}$, 0 → $\overline{PD}$				
Status Affected:	$\overline{TO}$, $\overline{PD}$				
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0000</td><td>0011</td></tr></table>	0000	0000	0000	0011
0000	0000	0000	0011		
Description:	The Power-Down status bit ($\overline{PD}$) is cleared. The Time-out status bit ($\overline{TO}$) is set. Watchdog Timer and its postscaler are cleared. The processor is put into Sleep mode with the oscillator stopped.				
Words:	1				
Cycles:	1				
Q Cycle Activity:					

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	Go to Sleep

Example: SLEEP

Before Instruction

$\overline{TO}$ = ?

PD = ?

After Instruction

$\overline{TO}$ = 1 †

PD = 0

† If WDT causes wake-up, this bit is cleared.

SUBFWB Subtract f from W with Borrow

Syntax:	SUBFWB f {,d {,a}}			
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$			
Operation:	$(W) - (f) - (\overline{C}) \rightarrow \text{dest}$			
Status Affected:	N, OV, C, DC, Z			
Encoding:	0101	01da	ffff	ffff
Description:	Subtract register 'f' and Carry flag			

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See

Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: SUBFWB REG, 1, 0

Before Instruction

REG = 3

W = 2

C = 1

After Instruction

REG = FF

W = 2

C = 0

Z = 0

N = 1 ; result is negative

Example 2: SUBFWB REG, 0, 0

Before Instruction

REG = 2

W = 5

C = 1

After Instruction

REG = 2

W = 3

C = 1

Z = 0

N = 0 ; result is positive

Example 3: SUBFWB REG, 1, 0

Before Instruction

REG = 1

W = 2

C = 0

After Instruction

REG = 0

W = 2

C = 1

Z = 1

N = 0 ; result is zero

PIC18F2585/2680/4585/4680

27.3 DC Characteristics: PIC18F2585/2680/4585/4680 (Industrial) PIC18LF2585/2680/4585/4680 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D080	VOL	Output Low Voltage I/O ports	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to $+85^{\circ}\text{C}$
D083		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to $+85^{\circ}\text{C}$
D090	VOH	Output High Voltage ⁽³⁾ I/O ports	VDD – 0.7	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to $+85^{\circ}\text{C}$
D092		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	VDD – 0.7	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to $+85^{\circ}\text{C}$
D100 ⁽⁴⁾	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	50	pF	To meet the AC Timing Specifications
D102	CB	SCL, SDA	—	400	pF	I ² C™ Specification

- Note 1:** In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.
- 2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** Parameter is characterized but not tested.

PIC18F2585/2680/4585/4680

TABLE 27-1: MEMORY PROGRAMMING REQUIREMENTS

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
Internal Program Memory Programming Specifications⁽¹⁾							
D110	VPP	Voltage on $\overline{\text{MCLR}}/\text{VPP}/\text{RE3}$ pin	9.00	—	13.25	V	(Note 3)
D113	IDDP	Supply Current during Programming	—	—	10	mA	
Data EEPROM Memory							
D120	ED	Byte Endurance	100K	1M	—	E/W	-40°C to $+85^{\circ}\text{C}$ Using EECON to read/write V_{MIN} = Minimum operating voltage
D121	VDRW	VDD for Read/Write	V_{MIN}	—	5.5	V	
D122	TDEW	Erase/Write Cycle Time	—	4	—	ms	Provided no other specifications are violated
D123	TRETD	Characteristic Retention	40	—	—	Year	
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽²⁾	1M	10M	—	E/W	
Program Flash Memory							
D130	EP	Cell Endurance	10K	100K	—	E/W	-40°C to $+85^{\circ}\text{C}$ V_{MIN} = Minimum operating voltage
D131	VPR	VDD for Read	V_{MIN}	—	5.5	V	
D132	VIE	VDD for Block Erase	4.5	—	5.5	V	Using ICSP™ port
D132A	VIW	VDD for Externally Timed Erase or Write	4.5	—	5.5	V	Using ICSP port
D132B	VPEW	VDD for Self-timed Write	V_{MIN}	—	5.5	V	V_{MIN} = Minimum operating voltage
D133	TIE	ICSP Block Erase Cycle Time	—	4	—	ms	$V_{\text{DD}} > 4.5\text{V}$
D133A	TIW	ICSP Erase or Write Cycle Time (externally timed)	1	—	—	ms	$V_{\text{DD}} > 4.5\text{V}$
D133A	TIW	Self-timed Write Cycle Time	—	2	—	ms	
D134	TRETD	Characteristic Retention	40	100	—	Year	Provided no other specifications are violated

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of table write instructions.

2: Refer to **Section 7.8 “Using the Data EEPROM”** for a more detailed discussion on data EEPROM endurance.

3: Required only if Single-Supply Programming is disabled.

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TABLE 27-7: PLL CLOCK TIMING SPECIFICATIONS (V_{DD} = 4.2V TO 5.5V)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
F10	FOSC	Oscillator Frequency Range	4	—	10	MHz	HS mode only
F11	FSYS	On-Chip VCO System Frequency	16	—	40	MHz	HS mode only
F12	t _{rc}	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13	ΔCLK	CLKO Stability (Jitter)	-2	—	+2	%	

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 27-8: AC CHARACTERISTICS: INTERNAL RC ACCURACY
PIC18F2585/2680/4585/4680 (INDUSTRIAL)
PIC18LF2585/2680/4585/4680 (INDUSTRIAL)

PIC18LF2585/2680/4585/4680 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial						
PIC18F2585/2680/4585/4680 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial						
Param No.	Device	Min	Typ	Max	Units	Conditions		
	INTOSC Accuracy @ Freq = 8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz⁽¹⁾							
	PIC18LFX585/X680	-2	+/-1	2	%	+25°C	VDD = 2.7-3.3V	
		-5	—	5	%	-10°C to +85°C	VDD = 2.7-3.3V	
		-10	+/-1	10	%	-40°C to +85°C	VDD = 2.7-3.3V	
	PIC18FX585/X680	-2	+/-1	2	%	+25°C	VDD = 4.5-5.5V	
		-5	—	5	%	-10°C to +85°C	VDD = 4.5-5.5V	
		-10	+/-1	10	%	-40°C to +85°C	VDD = 4.5-5.5V	
		INTRC Accuracy @ Freq = 31 kHz⁽²⁾						
PIC18LFX585/X680		26.562	—	35.938	kHz	-40°C to +85°C	VDD = 2.7-3.3V	
PIC18FX585/X680		26.562	—	35.938	kHz	-40°C to +85°C	VDD = 4.5-5.5V	

Legend: Shading of rows is to assist in readability of the table.

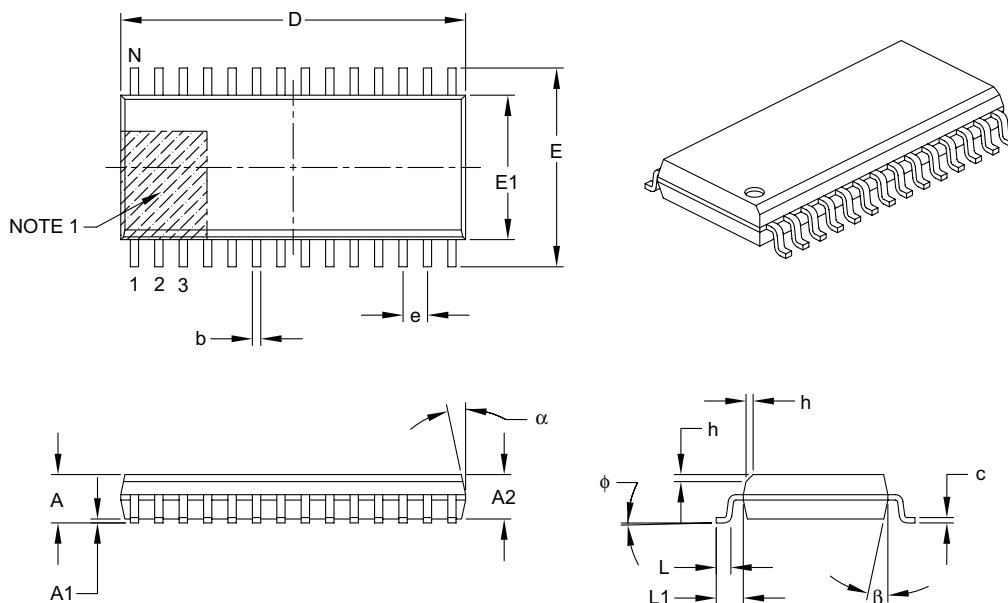
Note 1: Frequency calibrated at 25°C. OSC_{TUNE} register can be used to compensate for temperature drift.

2: INTRC frequency after calibration.

PIC18F2585/2680/4585/4680

28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1	1.40 REF		
Foot Angle Top	φ	0°	–	8°
Lead Thickness	c	0.18	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B

PIC18F2585/2680/4585/4680

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RB7/KBI3/PGD	14, 18
RC0/T1OSO/T13CKI	15, 19
RC1/T1OSI	15, 19
RC2/CCP1	15, 19
RC3/SCK/SCL	15, 19
RC4/SDI/SDA	15, 19
RC5/SDO	15, 19
RC6/TX/CK	15, 19
RC7/RX/DT	15, 19
RD0/PSP0/C1IN+	20
RD1/PSP1/C1IN-	20
RD2/PSP2/C2IN+	20
RD3/PSP3/C2IN-	20
RD4/PSP4/ECCP1/P1A	20
RD5/PSP5/P1B	20
RD6/PSP6/P1C	20
RD7/PSP7/P1D	20
RE0/RD/AN5	21
RE1/WR/AN6/C1OUT	21
RE2/CS/AN7/C2OUT	21
VDD	15, 21
VSS	15, 21