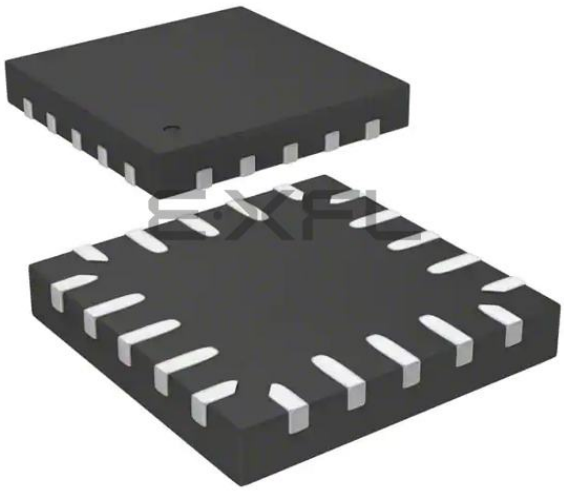
STMicroelectronics - STM8L101F1U6ATR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f1u6atr

3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It features 21 internal registers, 20 addressing modes including indexed, indirect and relative addressing, and 80 instructions.

3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

3.4 Interrupt controller

The STM8L101xx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 26 interrupt vectors with hardware priority
- Up to 29 external interrupt sources on 10 vectors
- Trap and reset interrupts.

3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

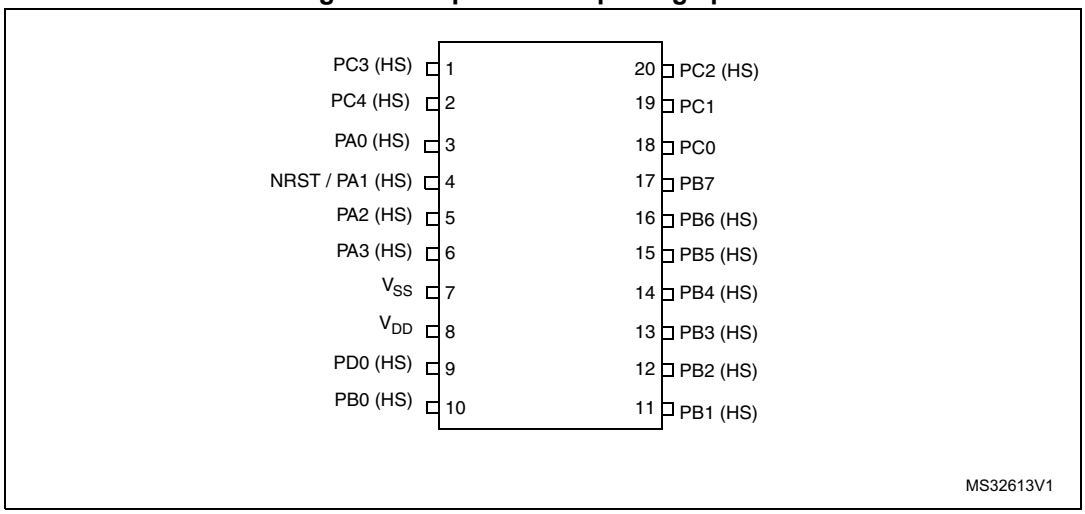
3.16 SPI

The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices. It can be configured as the master and in this case it provides the communication clock (SCK) to the external slave device. The interface can also operate in multi-master configuration.

3.17 I²C

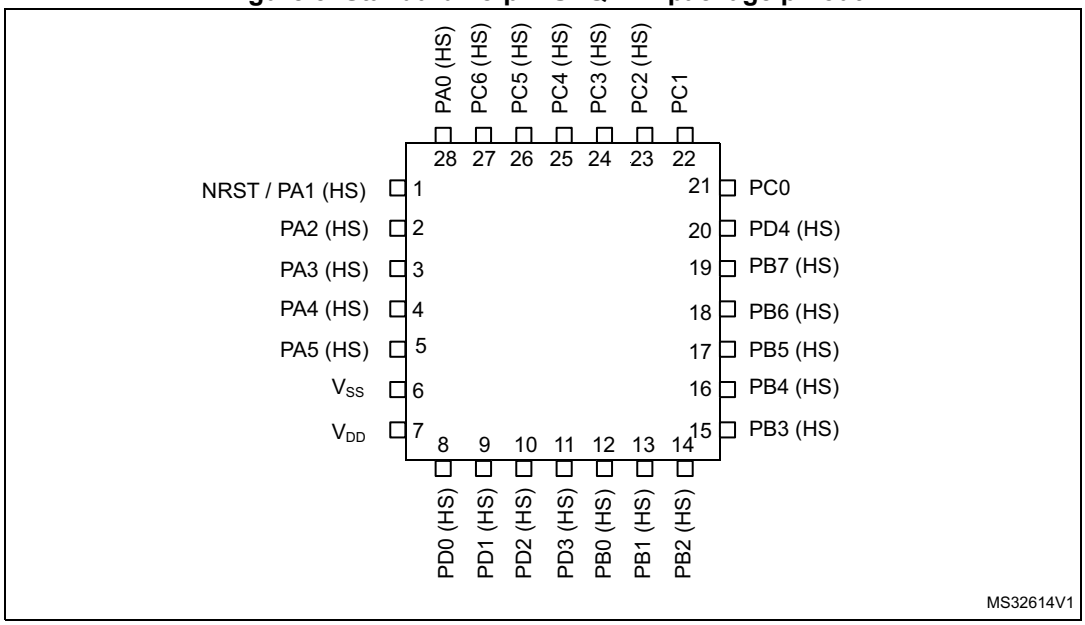
The inter-integrated circuit (I2C) bus interface is designed to serve as an interface between the microcontroller and the serial I^2C bus. It provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It manages standard and fast speed modes.

Figure 4. 20-pin TSSOP package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Figure 5. Standard 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 28-pin UFQFPN package. It is available on Port A6 in the Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers.

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	26	26	30	PC5	I/O	**X**	X	X	HS	X	X	**Port C5**	-
-	-	-	27	27	31	PC6	I/O	**X**	X	X	HS	X	X	**Port C6**	-
20	20	3	28	28	32	PA0(5)/SWIM/ BEEP/IR_TIM (6)	I/O	X	**X**(5)	X	HS(6)	X	X	**Port A0**	SWIM input and output /Beep output/Timer Infrared output

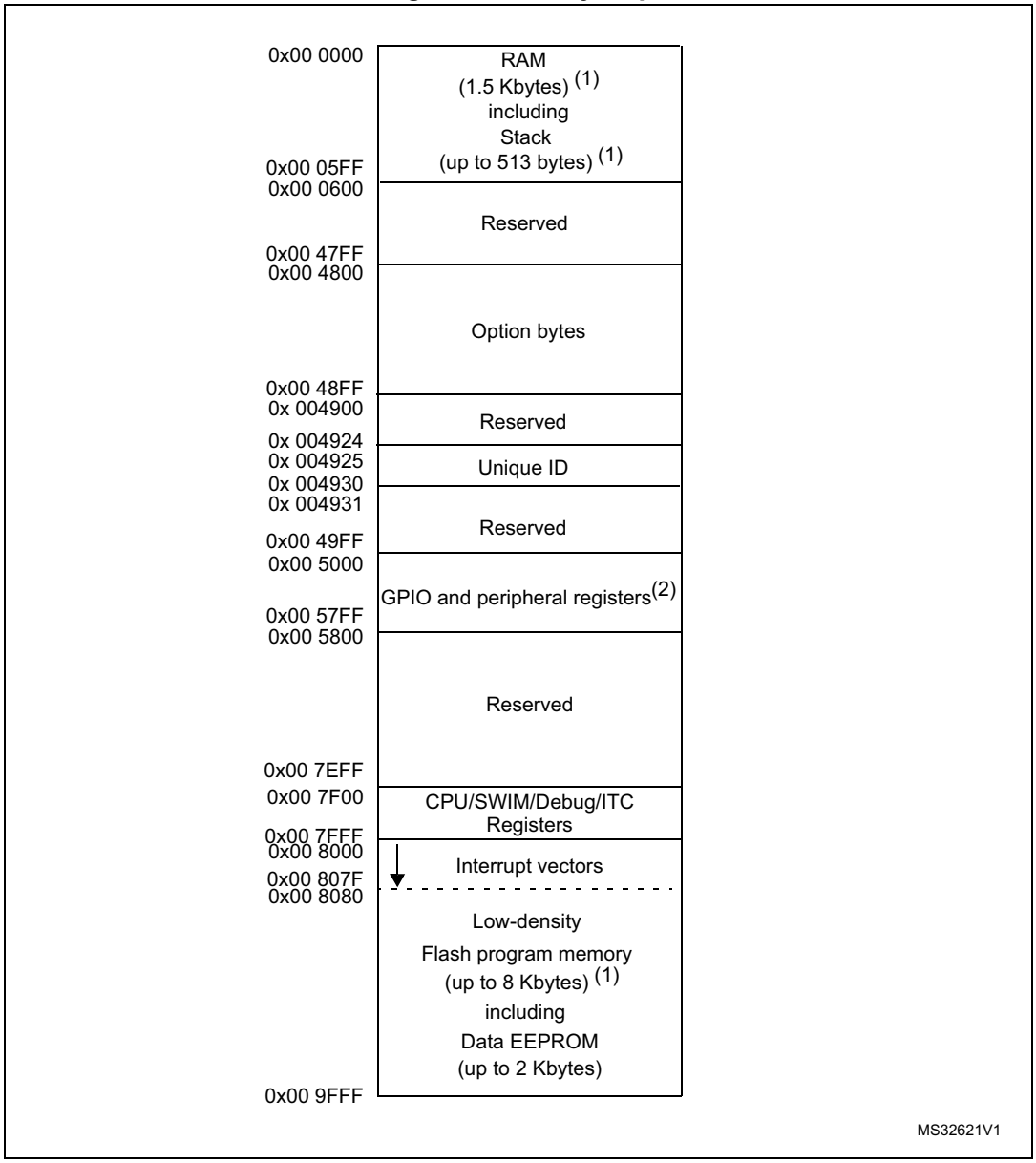
1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

5 Memory and register map

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0xX0
0x00 5055 to 0x00 509F	Reserved area (75 bytes)			
0x00 50A0	ITC-EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF	External interrupt port select register	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8 to 0x00 50AF	Reserved area (8 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2 to 0x00 50BF	Reserved area (14 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	Clock divider register	0x03
0x00 50C1 to 0x00 50C2		Reserved area (2 bytes)		
0x00 50C3		CLK_PCKENR	Peripheral clock gating register	0x00
0x00 50C4		Reserved (1 byte)		
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6 to 0x00 50DF	Reserved area (25 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5285		TIM3_SR1	TIM3 status register 1	0x00
0x00 5286		TIM3_SR2	TIM3 status register 2	0x00
0x00 5287		TIM3_EGR	TIM3 event generation register	0x00
0x00 5288		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5289		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 528A		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 528B		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528C		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528D		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528E		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 528F		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 5290		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 5291		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 5292		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5293		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5294		TIM3_BKR	TIM3 break register	0x00
0x00 5295		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5296 to 0x00 52DF	Reserved area (74 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E4		TIM4_SR1	TIM4 Status register 1	0x00
0x00 52E5		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E6		TIM4_CNTR	TIM4 counter	0x00
0x00 52E7		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E8		TIM4_ARR	TIM4 auto-reload register low	0xFF

Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	-25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	-5	
	Injected current on any other pin (2)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	±25	

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Total current consumption in Run mode (1)

Symbol	Parameter	Conditions(2)		Typ	Max(3)	Unit
$I_{DD\ (Run)}$	Supply current in Run mode(4) (5)	Code executed from RAM	f_{MASTER} = 2 MHz	0.39	0.60	mA
			f_{MASTER} = 4 MHz	0.55	0.70	
			f_{MASTER} = 8 MHz	0.90	1.20	
			f_{MASTER} = 16 MHz	1.60	2.10(6)	
		Code executed from Flash	f_{MASTER} = 2 MHz	0.55	0.70	
			f_{MASTER} = 4 MHz	0.88	1.80	
			f_{MASTER} = 8 MHz	1.50	2.50	
			f_{MASTER} = 16 MHz	2.70	3.50	

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{MASTER}$
3. Maximum values are given for T_A = –40 to 125 °C.
4. CPU executing typical data processing.
5. An approximate value of $I_{DD(Run)}$ can be given by the following formula: $I_{DD(Run)} = f_{MASTER}$ x 150 µA/MHz +215 µA.
6. Tested in production.

Figure 11. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 2 MHz

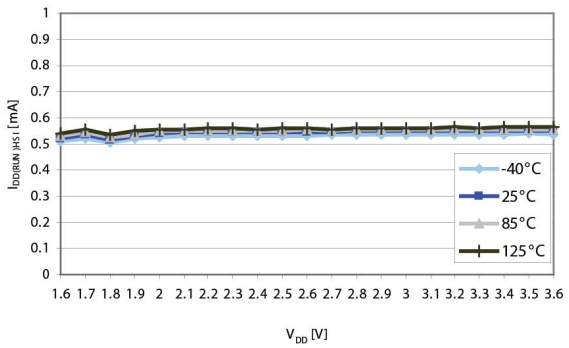
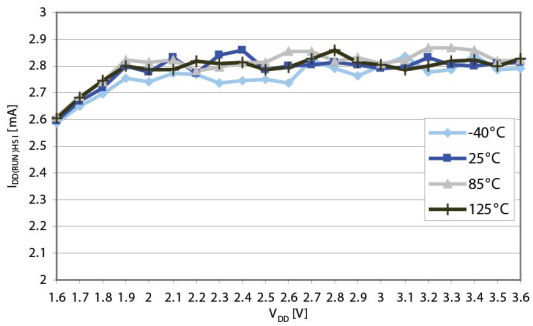


Figure 12. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Current consumption of on-chip peripherals

Measurement made for f_{MASTER} = from 2 MHz to 16 MHz

Table 21. Peripheral current consumption

Symbol	Parameter	Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM2)}$	TIM2 supply current (1)	9	µA/MHz
$I_{DD(TIM3)}$	TIM3 supply current (1)	9	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)	4	
$I_{DD(USART)}$	USART supply current (2)	7	
$I_{DD(SPI)}$	SPI supply current (2)	4	
$I_{DD(I^2C1)}$	I2C supply current (2)	4	
$I_{DD(COMP)}$	Comparator supply current (2)	20	µA

1. Data based on a differential I_{DD} measurement between all peripherals off and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pin toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pin toggling. Not tested in production.

9.3.4 Clock and timing characteristics

Internal clock sources

Subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator (HSI)

Table 22. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1	-	1	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 85 °C	-2.5(2)	-	2(2)	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 125 °C	-4.5(2)	-	2(2)	%
		V_{DD} = 3.0 V, 0 °C ≤T_A ≤ 55 °C	-1.5(2)	-	1.5(2)	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 70 °C	-2(2)	-	2(2)	%
		1.65 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤125 °C	-4.5(2)	-	3(2)	%
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	70	100(2)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.

Figure 16. Typical HSI frequency vs. V_{DD}

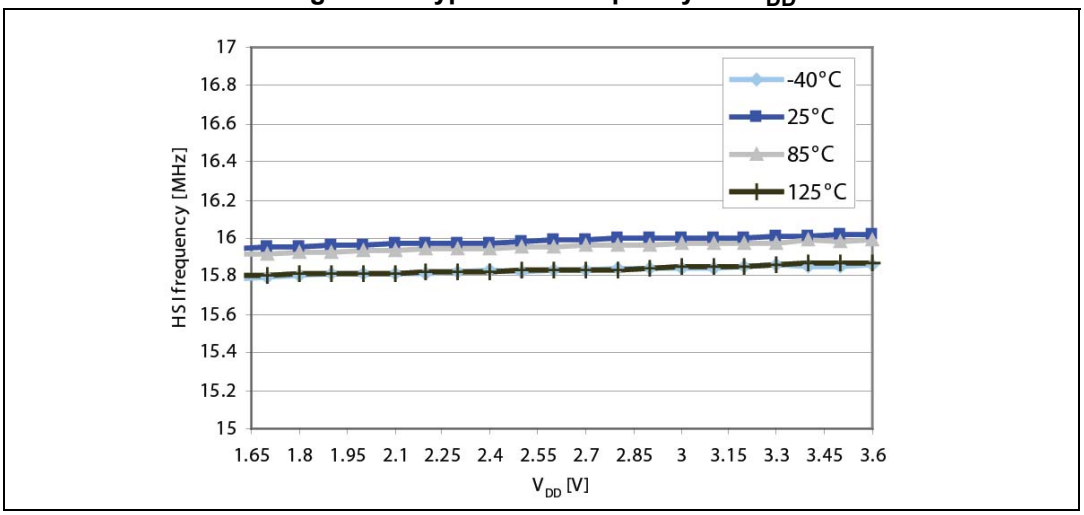


Figure 17. Typical HSI accuracy vs. temperature, V_{DD} = 3 V

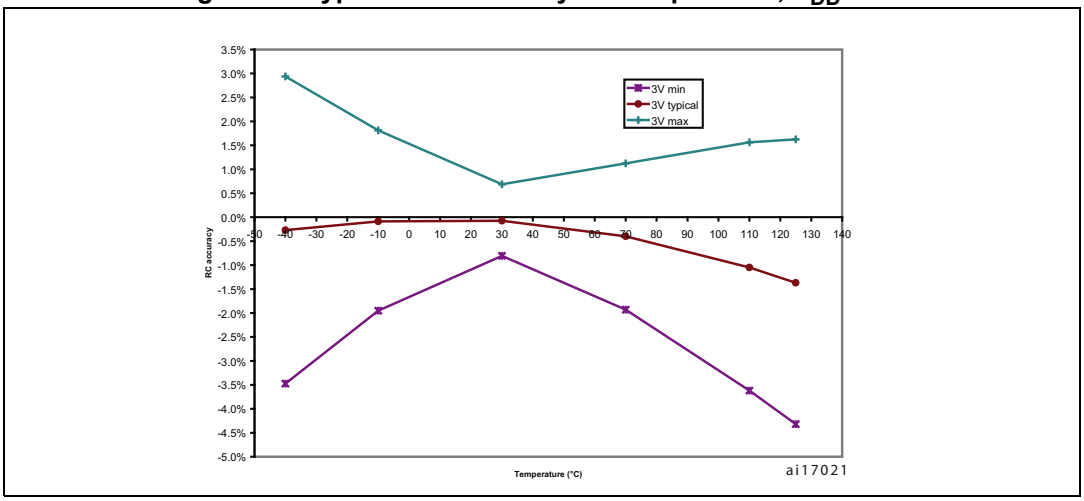


Figure 18. Typical HSI accuracy vs. temperature, V_{DD} = 1.65 V to 3.6 V

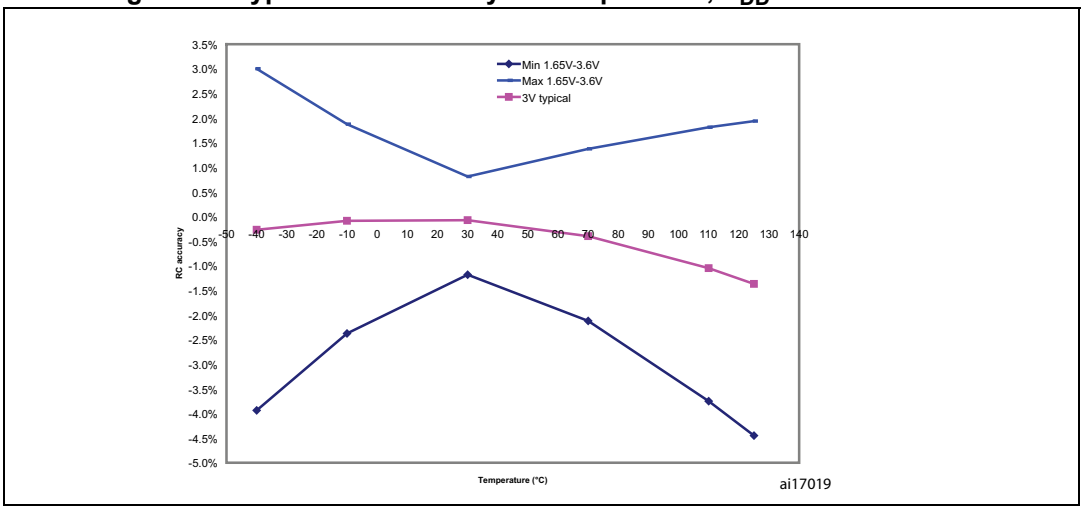


Table 25. Flash program memory (continued)

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET}	Data retention (program memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	years
	Data retention (data memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	
	Data retention (data memory) after 300k erase/write cycles at T_A = +125 °C	T_{RET} = 85 °C	1(1)	-	-	
N_{RW}	Erase/write cycles (program memory)	See notes (1)(2)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)	See notes (1)(3)	300(1)(4)	-	-	

1. Data based on characterization results, not tested in production.
2. Retention guaranteed after cycling is 10 years at 55 °C.
3. Retention guaranteed after cycling is 1 year at 55 °C.
4. Data based on characterization performed on the whole data memory (2 Kbytes).

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 26. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Standard I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	V
		True open drain I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Standard I/Os	0.70 x V_{DD}	-	V_{DD}+0.3	V
		True open drain I/Os V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		True open drain I/Os V_{DD} ≥ 2 V			5.5	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	250	-	

Figure 33. SPI timing diagram - slave mode and CPHA = 0

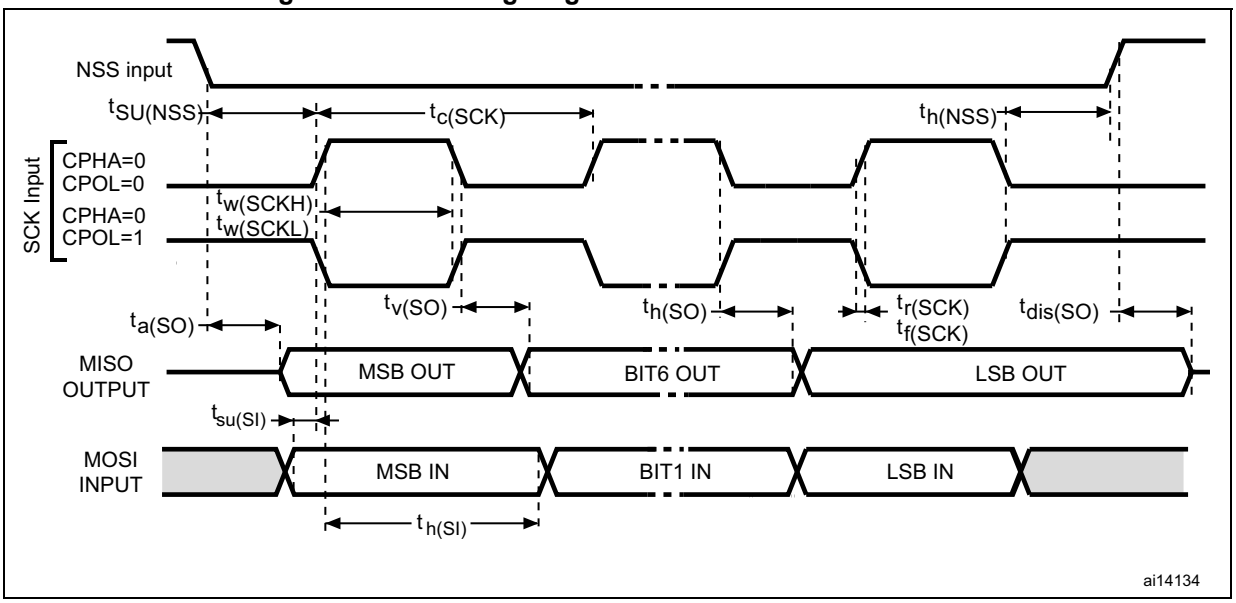
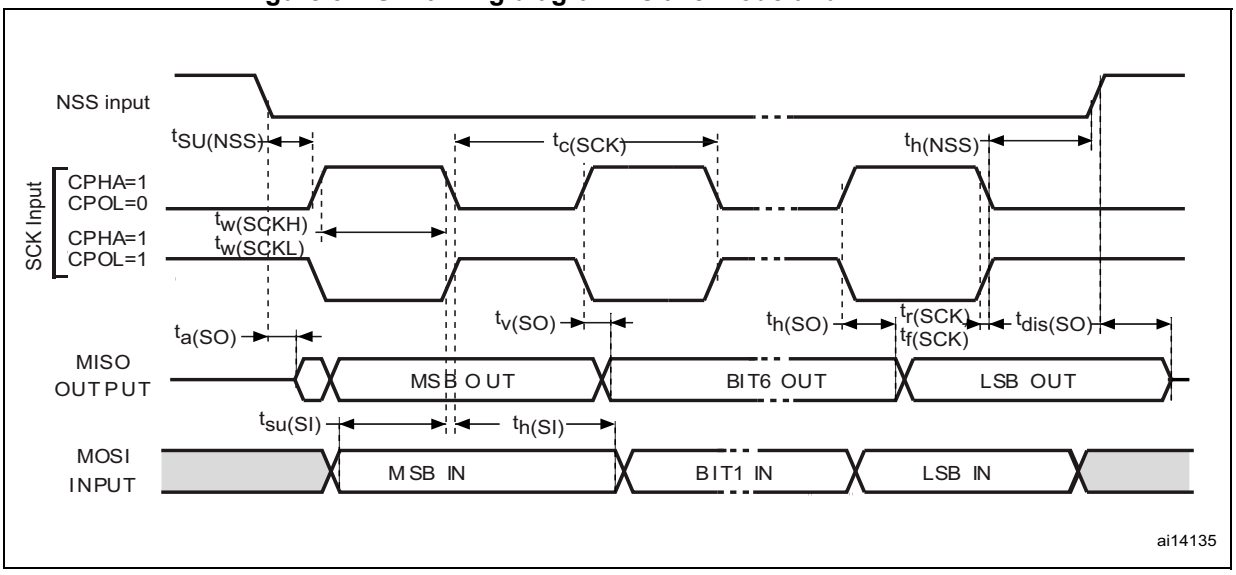
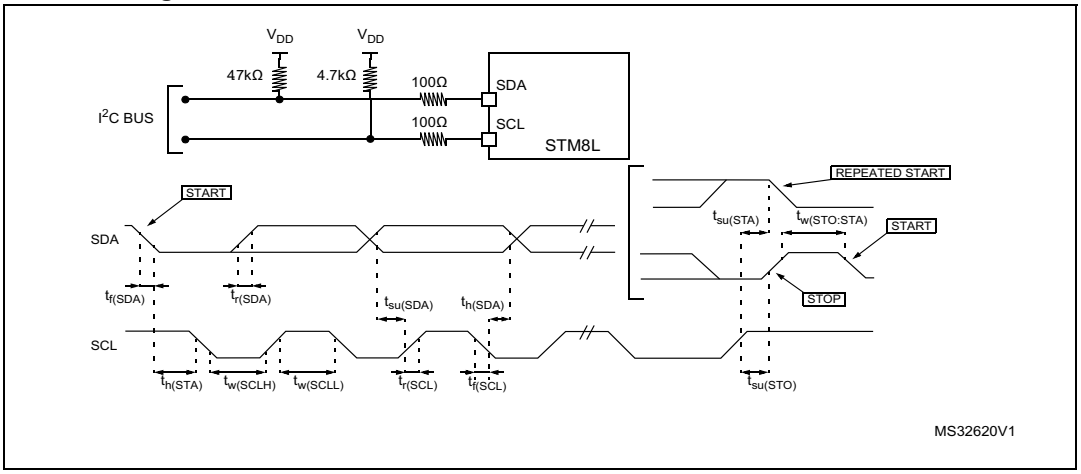


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 36. Typical application with I2C bus and timing diagram 1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

9.3.8 Comparator characteristics

Table 33. Comparator characteristics

Symbol	Parameter	Conditions	Min (1)	Typ	Max(1)	Unit
$V_{IN(COMP\_REF)}$	Comparator external reference	-	-0.1	-	V_{DD}-1.25	V
V_{IN}	Comparator input voltage range	-	-0.25	-	V_{DD}+0.25	V
V_{offset}(2)	Comparator offset error	-	-	-	±20	mV
t_{START}	Startup time (after BIAS_EN)	-	-	-	3(1)	µs
$I_{DD(COMP)}$	Analog comparator consumption	-	-	-	25(1)	µA
	Analog comparator consumption during power-down	-	-	-	60(1)	nA
t_{propag}(2)	Comparator propagation delay	100-mV input step with 5-mV overdrive, input rise time = 1 ns	-	-	2(1)	µs

1. Data guaranteed by design, not tested in production.
2. The comparator accuracy depends on the environment. In particular, the following cases may reduce the accuracy of the comparator and must be avoided:
   - Negative injection current on the I/Os close to the comparator inputs
   - Switching on I/Os close to the comparator inputs
   - Negative injection current on not used comparator input.
   - Switching with a high dV/dt on not used comparator input.

   These phenomena are even more critical when a big external serial resistor is added on the inputs.

Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 37. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 40*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 38. Thermal characteristics(1)

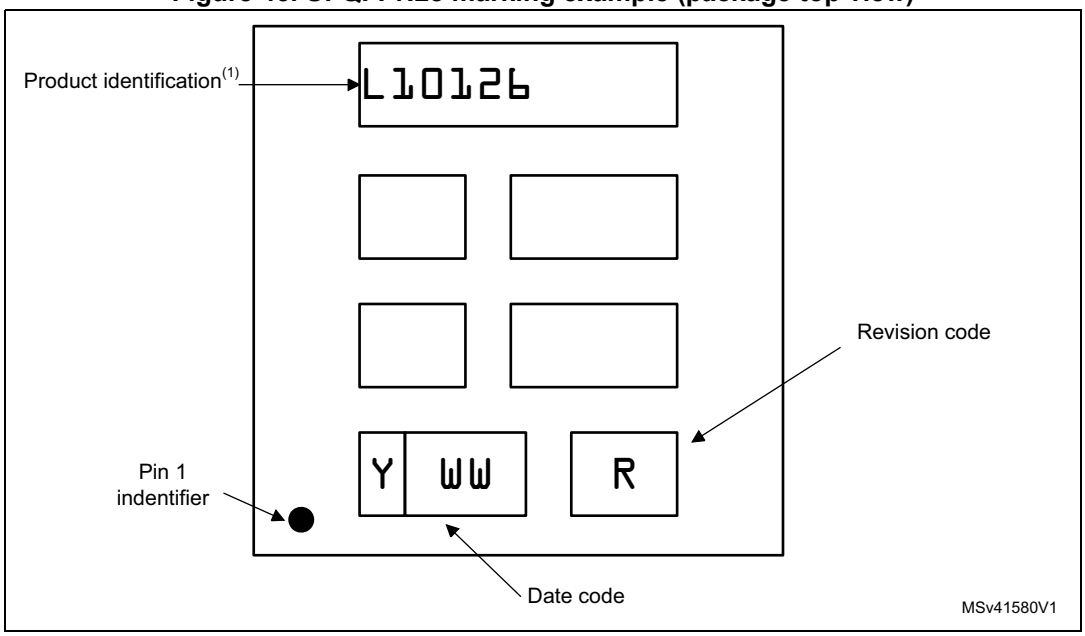
Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W
	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	25	°C/W
	Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm	80	°C/W
	Thermal resistance junction-ambient UFQFPN 20 - 3 x 3 mm - 0.6 mm	102	°C/W
	Thermal resistance junction-ambient TSSOP 20	110	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

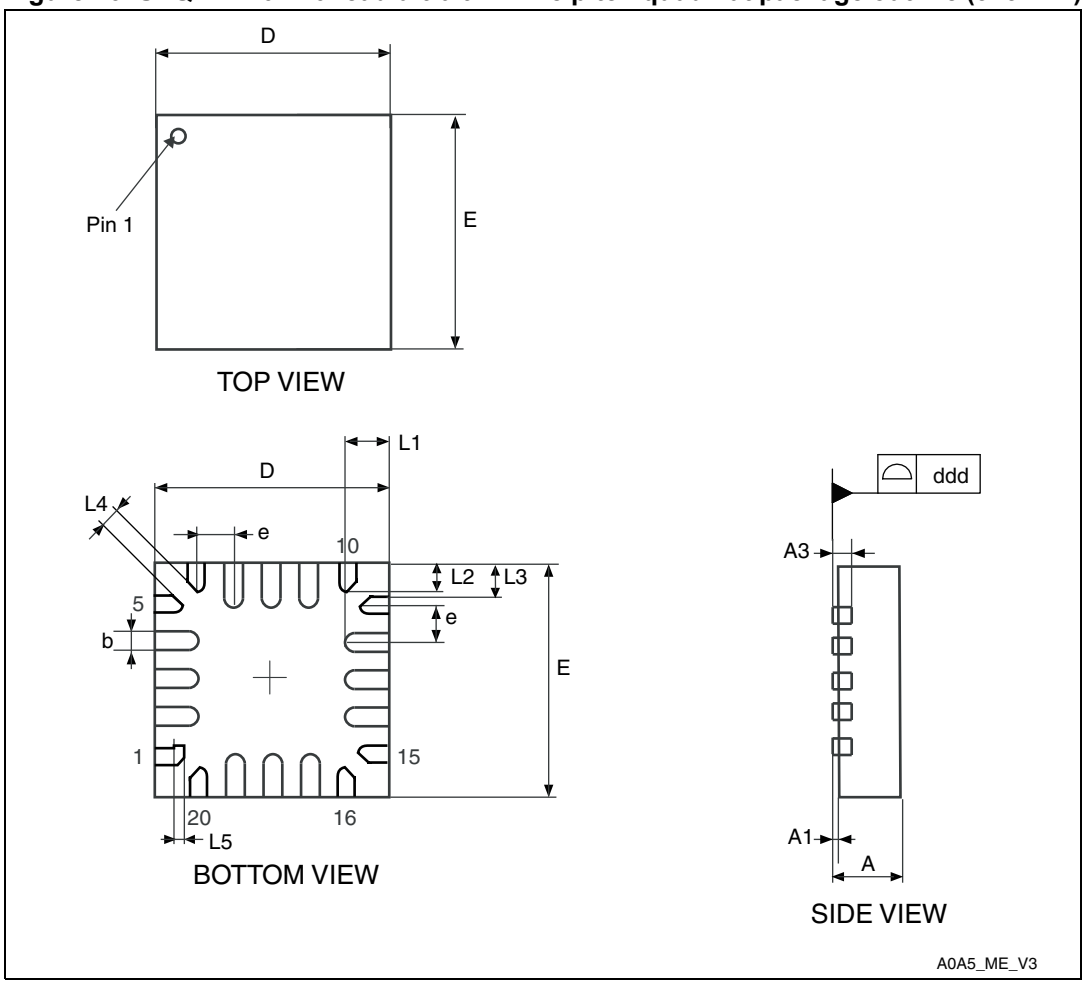
Figure 45. UFQFPN28 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.4 UFQFPN20 package information

Figure 46. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3 mm)



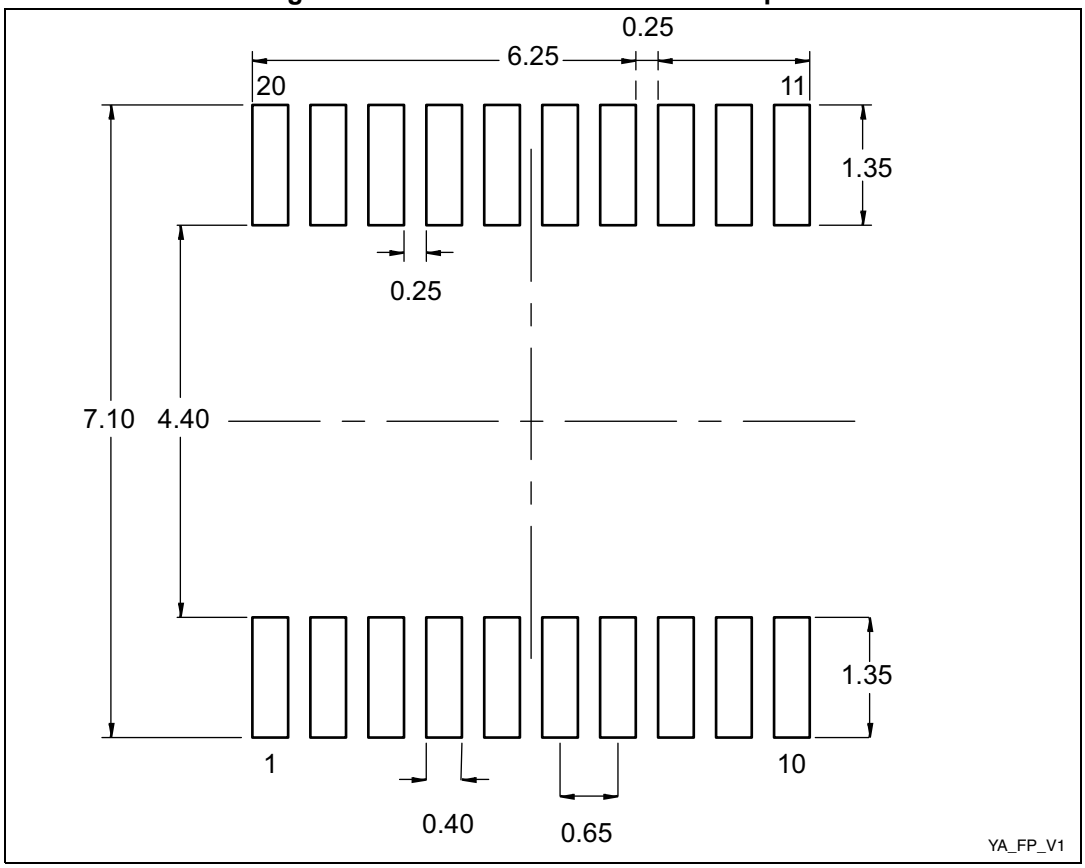
1. Drawing is not to scale.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data (continued)

Dim.	mm				inches[1]	
	Min	Typ	Max	Min	Typ	Max
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039
Number of pins	20					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 50. TSSOP20 recommended footprint



1. Dimensions are in millimeters.

Table 44. Document revision history (continued)

Date	Revision	Changes
14-Oct-2010	11	Added STM8L101F1 devices: Modified *Table 1: Device summary on page 1*, *Table 2: STM8L101xx device feature summary on page 9* and *Table 5: Flash and RAM boundary addresses on page 24* Modified warning below *Figure 3 on page 16* and below*Table 4: STM8L101xx pin description on page 20* Modified *Figure 52: STM8L101xx ordering information scheme on page 79* Modified text above *Figure 32: Recommended NRST pin configuration on page 54* Modified *Figure 32 on page 54*
02-Aug-2013	12	Added “The RAM content is preserved” in halt mode *Section 3.6: Low power modes* Reformatted *Figure 2: Standard 20-pin UFQFPN package pinout*, *Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 5: Standard 28-pin UFQFPN package pinout*, *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers* and *Figure 7: 32-pin package pinout* Corrected NRST/PA1 pin OD output capability in *Table 4: STM8L101xx pin description* and corrected note *2.* and *4.* Added note “Slope control of all GPIO can be programmed except...” in *Table 4: STM8L101xx pin description* Added note under *Table 5: Flash and RAM boundary addresses* Replaced UM0320 with UM0470 in *Section 7: Option bytes* Updated OPT2 and OPT3 in *Table 10: Option bytes* Added additional note *2.* references in *Table 22: HSI oscillator characteristics* Added note *2.* under *Table 17: Operating conditions at power-up / power-down* and under *Figure 32: Recommended NRST pin configuration* Corrected ‘SCK output’ in *Figure 35: SPI timing diagram - master mode(1)* Added top view in *Figure 43: UFQFPN20 3 x 3 mm 0.6 mm package outline* Repositioned the package layout and footprint for all packages. Replaced “Standard ports” with “High sink ports” Replaced “TIMx_TRIG” with “TIMx_ETR” Replaced all ‘"Data guaranteed, each individual device tested in production” notes with “Tested in production”
31-Mar-2014	13	Updated L3 value on *Table 42*, added note 2) and 3) on *Table 43*