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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f2p6

List of figures

3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It features 21 internal registers, 20 addressing modes including indexed, indirect and relative addressing, and 80 instructions.

3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

3.4 Interrupt controller

The STM8L101xx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 26 interrupt vectors with hardware priority
- Up to 29 external interrupt sources on 10 vectors
- Trap and reset interrupts.

3.10 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

3.11 General purpose and basic timers

STM8L101xx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Time base generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.12 Beeper

The STM8L101xx devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.13 Infrared (IR) interface

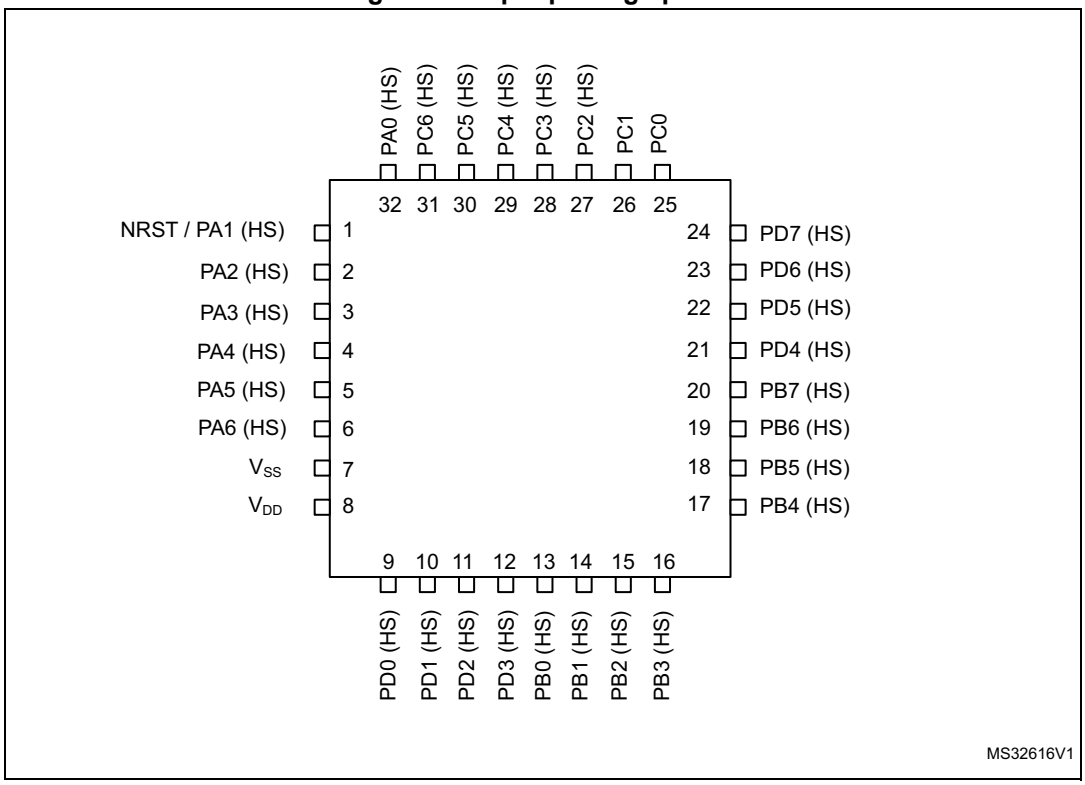
The STM8L101xx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.14 Comparators

The STM8L101xx features two zero-crossing comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal (comparison with ground) or external (comparison to a reference pin voltage).

Each comparator is connected to 4 channels, which can be used to generate interrupt, timer input capture or timer break. Their polarity can be inverted.

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0xX0
0x00 5055 to 0x00 509F	Reserved area (75 bytes)			
0x00 50A0	ITC-EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF	External interrupt port select register	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8 to 0x00 50AF	Reserved area (8 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2 to 0x00 50BF	Reserved area (14 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	Clock divider register	0x03
0x00 50C1 to 0x00 50C2		Reserved area (2 bytes)		
0x00 50C3		CLK_PCKENR	Peripheral clock gating register	0x00
0x00 50C4		Reserved (1 byte)		
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6 to 0x00 50DF	Reserved area (25 bytes)			

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Note: The values given at 85 °C <T_A ≤ 125 °C are only valid for suffix 3 versions.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

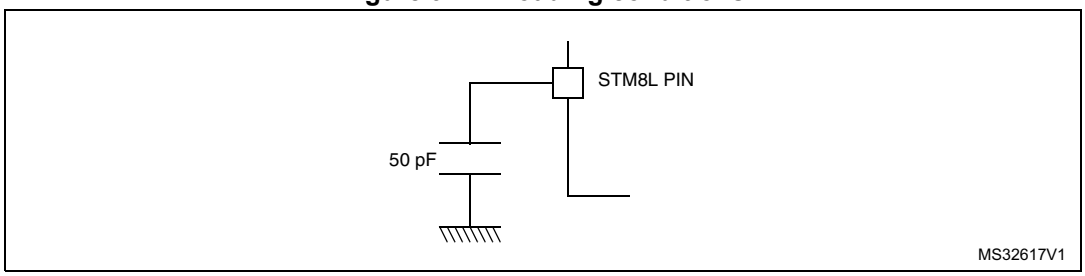
9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

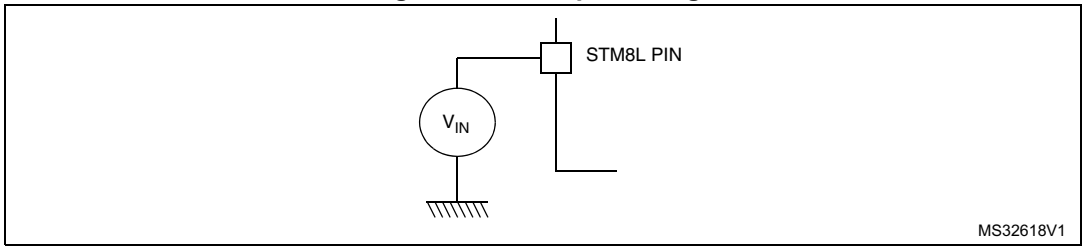
Figure 9. Pin loading conditions



9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on true open drain pins (PC0 and PC1)(1)	V_{SS}-0.3	V_{DD} + 4.0	
	Input voltage on any other pin (2)	V_{SS}-0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		-

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER} (1)	Master clock frequency	1.65 V ≤V_{DD} < 3.6 V	2	16	MHz
V_{DD}	Standard operating voltage	-	1.65	3.6	V
P_D (2)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP32	-	288	mW
		UFQFPN32	-	288	
		UFQFPN28	-	250	
		TSSOP20	-	181	
		UFQFPN20	-	196	
	Power dissipation at T_A= 125 °C for suffix 3 devices	LQFP32	-	83	
		UFQFPN32	-	185	
		UFQFPN28	-	62	
		TSSOP20	-	45	
		UFQFPN20	-	49	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)	–40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)	–40	125	
T_J	Junction temperature range	-40 °C ≤T_A ≤85 °C (6 suffix version)	- 40	105	°C
		-40 °C ≤T_A ≤125 °C (3 suffix version)	–40	130	°C

1. f_{MASTER} = f_{CPU}
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”

Figure 21. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

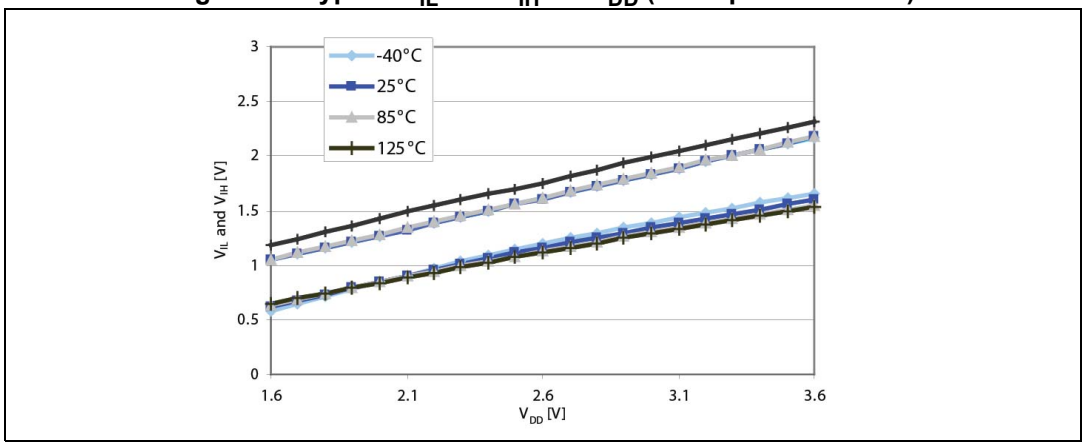


Figure 22. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

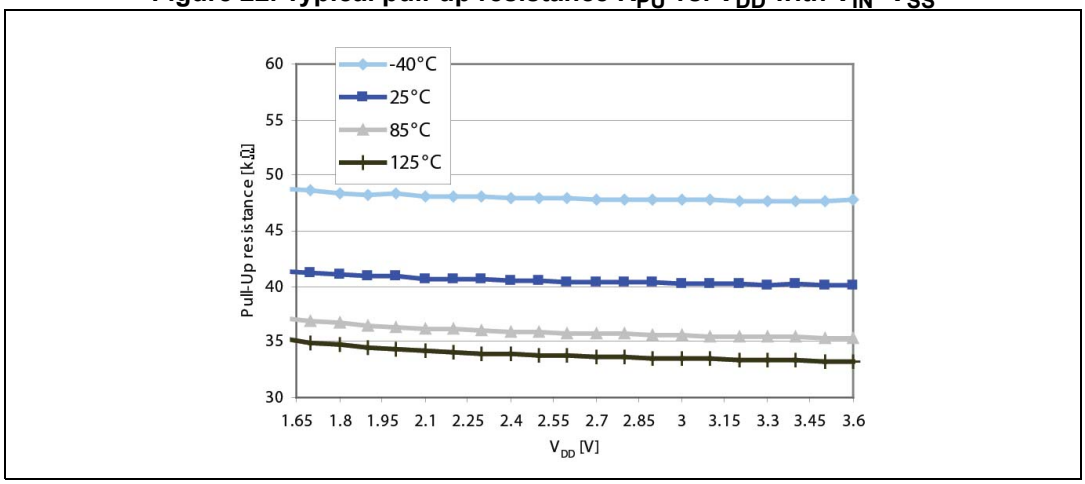


Figure 23. Typical pull-up current I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

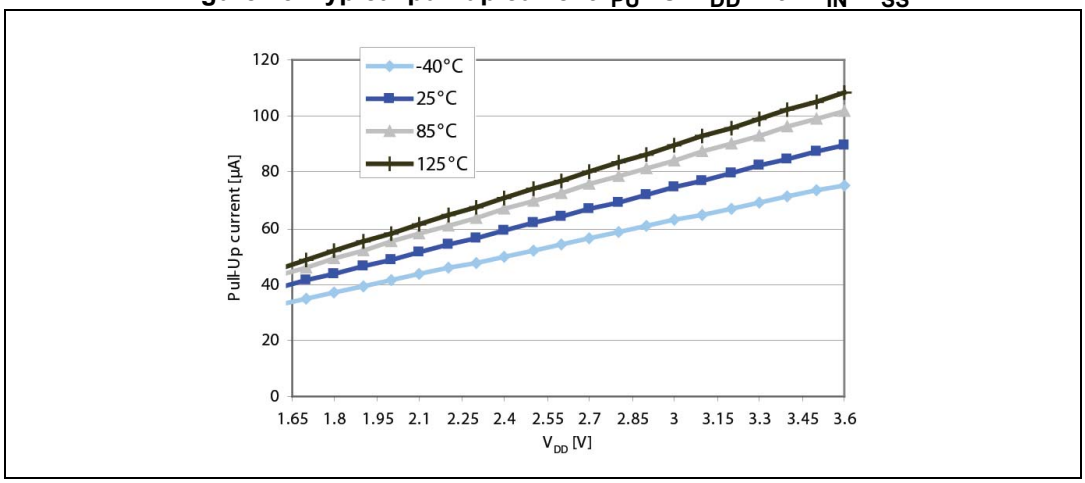
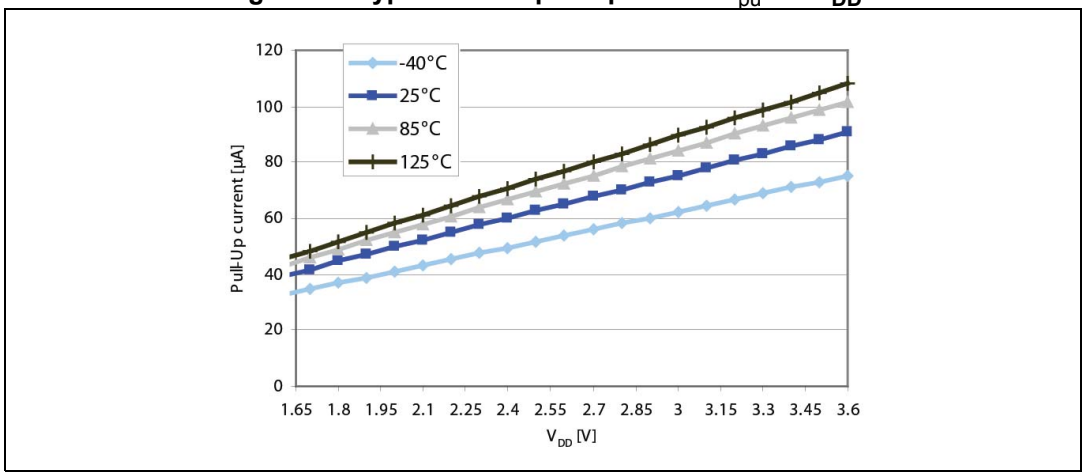
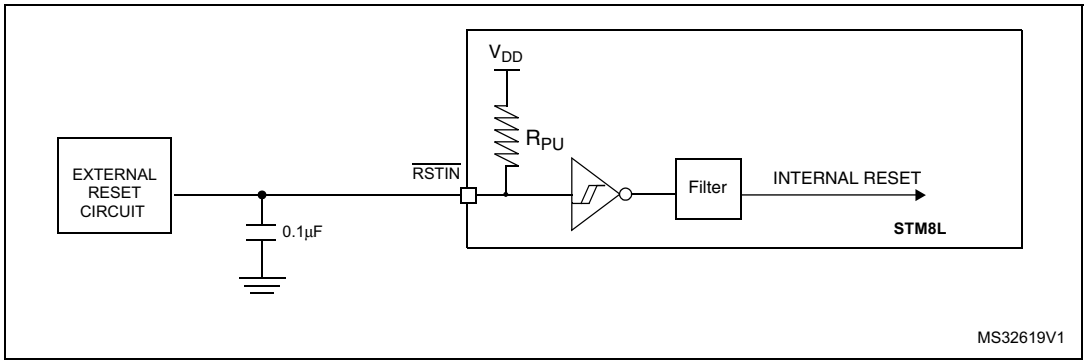


Figure 31. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 32* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 30*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 32. Recommended NRST pin configuration



1. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected.
2. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

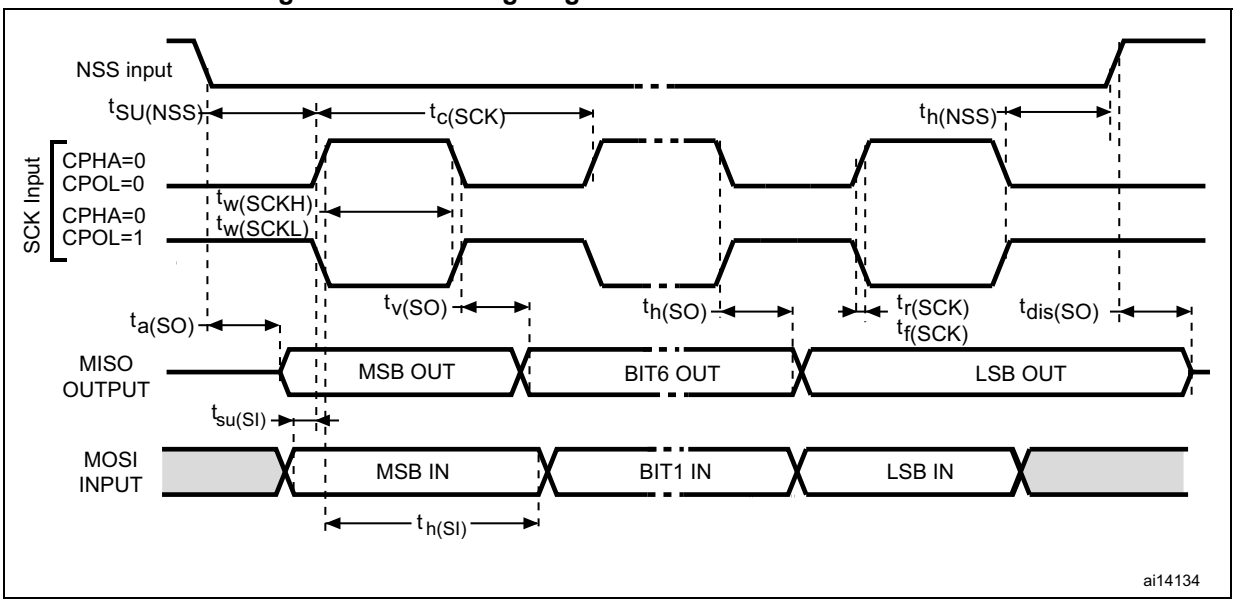
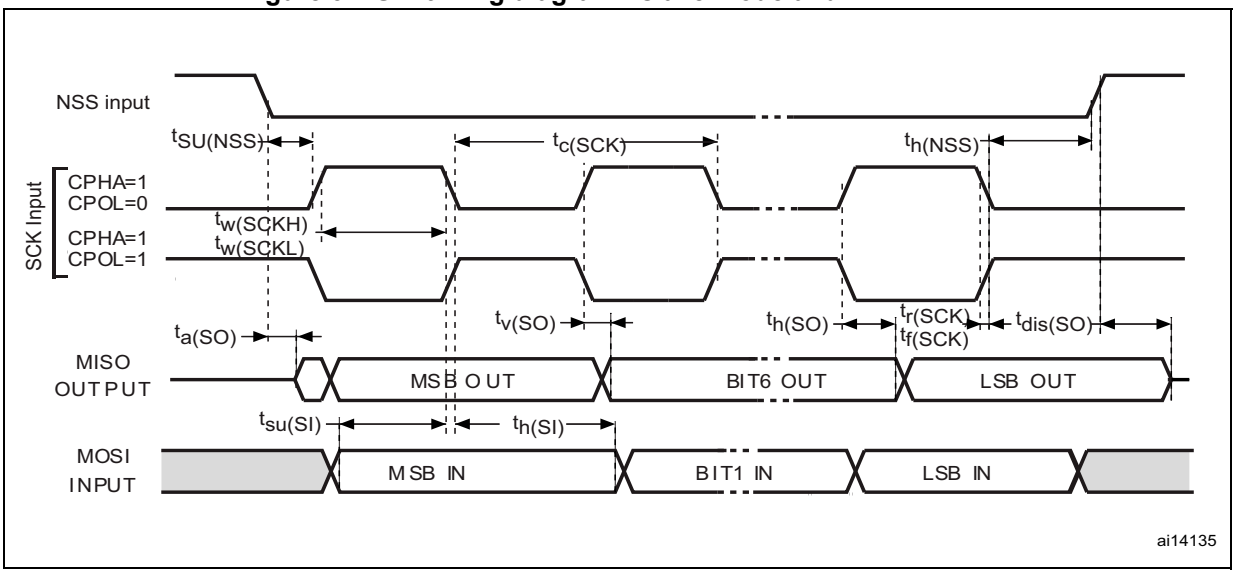
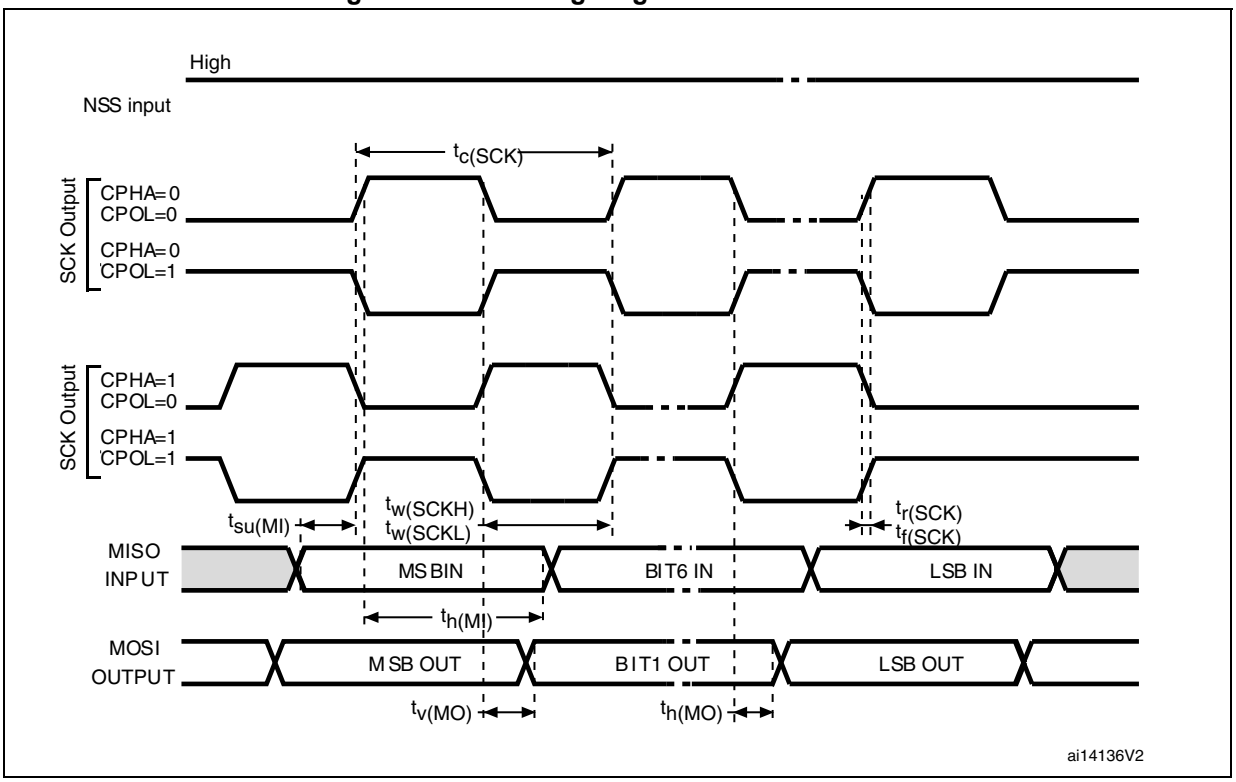


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. LQFP32- 32-pin low profile quad flat package (7x7), package mechanical data

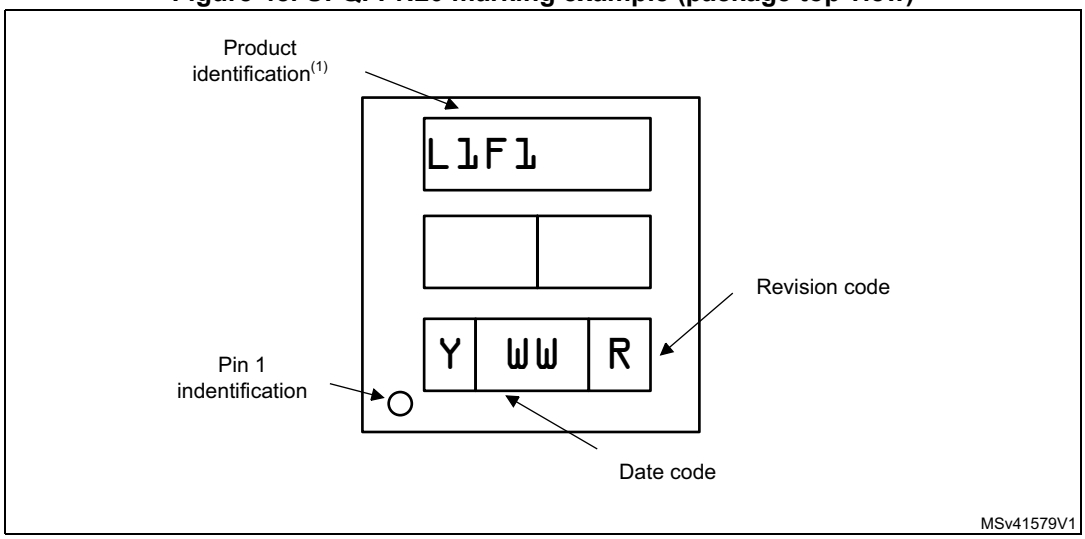
Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	0.100	-	-	0.0039	-
-	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

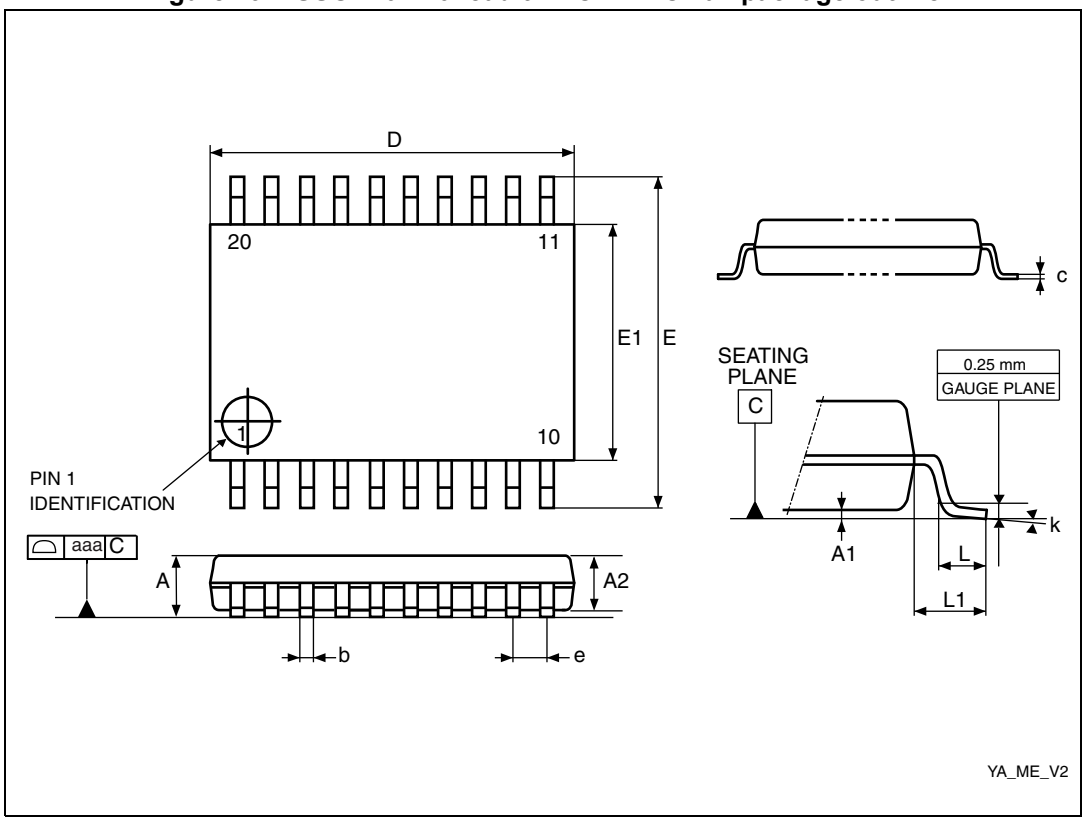
Figure 48. UFQFPN20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.5 TSSOP20 package information

Figure 49. TSSOP20 - 20-lead thin shrink small package outline



1. Drawing is not to scale.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data

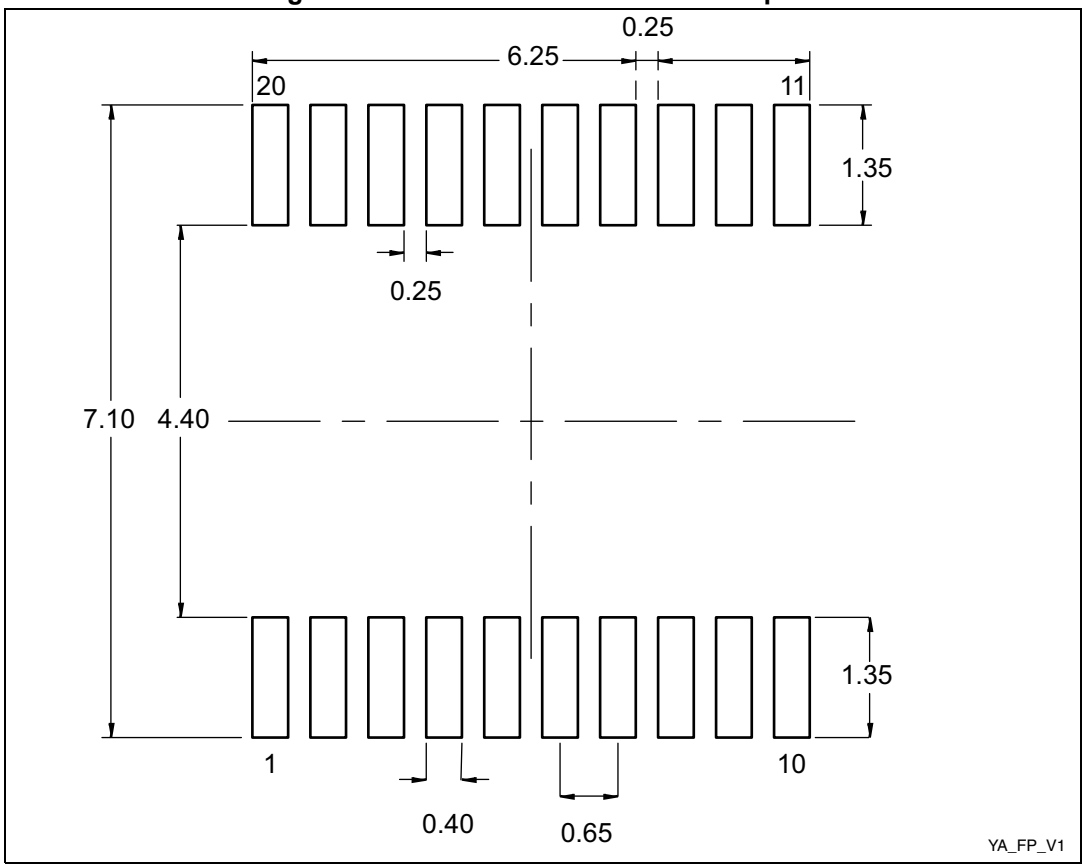
Dim.	mm				inches(1)	
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
CP	-	-	0.100	-	-	0.0039
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	0.1693	0.0256	-
L	0.450	0.600	0.750	0.1693	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data (continued)

Dim.	mm				inches[1]	
	Min	Typ	Max	Min	Typ	Max
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039
Number of pins	20					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

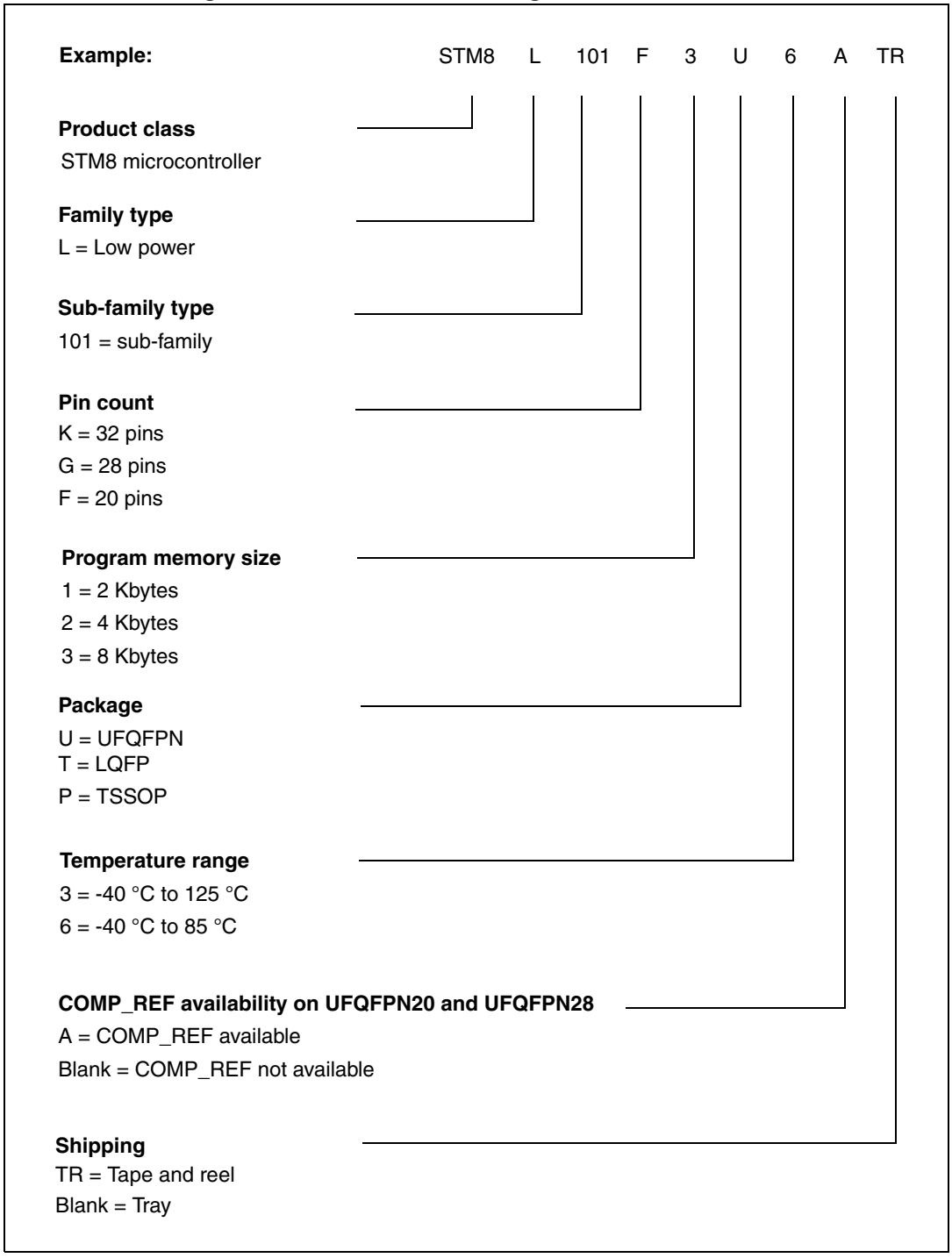
Figure 50. TSSOP20 recommended footprint



1. Dimensions are in millimeters.

11 Device ordering information

Figure 52. STM8L101xx ordering information scheme



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows the users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows the users to specify the components that they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

Table 44. Document revision history (continued)

Date	Revision	Changes
07-Sep-2009	7	Added STM8L101F2U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers Modified *Section 2: Description on page 9*. Modified *Table 2: STM8L101xx device feature summary on page 9* (Flash) Modified *Figure 1: STM8L101xx device block diagram on page 10* Modified *Section 3.5: Memory on page 12* Added note below *Figure 2: Standard 20-pin UFQFPN package pinout on page 15* and *Figure 5: Standard 28-pin UFQFPN package pinout on page 17* Added *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers on page 18* Modified reset values for Px_IDR registers in *Table 6: I/O Port hardware register map on page 24* Added *Section 6: Interrupt vector mapping on page 32* Modified OPT numbers in *Section 7: Option bytes* Modified OPT2 in *Table 10: Option bytes* Added *Section 8: Unique ID on page 36* TIM_IR pin replaced with IR_TIM pin Modified *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44* Modified *Figure 15: Typ. IDD(Halt) vs. VDD, fCPU = 2 MHz and 16 MHz on page 44* and *Figure 19: Typical LSI RC frequency vs. VDD on page 47* Modified *Table 27: Output driving current (High sink ports) on page 51* Updated *Table 29: Output driving current (PA0 with high sink LED driver capability) on page 51* Modified *: Functional EMS (electromagnetic susceptibility) on page 60* Modified conditions in *Table 35: EMI data on page 61* Added note to *Figure 37: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5) on page 67* Modified *Figure 41: UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4)(1) on page 70* Added *Figure 44: UFQFPN20 recommended footprint (1) on page 71* Added *Figure 46: TSSOP20 recommended footprint (1) on page 72* CMP replaced with COMP

Table 44. Document revision history (continued)

Date	Revision	Changes
29-Nov-2009	8	Modified status of the document (datasheet instead of preliminary data) Replaced WFQFPN32 with UFQFPN32 and WFQFPN28 with UFQFPN28. Modified title of the reference manual mentioned in *Section 2: Description on page 9* Added references to “low-density” in *Section 2: Description on page 9*, *Section 3.5: Memory on page 12* and in *Figure 8: Memory map on page 23* Modified *Figure 8: Memory map on page 23* (unique ID are added) *Table 7: General hardware register map on page 25*: Modified reserved areas and IR block replaced with IRTIM block Modified t_{TEMP} in *Table 17: Operating conditions at power-up / power-down on page 41* Modified *Table 23: LSI oscillator characteristics on page 47* Modified *Table 25: Flash program memory on page 47* (t_{PROG}) Modified *Table 16: General operating conditions on page 40* and *Table 38: Thermal characteristics on page 63* Modified *Section 13: Revision history on page 82*
18-Jun-2010	9	Modified *Introduction* and *Description* Modified one reserved area (0x00 5055 to 0x00 509F) in *Table 7: General hardware register map* Modified*Table 4: STM8L101xx pin description*: modified note 2 and removed “wpu” for PC0 and PC1 Removed one note to *Table 22: HSI oscillator characteristics on page 45* Modified first paragraph in *Section : NRST pin* Modified OPT3 description in *Table 11: Option byte description* Added note 5 to *Table 18: Total current consumption in Run mode* Modified $V_{ESD(CDM)}$ in *Table 36: ESD absolute maximum ratings on page 61* Modified *Figure 36: Typical application with I2C bus and timing diagram 1) on page 59* Modified COMP_REF availability information in *Figure 52: STM8L101xx ordering information scheme on page 79* Modified *Section 12.2: Software tools on page 78*
21-Jul-2010	10	Modified *Table 3: Legend/abbreviation for table 4 on page 20* and *Table 4: STM8L101xx pin description on page 20* (for PA0, PA1, PB0 and PB4) Modified *Table 13: Voltage characteristics on page 38* and *Table 14: Current characteristics on page 39* Modified V_{IH} in *Table 26: I/O static characteristics on page 48* Added notes below UFQFPN32 package