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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f2p6tr

3.5 Memory

The STM8L101xx devices have the following main features:

- 1.5 Kbytes of RAM
- The EEPROM is divided into two memory arrays (see the STM8L reference manual for details on the memory mapping):
  - Up to 8 Kbytes of low-density embedded Flash program including up to 2 Kbytes of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.

Error correction code is implemented on the EEPROM.

3.6 Low power modes

To minimize power consumption, the product features three low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode: CPU and peripheral clocks are stopped. The programmable wakeup time is controlled by the AWU unit.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. Wakeup is triggered by an external interrupt.

3.7 Voltage regulators

The STM8L101xx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

3.8 Clock control

The STM8L101xx embeds a robust clock controller. It is used to distribute the system clock to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

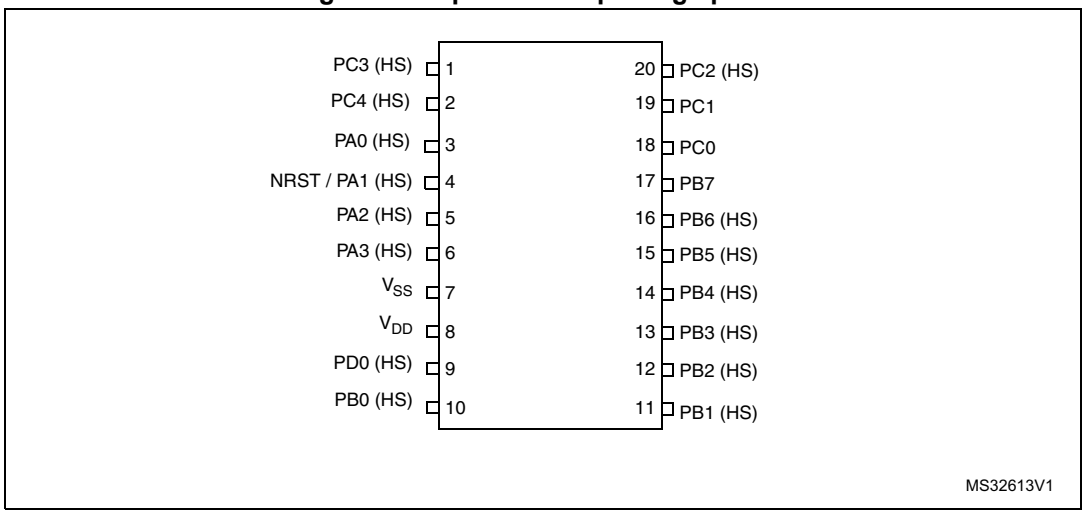
In addition, a 38 kHz low speed internal RC oscillator is used by the independent watchdog (IWDG) and Auto-wakeup unit (AWU).

3.9 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

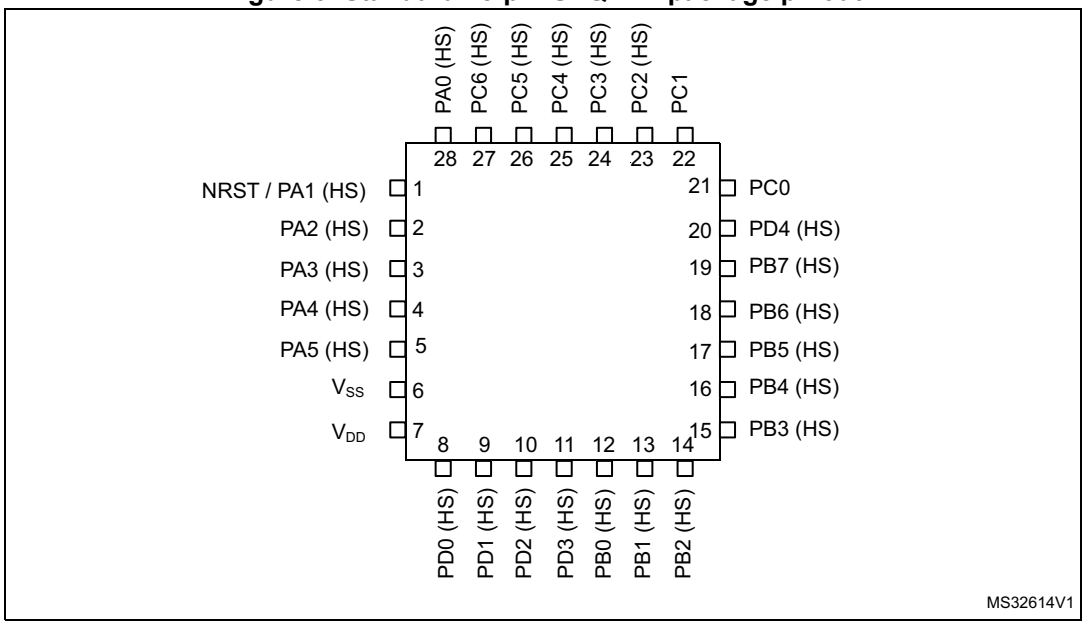
It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

Figure 4. 20-pin TSSOP package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

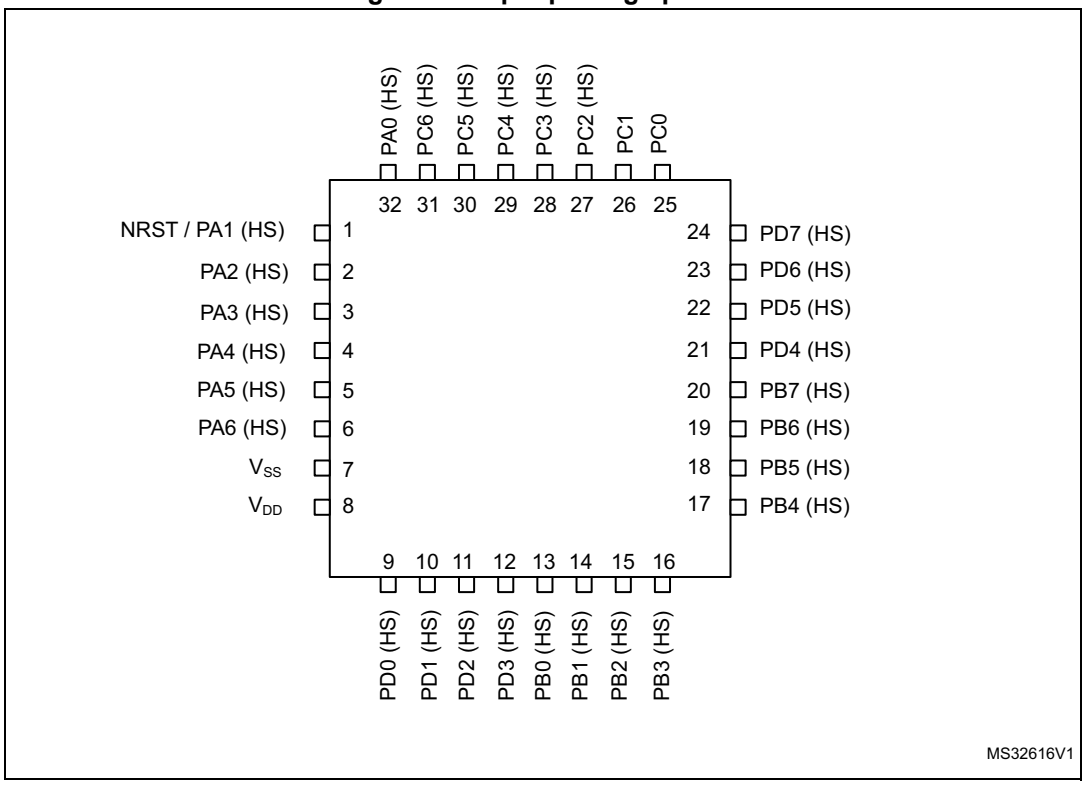
Figure 5. Standard 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 28-pin UFQFPN package. It is available on Port A6 in the Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers.

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	-	Reserved	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(1)	0x00 800C
2-3	-	Reserved	-	-	-	-	0x00 8010 -0x00 8017
4	AWU	Auto wakeup from Halt	-	Yes	Yes	Yes(1)	0x00 8018
5	-	Reserved	-	-	-	-	0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	-	Reserved	-	-	-	-	0x00 8048
17	-	Reserved	-	-	-	-	0x00 804C -0x00 804F
18	COMP	Comparators	-	-	Yes	Yes(1)	0x00 8050
19	TIM2	Update /Overflow/Trigger/Break	-	-	Yes	Yes	0x00 8054
20	TIM2	Capture/Compare	-	-	Yes	Yes	0x00 8058
21	TIM3	Update /Overflow/Break	-	-	Yes	Yes(1)	0x00 805C
22	TIM3	Capture/Compare	-	-	Yes	Yes(1)	0x00 8060
23-24	-	Reserved	-	-	-	-	0x00 8064-0x00 806B
25	TIM4	Update /Trigger	-	-	Yes	Yes(1)	0x00 806C
26	SPI	End of Transfer	Yes	Yes	Yes	Yes(1)	0x00 8070

Table 11. Option byte description (continued)

OPT3	**DATASIZE[7:0]** Size of the data EEPROM area 0x00: no data EEPROM area (1) 0x01: 1 page reserved for data storage from 0x9FC0 to 0x9FFF(1) 0x02: 2 pages reserved for data storage from 0x9F80 to 0x9FFF(1) ... (1) 0x20: 32 pages reserved for data storage from 0x9800 to 0x9FFF(1) Refer to *Data EEPROM (DATA)* section in the STM8L reference manual (RM0013) for more details. DATASIZE[7:6] are forced to 0 internal by HW.
OPT4	**IWDG_HW:** *Independent watchdog* 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: *Independent window watchdog reset on Halt/Active-halt* 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode

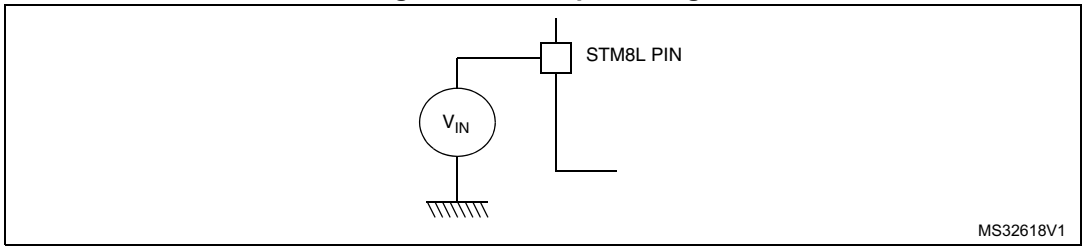
1. 0x00 is the only allowed value for 4 Kbyte STM8L101xx devices.

Caution: After a device reset, read access to the program memory is not guaranteed if address 0x4807 is not programmed to 0x00.

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on true open drain pins (PC0 and PC1)(1)	V_{SS}-0.3	V_{DD} + 4.0	
	Input voltage on any other pin (2)	V_{SS}-0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		-

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER} (1)	Master clock frequency	1.65 V ≤V_{DD} < 3.6 V	2	16	MHz
V_{DD}	Standard operating voltage	-	1.65	3.6	V
P_D (2)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP32	-	288	mW
		UFQFPN32	-	288	
		UFQFPN28	-	250	
		TSSOP20	-	181	
		UFQFPN20	-	196	
	Power dissipation at T_A= 125 °C for suffix 3 devices	LQFP32	-	83	
		UFQFPN32	-	185	
		UFQFPN28	-	62	
		TSSOP20	-	45	
		UFQFPN20	-	49	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)	–40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)	–40	125	
T_J	Junction temperature range	-40 °C ≤T_A ≤85 °C (6 suffix version)	- 40	105	°C
		-40 °C ≤T_A ≤125 °C (3 suffix version)	–40	130	°C

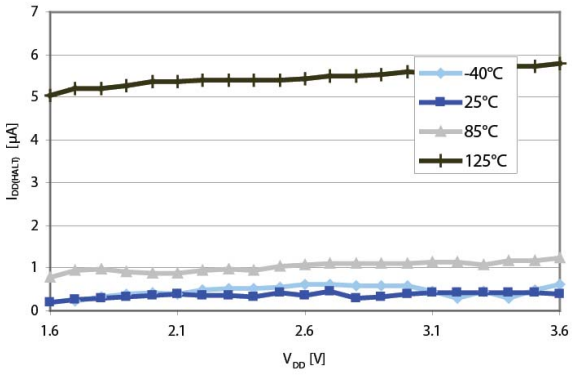
1. f_{MASTER} = f_{CPU}
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”

Table 20. Total current consumption and timing in Halt and Active-halt mode at V_{DD} = 1.65 V to 3.6 V (1)(2)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC osc. (at 37 kHz)	T_A = -40 °C to 25 °C	0.8	2	µA
			T_A = 55 °C	1	2.5	µA
			T_A = 85 °C	1.4	3.2	µA
			T_A = 105 °C	2.9	7.5	µA
			T_A = 125 °C	5.8	13	µA
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode	-	-	2	-	mA
$t_{WU(AH)}$(3)	Wakeup time from Active-halt mode to Run mode	f_{CPU}= 16 MHz		4	6.5	µs
$I_{DD(Halt)}$	Supply current in Halt mode	T_A = -40 °C to 25 °C		0.35	1.2(4)	µA
		T_A = 55 °C		0.6	1.8	µA
		T_A = 85 °C		1	2.5(4)	µA
		T_A = 105 °C		2.5	6.5	µA
		T_A = 125 °C		5.4	12(4)	µA
$I_{DD(WUFH)}$	Supply current during wakeup time from Halt mode			2	-	mA
$t_{WU(Halt)}$(3)	Wakeup time from Halt mode to Run mode	f_{CPU} = 16 MHz		4	6.5	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Measured from interrupt event to interrupt vector fetch.
   To get t_{WU} for another CPU frequency use t_{WU}(FREQ) = t_{WU}(16 MHz) + 1.5 (T_{FREQ}-$T_{16\ MHz}$).
   The first word of interrupt routine is fetched 5 CPU cycles after t_{WU}.
4. Tested in production.

Figure 15. Typ. $I_{DD(Halt)}$ vs. V_{DD}, f_{CPU} = 2 MHz and 16 MHz



1. Typical current consumption measured with code executed from Flash.

Table 26. I/O static characteristics (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(6)	$V_{IN} = V_{SS}$	30	45	60	kΩ
C_{IO}(7)	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 22*).
7. Data guaranteed by Design, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs. V_{DD} (High sink I/Os)

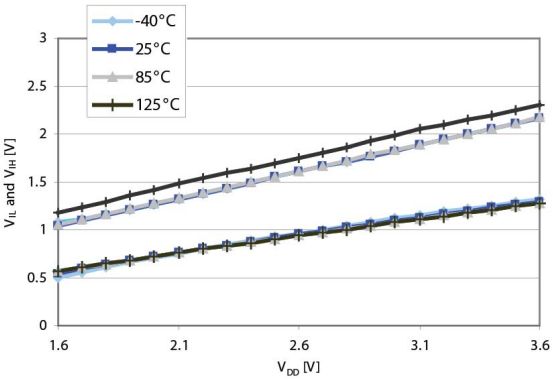
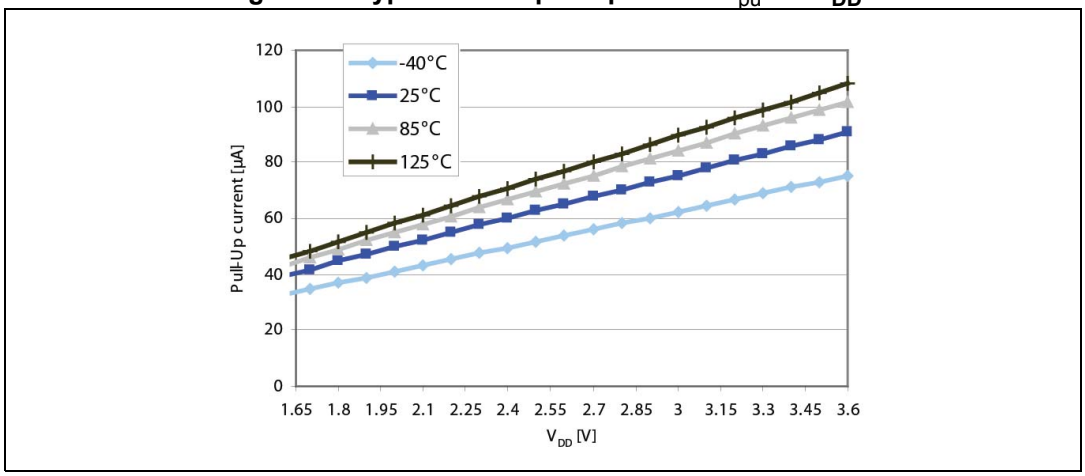
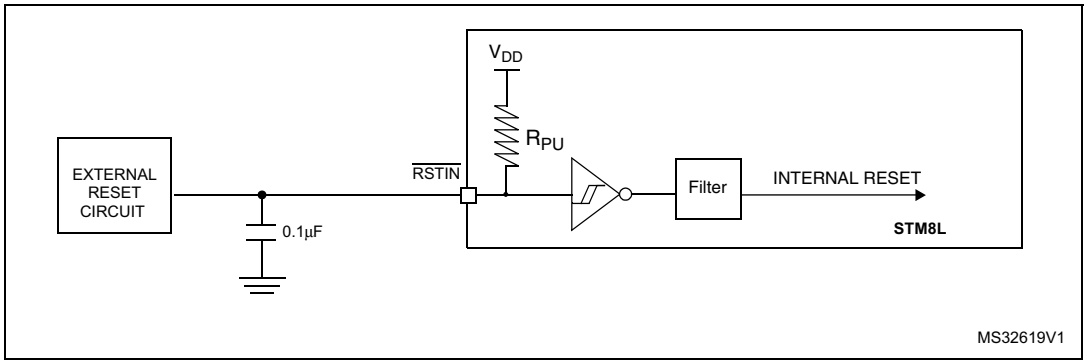


Figure 31. Typical NRST pull-up current I_{pu} vs. V_{DD}



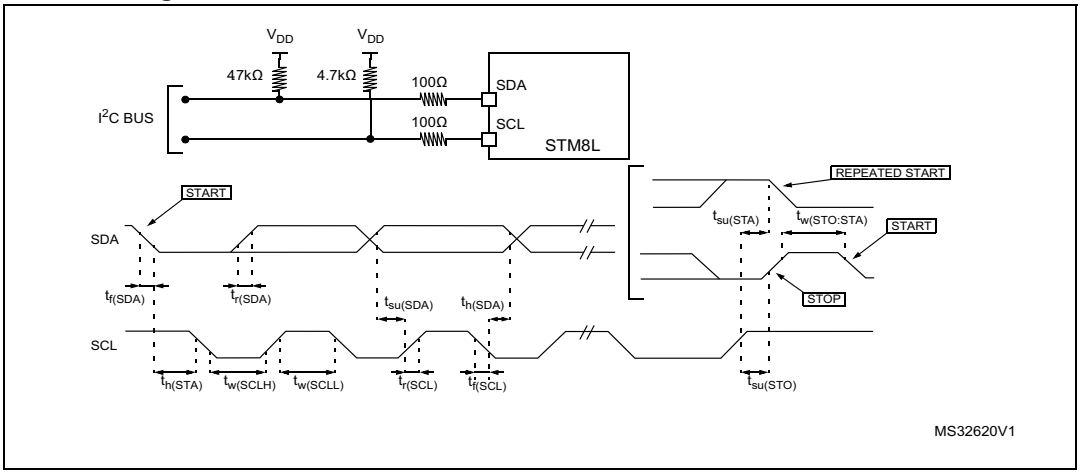
The reset network shown in *Figure 32* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 30*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 32. Recommended NRST pin configuration



1. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected.
2. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.

Figure 36. Typical application with I2C bus and timing diagram 1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

9.3.8 Comparator characteristics

Table 33. Comparator characteristics

Symbol	Parameter	Conditions	Min (1)	Typ	Max(1)	Unit
$V_{IN(COMP\_REF)}$	Comparator external reference	-	-0.1	-	V_{DD}-1.25	V
V_{IN}	Comparator input voltage range	-	-0.25	-	V_{DD}+0.25	V
V_{offset}(2)	Comparator offset error	-	-	-	±20	mV
t_{START}	Startup time (after BIAS_EN)	-	-	-	3(1)	µs
$I_{DD(COMP)}$	Analog comparator consumption	-	-	-	25(1)	µA
	Analog comparator consumption during power-down	-	-	-	60(1)	nA
t_{propag}(2)	Comparator propagation delay	100-mV input step with 5-mV overdrive, input rise time = 1 ns	-	-	2(1)	µs

1. Data guaranteed by design, not tested in production.
2. The comparator accuracy depends on the environment. In particular, the following cases may reduce the accuracy of the comparator and must be avoided:
   - Negative injection current on the I/Os close to the comparator inputs
   - Switching on I/Os close to the comparator inputs
   - Negative injection current on not used comparator input.
   - Switching with a high dV/dt on not used comparator input.

   These phenomena are even more critical when a big external serial resistor is added on the inputs.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 35. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP32 conforming to IEC61967-2	0.1 MHz to 30 MHz	-3	dBµV
			30 MHz to 130 MHz	-6	
			130 MHz to 1 GHz	-5	
			SAE EMI Level	1	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin).

This test conforms to the JESD22-A114A/A115A standard.

Table 36. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results, not tested in production.

Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 37. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 40*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

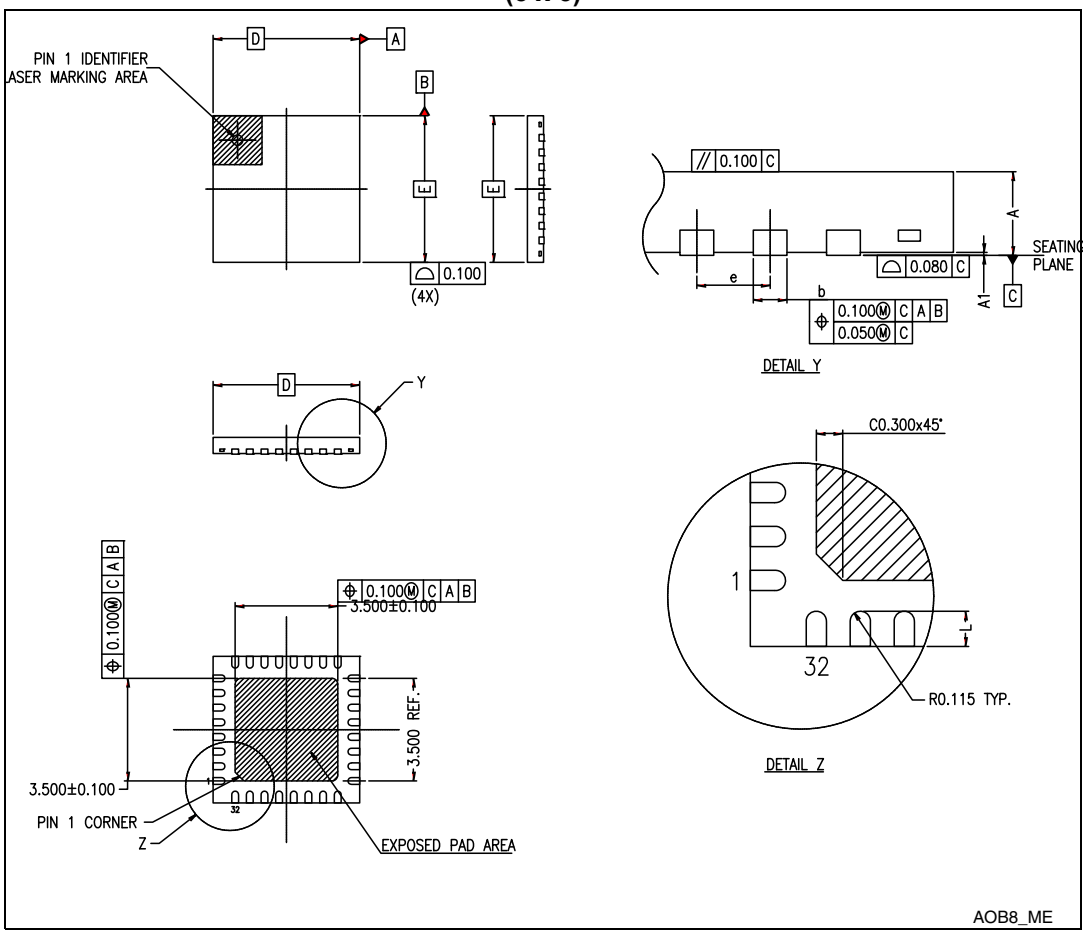
- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 UFQFPN32 package information

Figure 37. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)



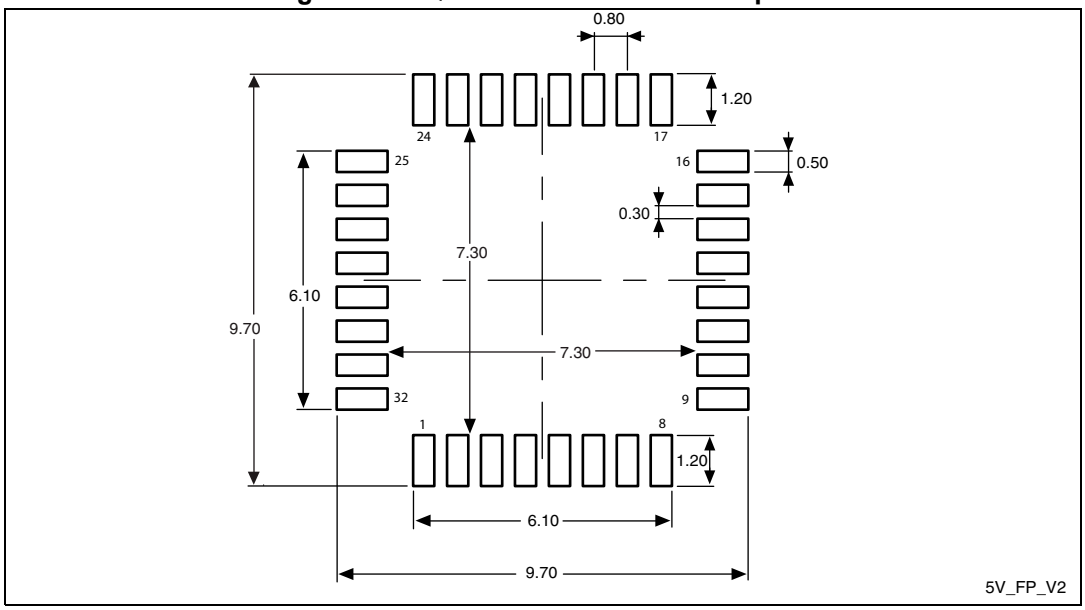
1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 40. LQFP32- 32-pin low profile quad flat package (7x7), package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.600	-	-	0.2205	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.600	-	-	0.2205	-
e	-	0.800	-	-	0.0315	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	0.100	-	-	0.0039	-
-	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. LQFP32 recommended footprint

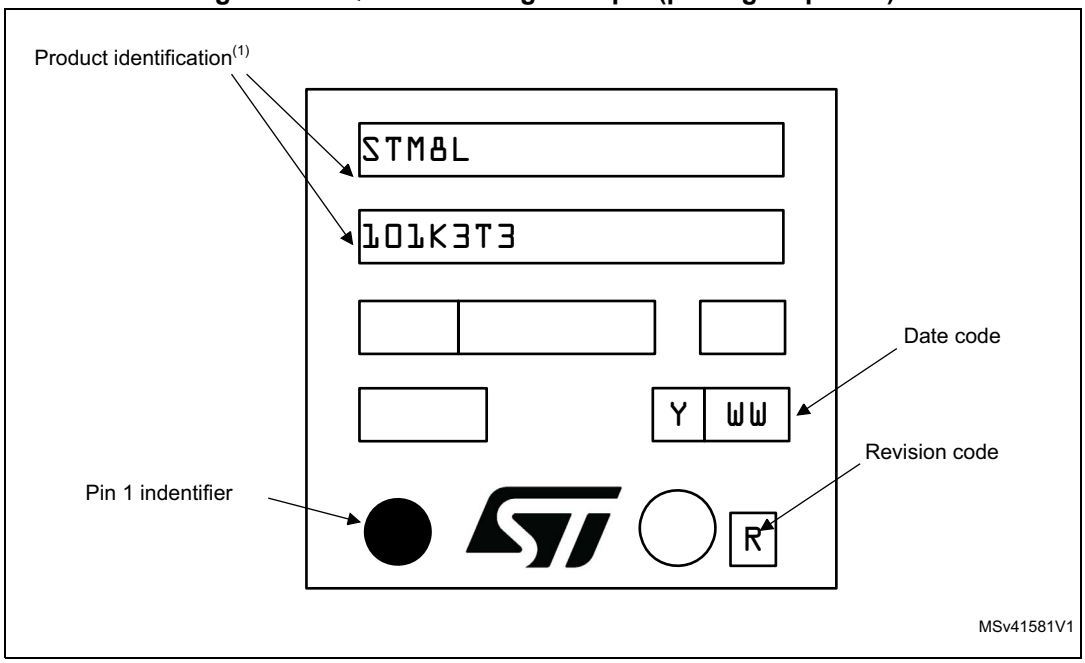


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. LQFP32 marking example (package top view)



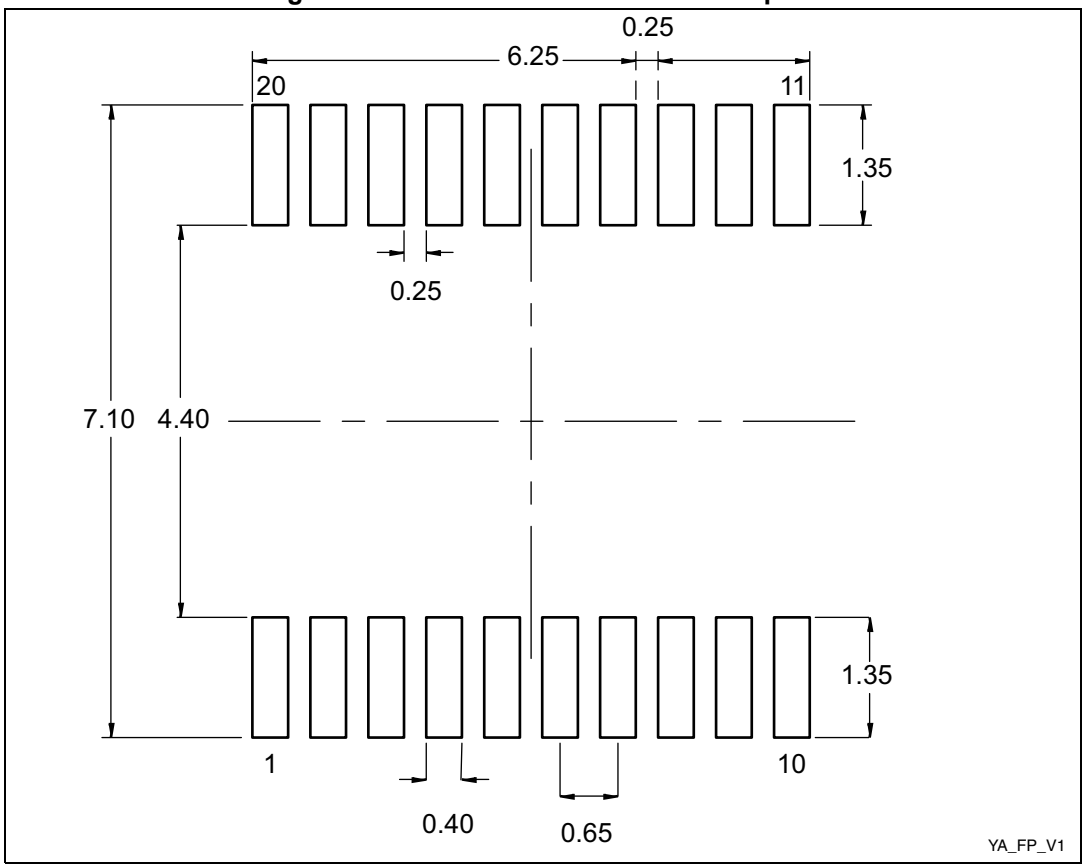
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data (continued)

Dim.	mm				inches[1]	
	Min	Typ	Max	Min	Typ	Max
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039
Number of pins	20					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

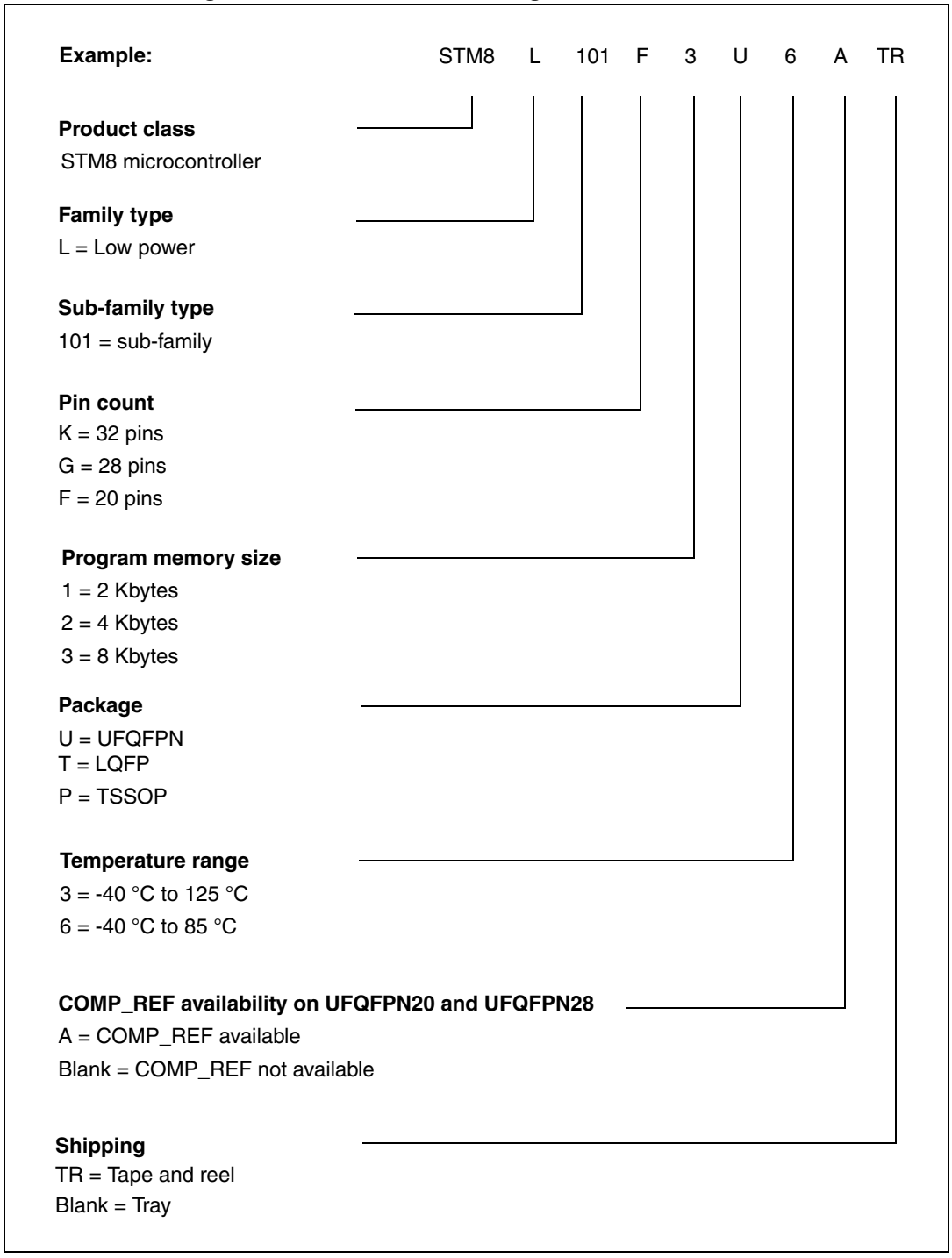
Figure 50. TSSOP20 recommended footprint



1. Dimensions are in millimeters.

11 Device ordering information

Figure 52. STM8L101xx ordering information scheme



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

Table 44. Document revision history (continued)

Date	Revision	Changes
18-Dec-2014	14	Updated: – *Figure 46: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3 mm)*, – *Table 42: UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data*.
02-Aug-2016	15	Added: – *Figure 39: UFQFPN32 marking example (package top view)* – *Figure 42: LQFP32 marking example (package top view)* – *Figure 45: UFQFPN28 marking example (package top view)* – *Figure 48: UFQFPN20 marking example (package top view)* – *Figure 51: TSSOP20 marking example (package top view)* Updated: – *Section 9.2: Absolute maximum ratings*.