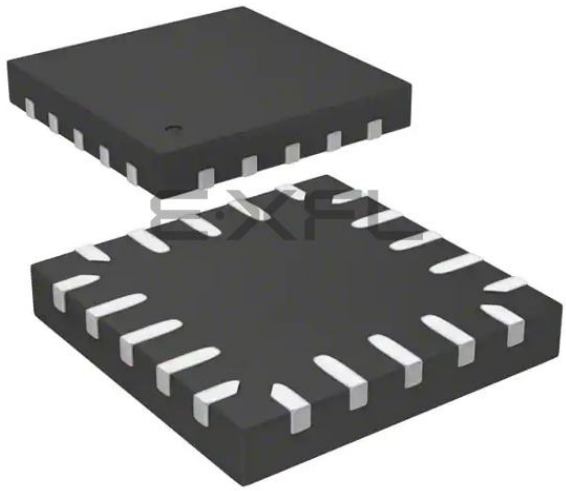

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f2u6atr

1 Introduction

This datasheet provides the STM8L101x1 STM8L101x2 STM8L101x3 pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller memory, registers and peripherals, please refer to the STM8L reference manual.

The STM8L101x1 STM8L101x2 STM8L101x3devices are members of the STM8L low-power 8-bit family. They are
referred to as low-density devices in the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller family reference manual (RM0013) and in the STM8L Flash programming manual (PM0054).

All devices of the SM8L product line provide the following benefits:

- Reduced system cost
  - Up to 8 Kbytes of low-density embedded Flash program memory including up to 2 Kbytes of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs.
  - Smaller battery and cheaper power supplies.
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MH, 0.8 µA in Active-halt mode, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Product family operating from 1.65 V to 3.6 V supply.

2 Description

The STM8L101x1 STM8L101x2 STM8L101x3 low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All STM8L101xx microcontrollers feature low power low-voltage single-supply program Flash memory. The 8-Kbyte devices embed data EEPROM.

The STM8L101xx low power family is based on a generic set of state-of-the-art peripherals. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

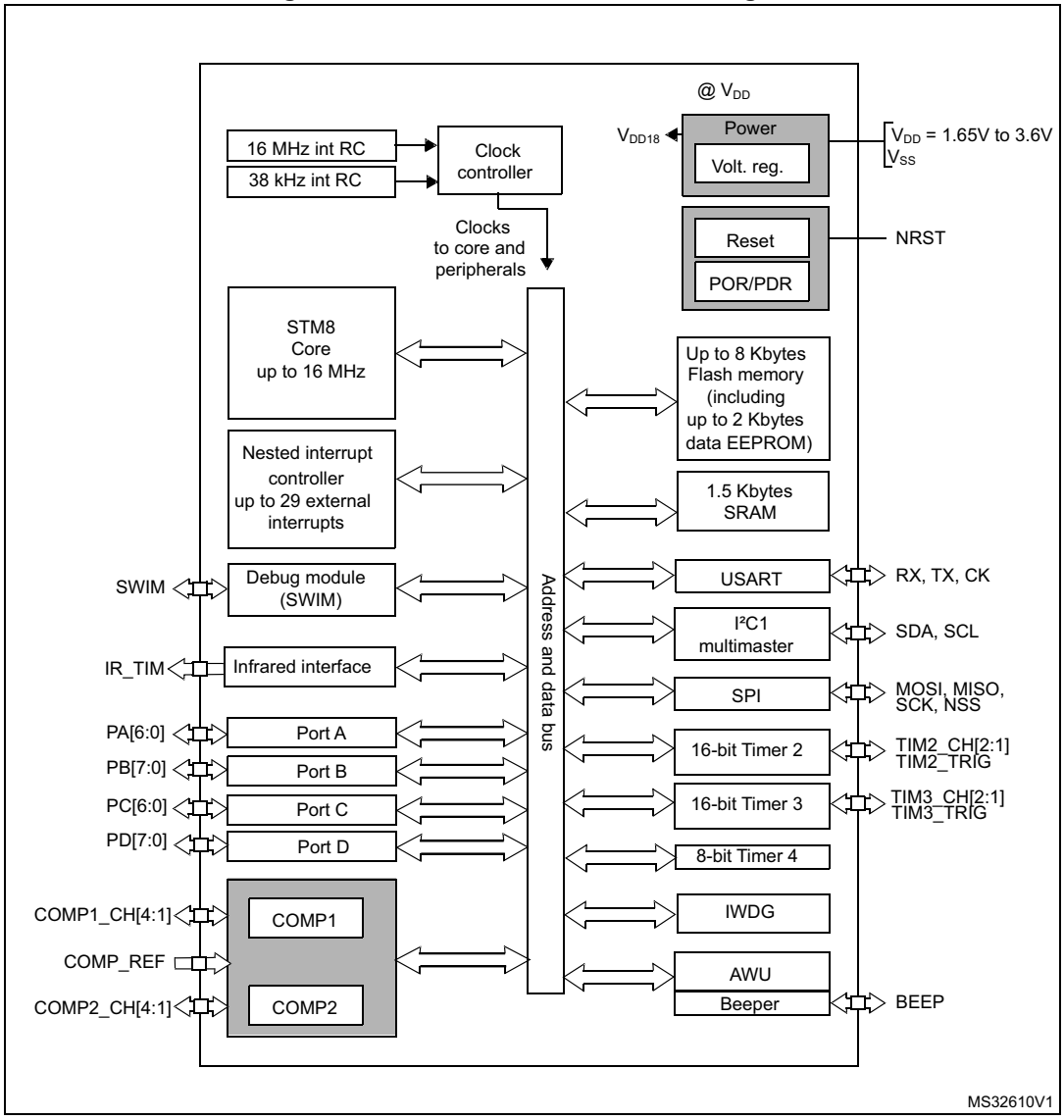
All STM8L low power products are based on the same architecture with the same memory mapping and a coherent pinout.

Table 2. STM8L101xx device feature summary

Features	STM8L101xx		
Flash	2 Kbytes of Flash program memory	4 Kbytes of Flash program memory	8 Kbytes of Flash program memory including up to 2 Kbytes of Data EEPROM
RAM	1.5 Kbytes		
Peripheral functions	Independent watchdog (IWDG), Auto-wakeup unit (AWU), Beep, Serial peripheral interface (SPI), Inter-integrated circuit (I²C), Universal synchronous / asynchronous receiver / transmitter (USART), 2 comparators, Infrared (IR) interface		
Timers	Two 16-bit timers, one 8-bit timer		
Operating voltage	1.65 to 3.6 V		
Operating temperature	-40 to +85 °C		-40 to +85 °C or -40 to +125 °C
Packages	UFQFPN20 3x3	UFQFPN28 4x 4 UFQFPN20 3x3 TSSOP20 4.4 x 6.4	UFQFPN28 4x4 UFQFPN20 3x3 UFQFPN32 LQFP32

3 Product overview

Figure 1. STM8L101xx device block diagram



Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog

3.10 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

3.11 General purpose and basic timers

STM8L101xx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Time base generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.12 Beeper

The STM8L101xx devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.13 Infrared (IR) interface

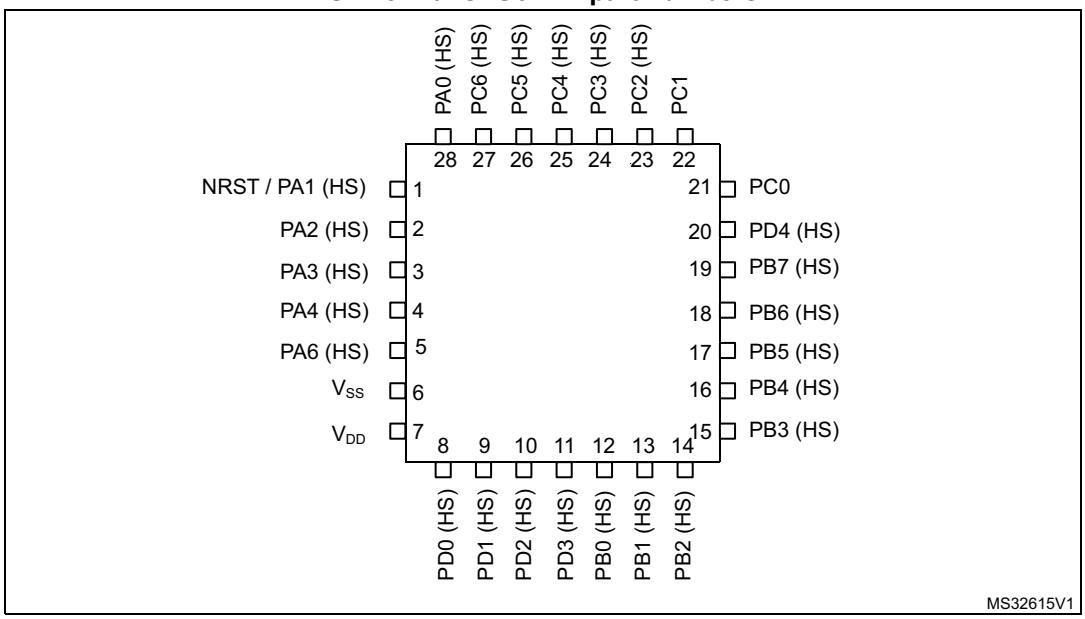
The STM8L101xx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

3.14 Comparators

The STM8L101xx features two zero-crossing comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal (comparison with ground) or external (comparison to a reference pin voltage).

Each comparator is connected to 4 channels, which can be used to generate interrupt, timer input capture or timer break. Their polarity can be inverted.

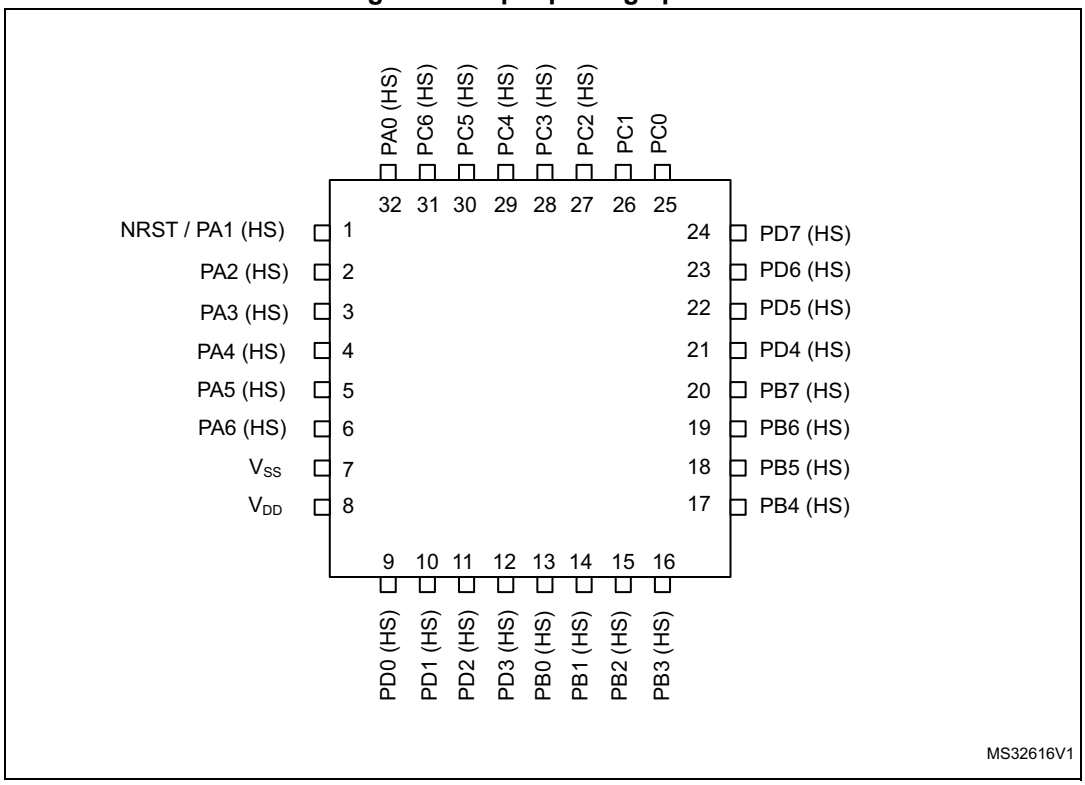
Figure 6. 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Warning: For the STM8L101G3U6ATR and STM8L101G2U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	26	26	30	PC5	I/O	**X**	X	X	HS	X	X	**Port C5**	-
-	-	-	27	27	31	PC6	I/O	**X**	X	X	HS	X	X	**Port C6**	-
20	20	3	28	28	32	PA0(5)/SWIM/ BEEP/IR_TIM (6)	I/O	X	**X**(5)	X	HS(6)	X	X	**Port A0**	SWIM input and output /Beep output/Timer Infrared output

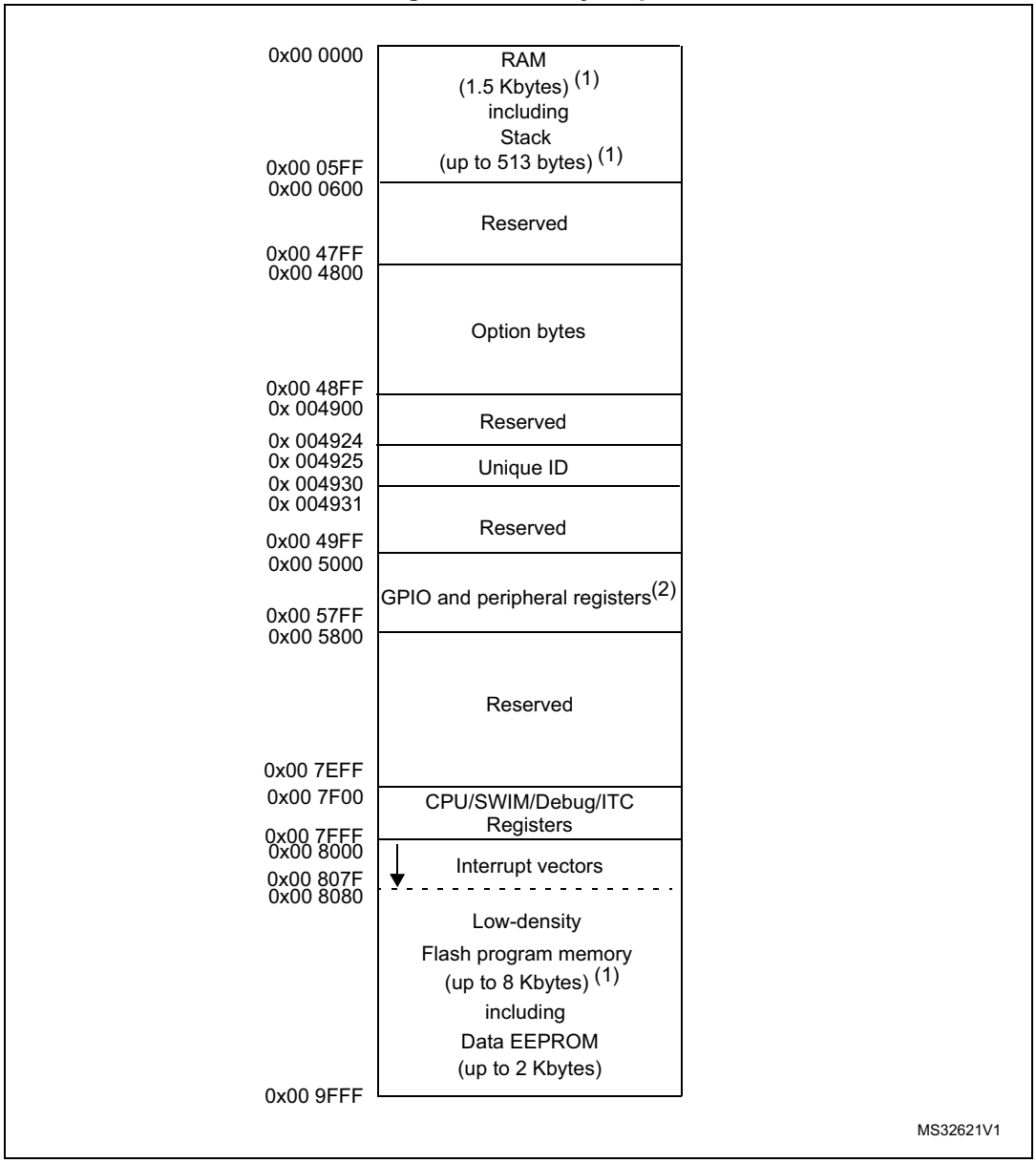
1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

5 Memory and register map

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER} (1)	Master clock frequency	1.65 V ≤V_{DD} < 3.6 V	2	16	MHz
V_{DD}	Standard operating voltage	-	1.65	3.6	V
P_D (2)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP32	-	288	mW
		UFQFPN32	-	288	
		UFQFPN28	-	250	
		TSSOP20	-	181	
		UFQFPN20	-	196	
	Power dissipation at T_A= 125 °C for suffix 3 devices	LQFP32	-	83	
		UFQFPN32	-	185	
		UFQFPN28	-	62	
		TSSOP20	-	45	
		UFQFPN20	-	49	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)	–40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)	–40	125	
T_J	Junction temperature range	-40 °C ≤T_A ≤85 °C (6 suffix version)	- 40	105	°C
		-40 °C ≤T_A ≤125 °C (3 suffix version)	–40	130	°C

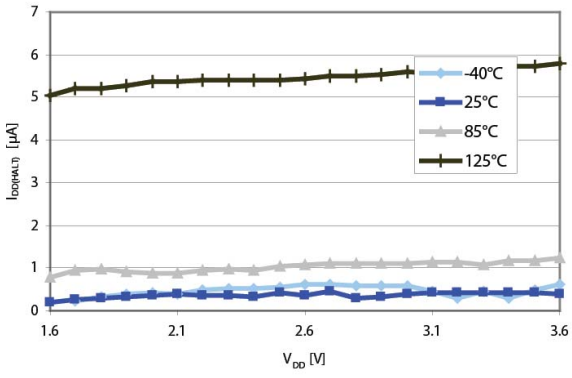
1. f_{MASTER} = f_{CPU}
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”

Table 20. Total current consumption and timing in Halt and Active-halt mode at V_{DD} = 1.65 V to 3.6 V (1)(2)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC osc. (at 37 kHz)	T_A = -40 °C to 25 °C	0.8	2	µA
			T_A = 55 °C	1	2.5	µA
			T_A = 85 °C	1.4	3.2	µA
			T_A = 105 °C	2.9	7.5	µA
			T_A = 125 °C	5.8	13	µA
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode	-	-	2	-	mA
$t_{WU(AH)}$(3)	Wakeup time from Active-halt mode to Run mode	f_{CPU}= 16 MHz		4	6.5	µs
$I_{DD(Halt)}$	Supply current in Halt mode	T_A = -40 °C to 25 °C		0.35	1.2(4)	µA
		T_A = 55 °C		0.6	1.8	µA
		T_A = 85 °C		1	2.5(4)	µA
		T_A = 105 °C		2.5	6.5	µA
		T_A = 125 °C		5.4	12(4)	µA
$I_{DD(WUFH)}$	Supply current during wakeup time from Halt mode			2	-	mA
$t_{WU(Halt)}$(3)	Wakeup time from Halt mode to Run mode	f_{CPU} = 16 MHz		4	6.5	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Measured from interrupt event to interrupt vector fetch.
   To get t_{WU} for another CPU frequency use t_{WU}(FREQ) = t_{WU}(16 MHz) + 1.5 (T_{FREQ}-$T_{16\ MHz}$).
   The first word of interrupt routine is fetched 5 CPU cycles after t_{WU}.
4. Tested in production.

Figure 15. Typ. $I_{DD(Halt)}$ vs. V_{DD}, f_{CPU} = 2 MHz and 16 MHz



1. Typical current consumption measured with code executed from Flash.

Inter IC control interface (I2C)

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

The STM8L I^2C interface meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 32. I2C characteristics

Symbol	Parameter	Standard mode I2C		Fast mode I2C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0 (3)	-	0 (4)	900 (3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SCK} must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

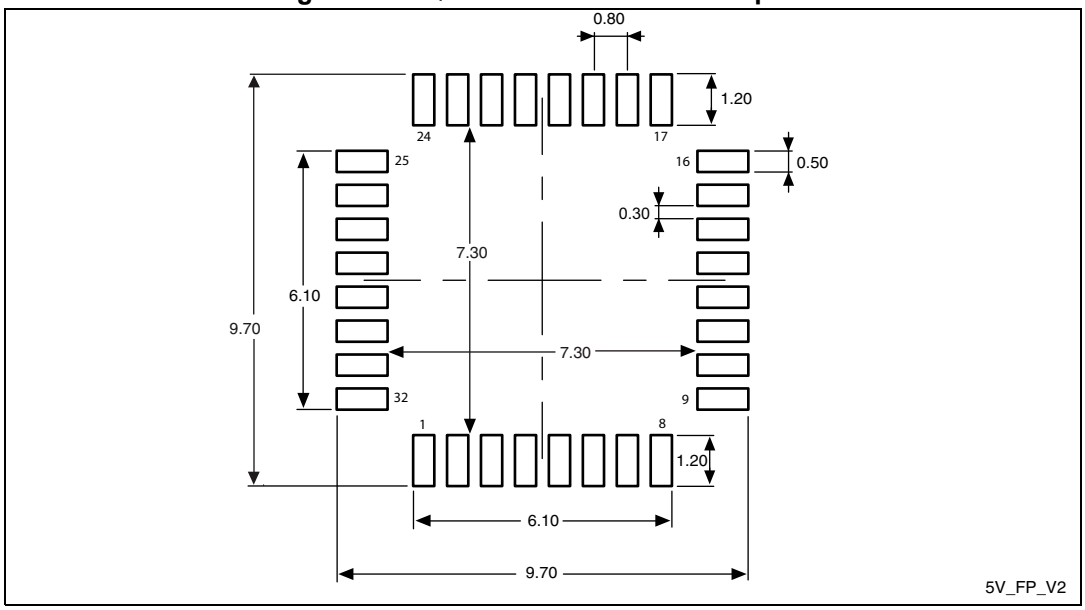
Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance
For other speed ranges, achieved speed can have ±2% tolerance
The above variations depend on the accuracy of the external components used.

Table 38. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W
	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	25	°C/W
	Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm	80	°C/W
	Thermal resistance junction-ambient UFQFPN 20 - 3 x 3 mm - 0.6 mm	102	°C/W
	Thermal resistance junction-ambient TSSOP 20	110	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

Figure 41. LQFP32 recommended footprint

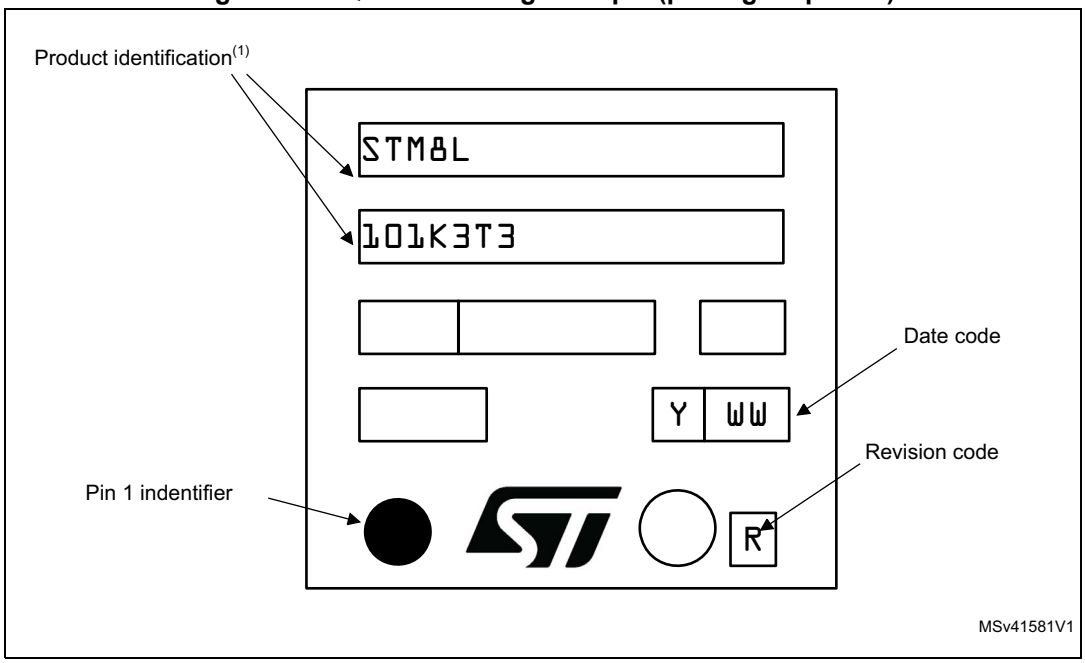


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 42. LQFP32 marking example (package top view)



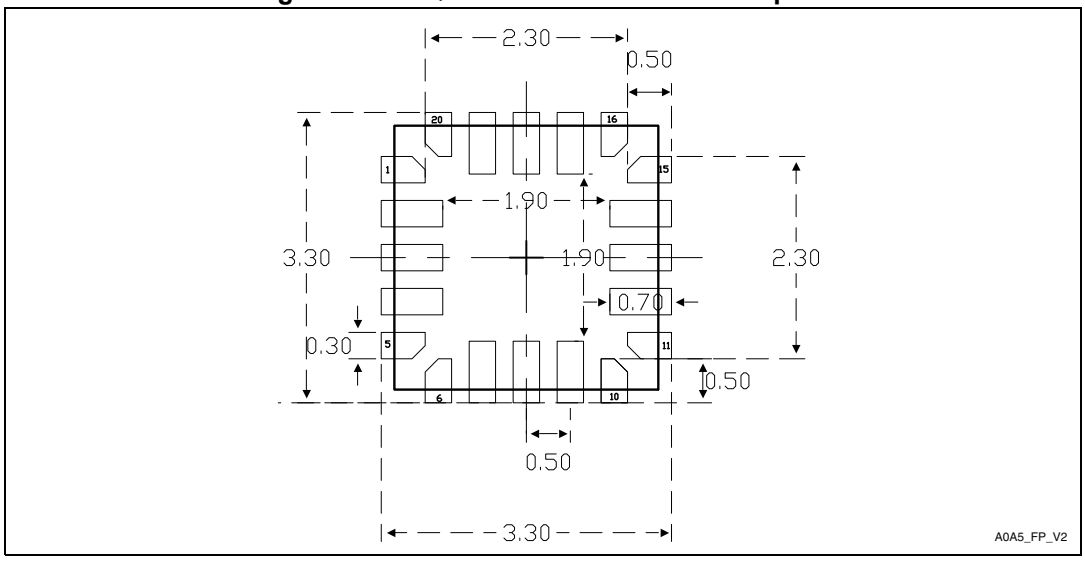
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 42. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd	-	0.050	-	-	0.0020	-

1. Values in inches are rounded to 4 decimal digits

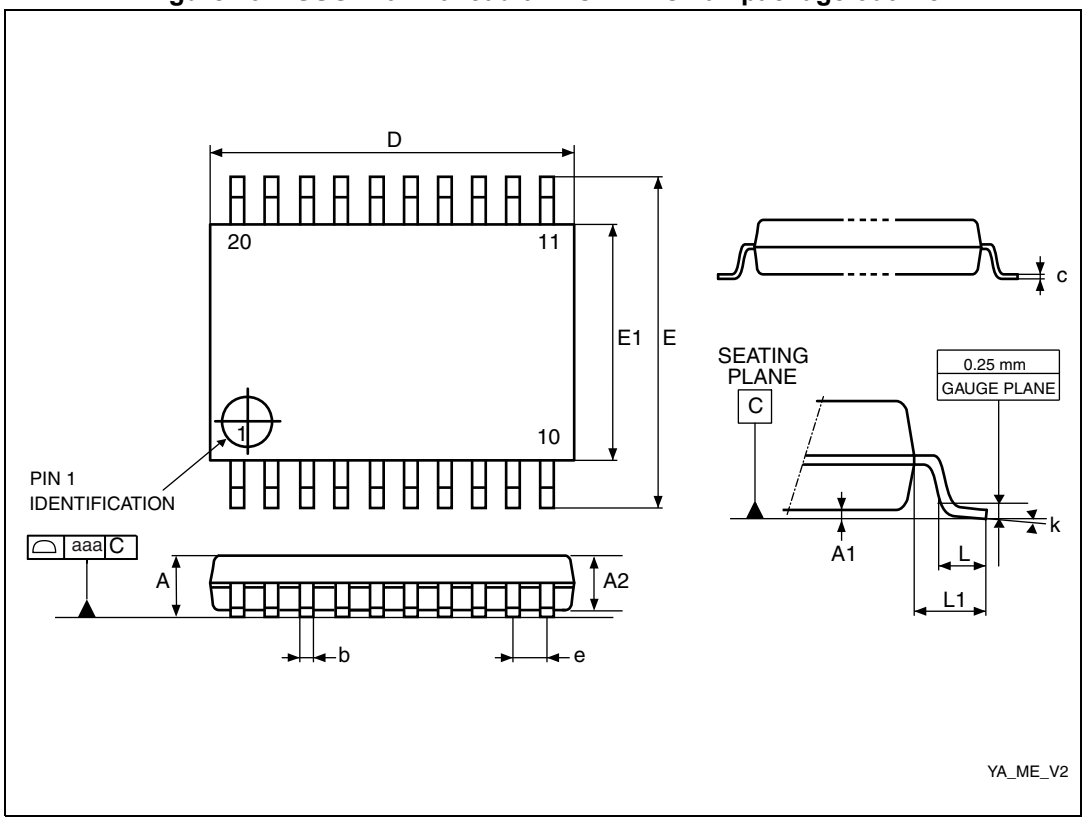
Figure 47. UFQFPN20 recommended footprint



1. Dimensions are in millimeters.

10.5 TSSOP20 package information

Figure 49. TSSOP20 - 20-lead thin shrink small package outline



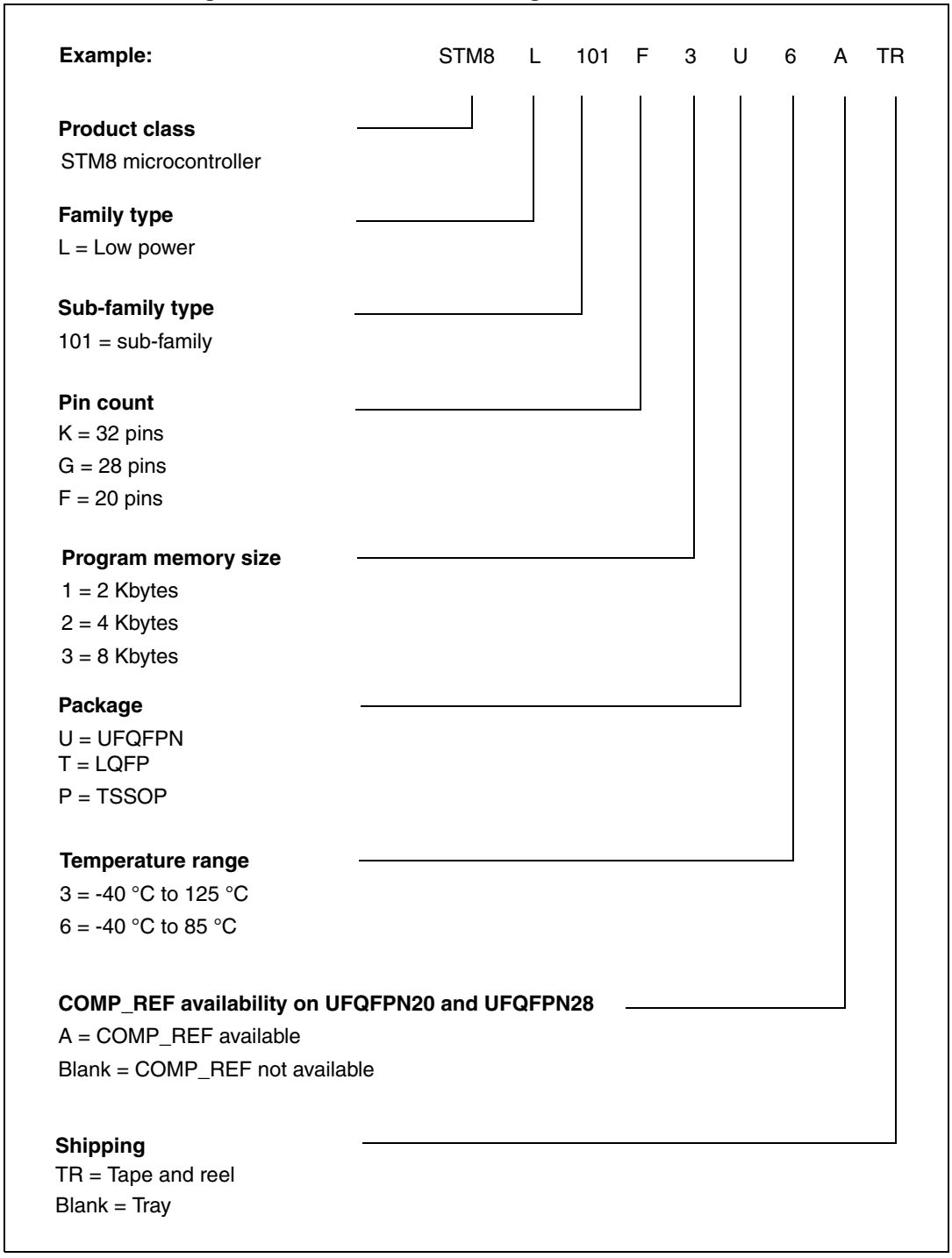
1. Drawing is not to scale.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data

Dim.	mm				inches(1)	
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
CP	-	-	0.100	-	-	0.0039
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	0.1693	0.0256	-
L	0.450	0.600	0.750	0.1693	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

11 Device ordering information

Figure 52. STM8L101xx ordering information scheme



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows the user to assemble and link their application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user's application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

Table 44. Document revision history (continued)

Date	Revision	Changes
12-Jun-2009	6	Removed TSSOP28 package Modified consumption value on first page Added BEEP_CSR (address 00 50F3h) in *Table 7: General hardware register map on page 25* TIM2_PSCRL replaced with TIM2_PSCR and CLK_PCKEN replaced with CLK_PCKENR in *Table 7: General hardware register map on page 25* Added graphs in *Section 9: Electrical parameters on page 37* Added t_{WU}(AH) and t_{WU}(Halt) max values in *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44* Modified *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44* Updated *Table 22: HSI oscillator characteristics on page 45*, *Table 23: LSI oscillator characteristics on page 47* and *Table 24: RAM and hardware registers on page 47* Modified *Table 27: Output driving current (High sink ports) on page 51* Removed note 1 in *Table 37: Electrical sensitivities on page 62* Added note to *Table 39: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data on page 67* and *Table 41: UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package (4 x 4), package mechanical data on page 70*

Table 44. Document revision history (continued)

Date	Revision	Changes
29-Nov-2009	8	Modified status of the document (datasheet instead of preliminary data) Replaced WFQFPN32 with UFQFPN32 and WFQFPN28 with UFQFPN28. Modified title of the reference manual mentioned in *Section 2: Description on page 9* Added references to “low-density” in *Section 2: Description on page 9*, *Section 3.5: Memory on page 12* and in *Figure 8: Memory map on page 23* Modified *Figure 8: Memory map on page 23* (unique ID are added) *Table 7: General hardware register map on page 25*: Modified reserved areas and IR block replaced with IRTIM block Modified t_{TEMP} in *Table 17: Operating conditions at power-up / power-down on page 41* Modified *Table 23: LSI oscillator characteristics on page 47* Modified *Table 25: Flash program memory on page 47* (t_{PROG}) Modified *Table 16: General operating conditions on page 40* and *Table 38: Thermal characteristics on page 63* Modified *Section 13: Revision history on page 82*
18-Jun-2010	9	Modified *Introduction* and *Description* Modified one reserved area (0x00 5055 to 0x00 509F) in *Table 7: General hardware register map* Modified*Table 4: STM8L101xx pin description*: modified note 2 and removed “wpu” for PC0 and PC1 Removed one note to *Table 22: HSI oscillator characteristics on page 45* Modified first paragraph in *Section : NRST pin* Modified OPT3 description in *Table 11: Option byte description* Added note 5 to *Table 18: Total current consumption in Run mode* Modified $V_{ESD(CDM)}$ in *Table 36: ESD absolute maximum ratings on page 61* Modified *Figure 36: Typical application with I2C bus and timing diagram 1) on page 59* Modified COMP_REF availability information in *Figure 52: STM8L101xx ordering information scheme on page 79* Modified *Section 12.2: Software tools on page 78*
21-Jul-2010	10	Modified *Table 3: Legend/abbreviation for table 4 on page 20* and *Table 4: STM8L101xx pin description on page 20* (for PA0, PA1, PB0 and PB4) Modified *Table 13: Voltage characteristics on page 38* and *Table 14: Current characteristics on page 39* Modified V_{IH} in *Table 26: I/O static characteristics on page 48* Added notes below UFQFPN32 package