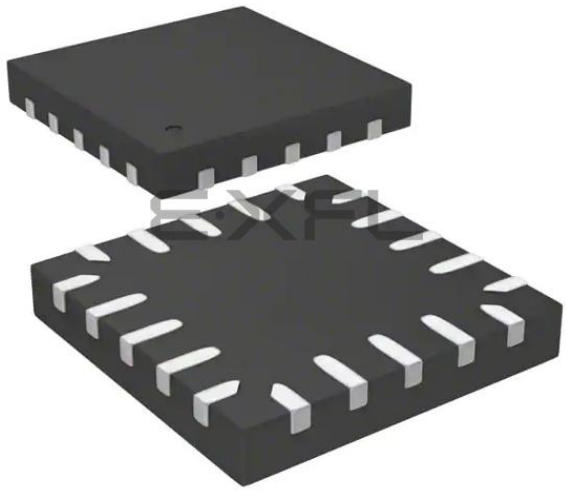

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f2u6tr

List of figures

2 Description

The STM8L101x1 STM8L101x2 STM8L101x3 low-power family features the enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All STM8L101xx microcontrollers feature low power low-voltage single-supply program Flash memory. The 8-Kbyte devices embed data EEPROM.

The STM8L101xx low power family is based on a generic set of state-of-the-art peripherals. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

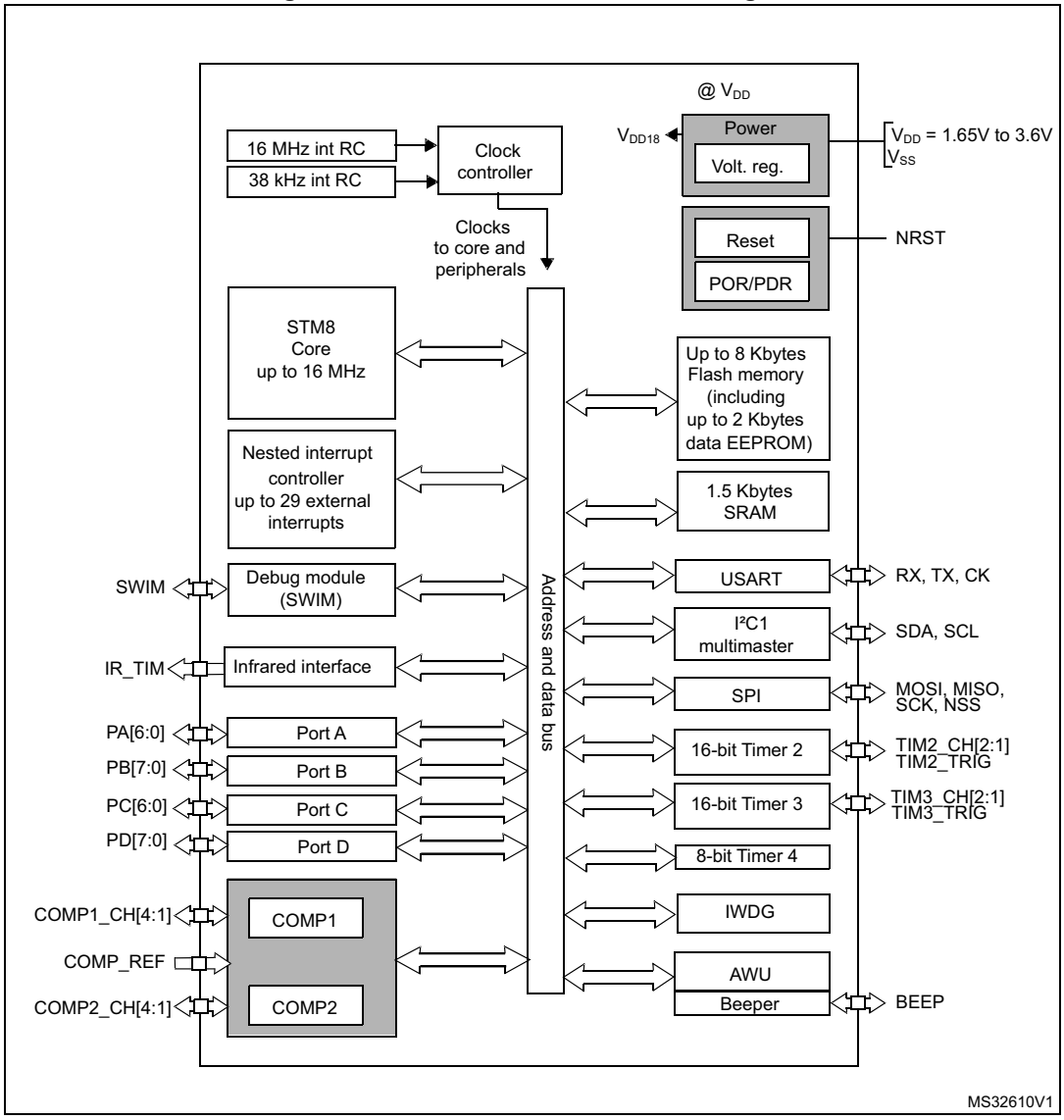
All STM8L low power products are based on the same architecture with the same memory mapping and a coherent pinout.

Table 2. STM8L101xx device feature summary

Features	STM8L101xx		
Flash	2 Kbytes of Flash program memory	4 Kbytes of Flash program memory	8 Kbytes of Flash program memory including up to 2 Kbytes of Data EEPROM
RAM	1.5 Kbytes		
Peripheral functions	Independent watchdog (IWDG), Auto-wakeup unit (AWU), Beep, Serial peripheral interface (SPI), Inter-integrated circuit (I²C), Universal synchronous / asynchronous receiver / transmitter (USART), 2 comparators, Infrared (IR) interface		
Timers	Two 16-bit timers, one 8-bit timer		
Operating voltage	1.65 to 3.6 V		
Operating temperature	-40 to +85 °C		-40 to +85 °C or -40 to +125 °C
Packages	UFQFPN20 3x3	UFQFPN28 4x 4 UFQFPN20 3x3 TSSOP20 4.4 x 6.4	UFQFPN28 4x4 UFQFPN20 3x3 UFQFPN32 LQFP32

3 Product overview

Figure 1. STM8L101xx device block diagram

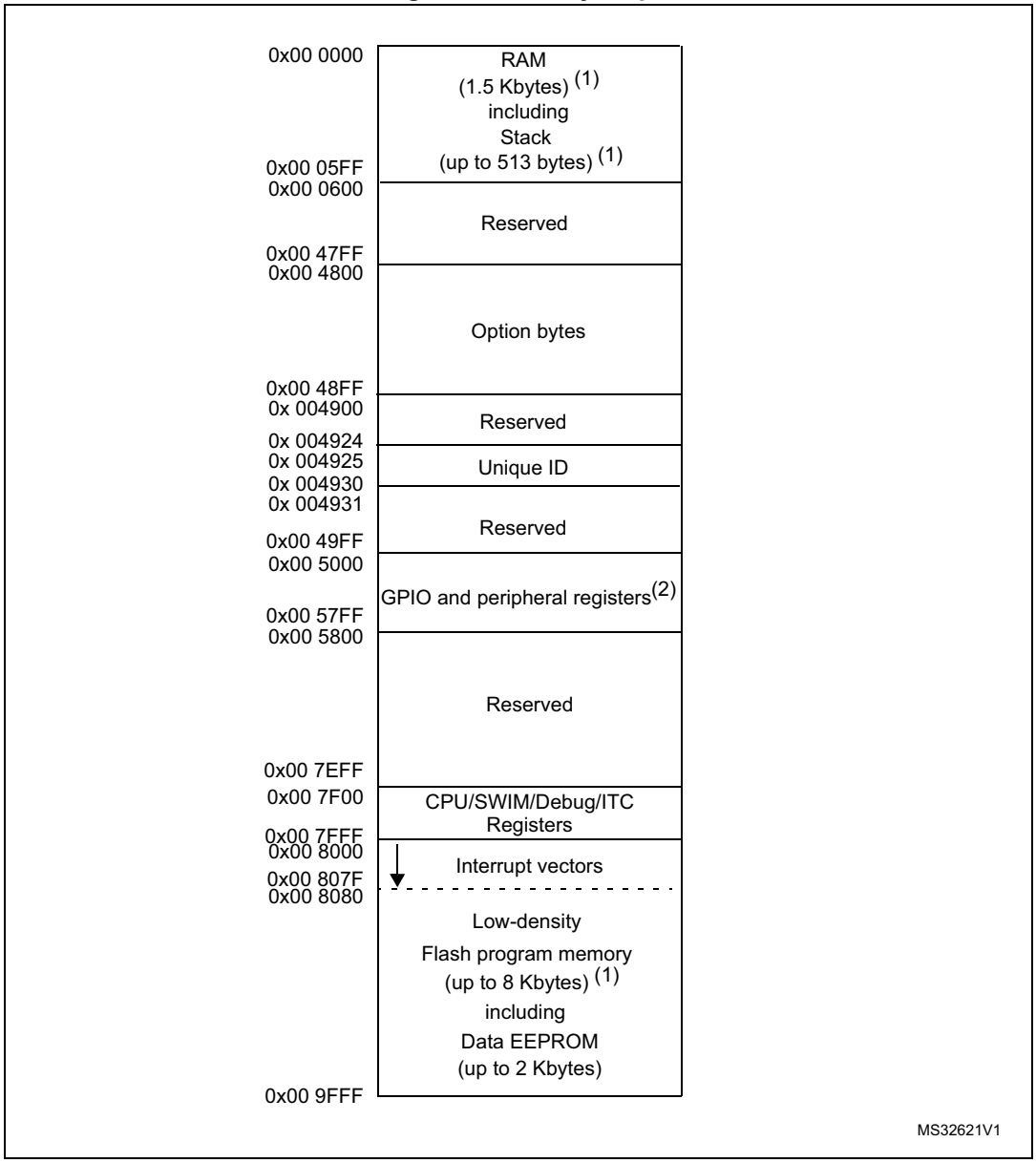


Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog

5 Memory and register map

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5255		TIM2_SR1	TIM2 status register 1	0x00
0x00 5256		TIM2_SR2	TIM2 status register 2	0x00
0x00 5257		TIM2_EGR	TIM2 event generation register	0x00
0x00 5258		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5259		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525B		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525C		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525D		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525E		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 525F		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5260		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5261		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5262		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5263		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5264		TIM2_BKR	TIM2 break register	0x00
0x00 5265		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5266 to 0x00 527F	Reserved area (26 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E9 to 0x00 52FE	Reserved area (23 bytes)			
0x00 52FF	IRTIM	IR_CR	Infra-red control register	0x00
0x00 5300	COMP	COMP_CR	Comparator control register	0x00
0x00 5301		COMP_CSR	Comparator status register	0x00
0x00 5302		COMP_CCS	Comparator channel selection register	0x00

Table 8. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x80
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x05
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CC	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CFG	CFG_GCR	Global configuration register	0x00
0x00 7F61 0x00 7F6F	Reserved area (15 bytes)			
0x00 7F70	ITC-SPR (1)	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF

Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	Breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	Breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	Breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	Breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	Breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	Breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	Debug module control register 1	0x00
0x00 7F97		DM_CR2	Debug module control register 2	0x00
0x00 7F98		DM_CSR1	Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	Enable function register	0xFF

1. Refer to *Table 7: General hardware register map on page 25* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

Table 11. Option byte description (continued)

OPT3	**DATASIZE[7:0]** Size of the data EEPROM area 0x00: no data EEPROM area (1) 0x01: 1 page reserved for data storage from 0x9FC0 to 0x9FFF(1) 0x02: 2 pages reserved for data storage from 0x9F80 to 0x9FFF(1) ... (1) 0x20: 32 pages reserved for data storage from 0x9800 to 0x9FFF(1) Refer to *Data EEPROM (DATA)* section in the STM8L reference manual (RM0013) for more details. DATASIZE[7:6] are forced to 0 internal by HW.
OPT4	**IWDG_HW:** *Independent watchdog* 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: *Independent window watchdog reset on Halt/Active-halt* 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode

1. 0x00 is the only allowed value for 4 Kbyte STM8L101xx devices.

Caution: After a device reset, read access to the program memory is not guaranteed if address 0x4807 is not programmed to 0x00.

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Note: The values given at 85 °C <T_A ≤ 125 °C are only valid for suffix 3 versions.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

Figure 9. Pin loading conditions

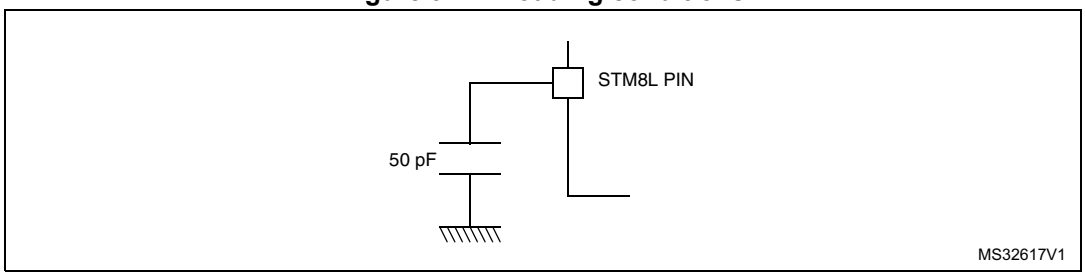


Table 19. Total current consumption in Wait mode(1)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
$I_{DD\ (Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals off, HSI internal RC osc.	f_{MASTER} = 2 MHz	245	400	µA
			f_{MASTER} = 4 MHz	300	450	
			f_{MASTER} = 8 MHz	380	600	
			f_{MASTER} = 16 MHz	510	800	

1. Based on characterization results, unless otherwise specified.
2. Maximum values are given for T_A = -40 to 125 °C.

Figure 13. $I_{DD(WAIT)}$ vs. V_{DD}, f_{CPU} = 2 MHz

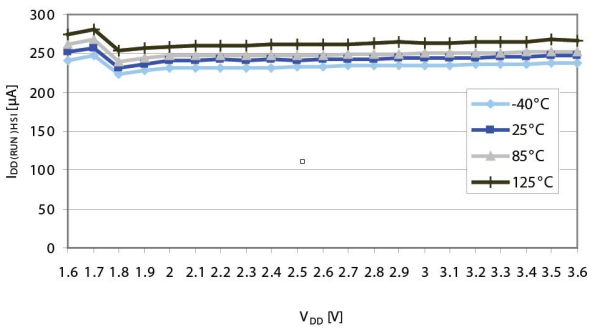
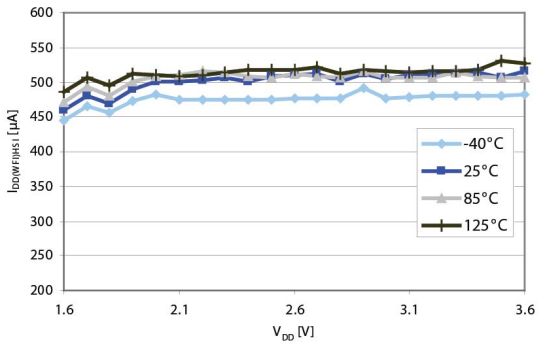


Figure 14. $I_{DD(WAIT)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Figure 21. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

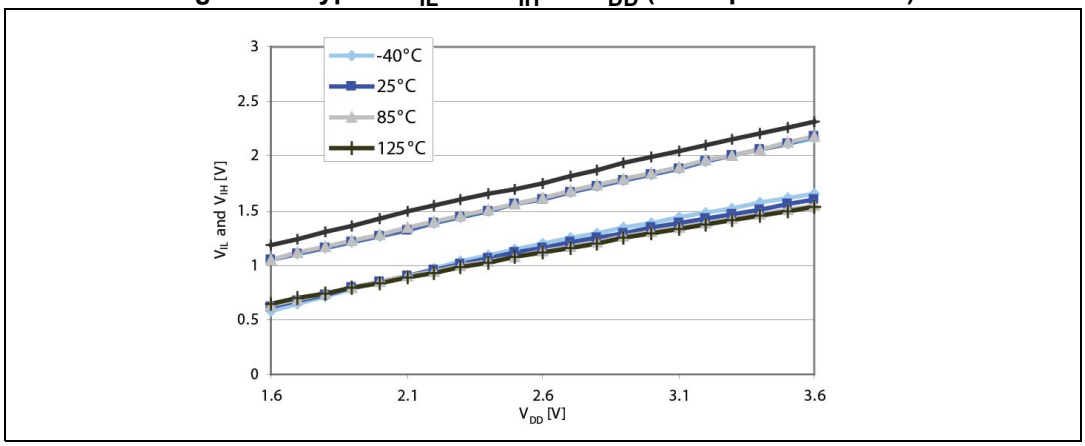


Figure 22. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

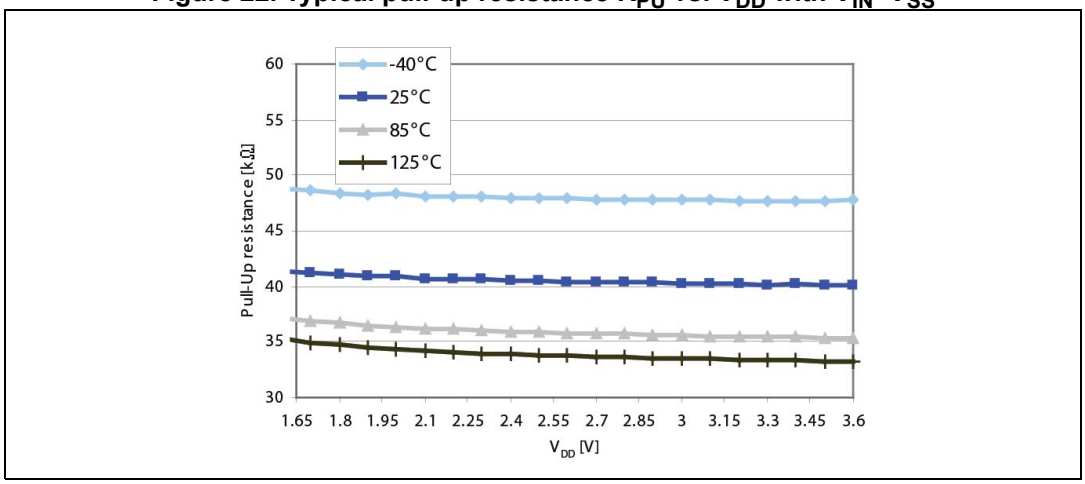


Figure 23. Typical pull-up current I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

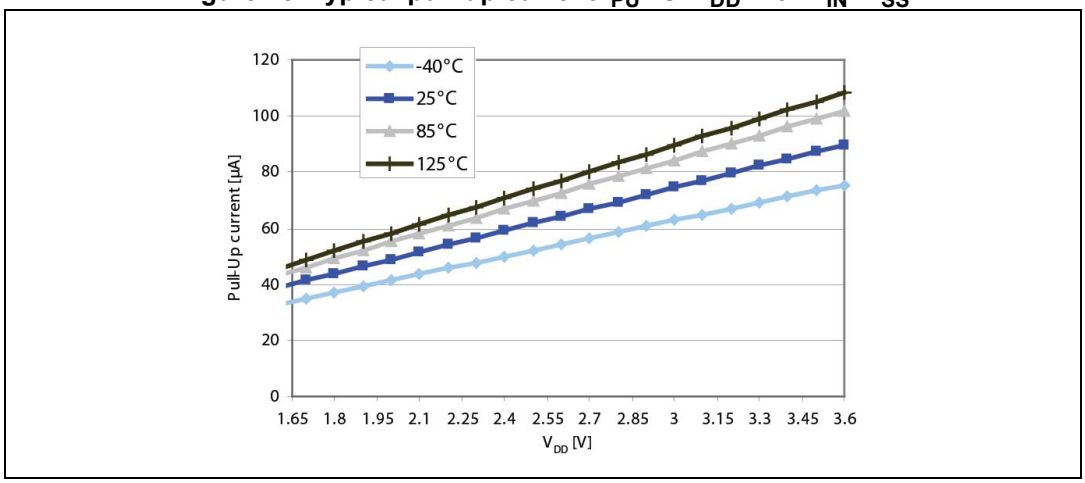
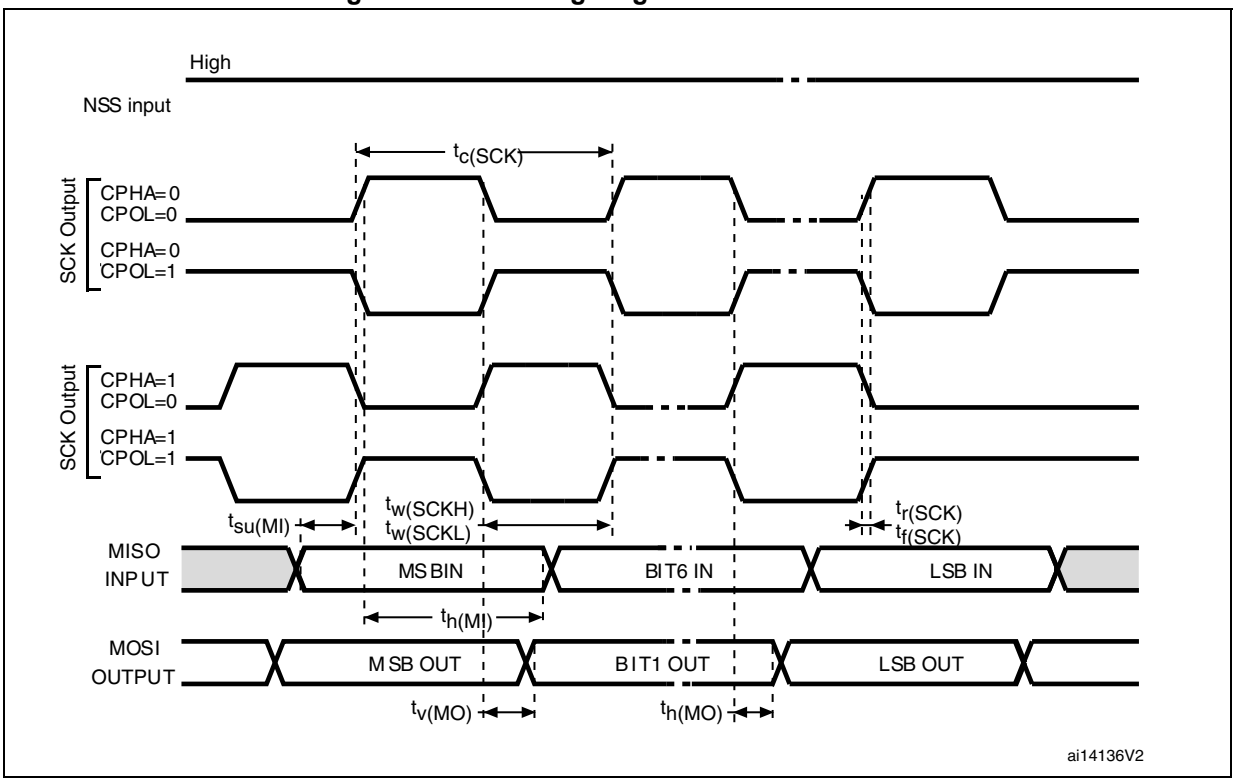


Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 35. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP32 conforming to IEC61967-2	0.1 MHz to 30 MHz	-3	dBµV
			30 MHz to 130 MHz	-6	
			130 MHz to 1 GHz	-5	
			SAE EMI Level	1	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin).

This test conforms to the JESD22-A114A/A115A standard.

Table 36. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results, not tested in production.

Table 38. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W
	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	25	°C/W
	Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm	80	°C/W
	Thermal resistance junction-ambient UFQFPN 20 - 3 x 3 mm - 0.6 mm	102	°C/W
	Thermal resistance junction-ambient TSSOP 20	110	°C/W

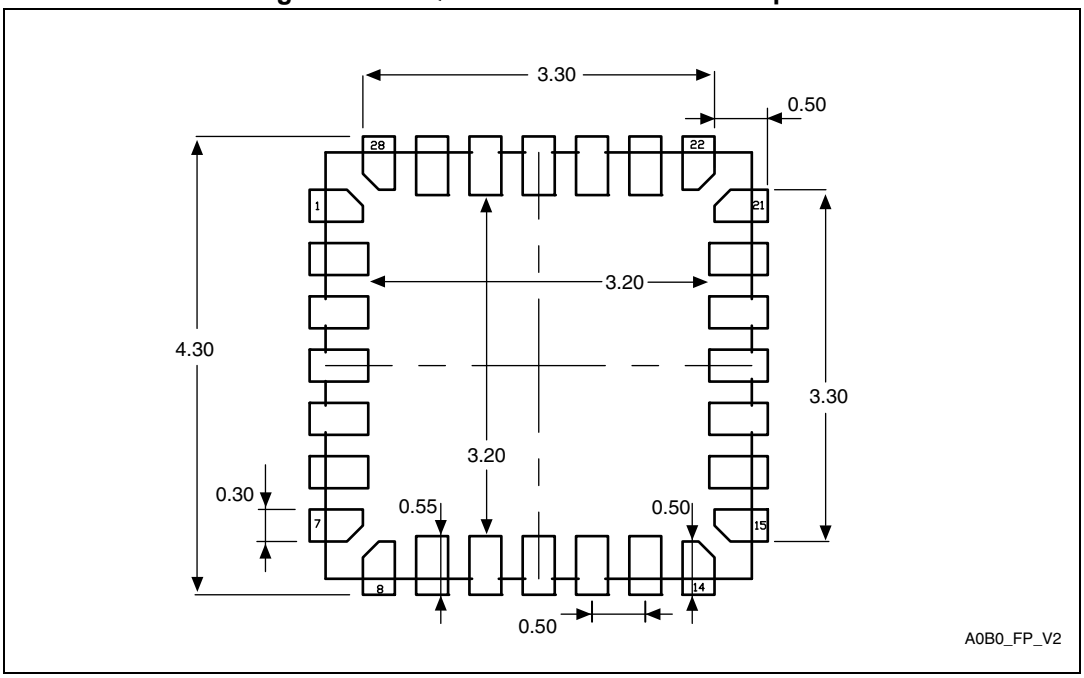
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

Table 41. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package (4 x 4), package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0	0.020	0.050	0	0.0008	0.002
A3	-	0.152	-	-	0.0060	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	-	4.000	-	-	0.1575	-
E	-	4.000	-	-	0.1575	-
e	-	0.500	-	-	0.0197	-
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
L2	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	0.080	-	-	0.0031	-
-	Number of pins					
N	28					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. UFQFPN28 recommended footprint



1. Dimensions are expressed in millimeters.

13 Revision history

Table 44. Document revision history

Date	Revision	Changes
19-Dec-2008	1	Initial release.
22-Apr-2009	2	Added TSSOP28 package Modified packages on first page COMPx_OUT pins removed Added *Figure 6: 28-pin TSSOP package pinout on page 17* Modified *Section 9: Electrical parameters on page 37*. Updated UBC[7:0] description in *Section 7: Option bytes*. Updated low power current consumption on cover page. Updated *Table 13: Voltage characteristics*, *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V*, *Table 26: I/O static characteristics*, *Table 30: NRST pin characteristics*, and *Section 9.3.9: EMC characteristics*. Updated PA1/NRST, PC0 and PC1 in *Table 4: STM8L101xx pin description*. Added ECC feature. Changed internal RC frequency to 38 kHz. Updated electrical characteristics in *Table 16*, *Table 18*, *Table 19*, *Table 20*, *Table 22*, *Table 23*, and *Table 26*.
24-Apr-2009	3	Corrected title on cover page. Changed VFQFPN32 to WFQFPN32 and updated *Table 39: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data*. Updated *Table 13*, *Table 26*, and *Table 33*.
14-May-2009	4	Replaced WFQFPN20 3 x 3 mm 0.8 mm package by UFQFPN20 3 x 3 mm 0.6 mm package (first page, *Table 16: General operating conditions on page 40*, *Table 38: Thermal characteristics on page 63*, *Section 10.2: Package mechanical data on page 67*) Added one UFQFPN20 version with COMP_REF Modified *Figure 40: LQFP32 recommended footprint(1) on page 69* Added I_{PROG} values in *Table 25: Flash program memory on page 47* Updated *Table 31: SPI characteristics on page 55*
15-May-2009	5	Added STM8L101F3U6ATR part number in *Section 4: Pin description on page 15* and in *Figure 47: STM8L101xx ordering information scheme on page 74*