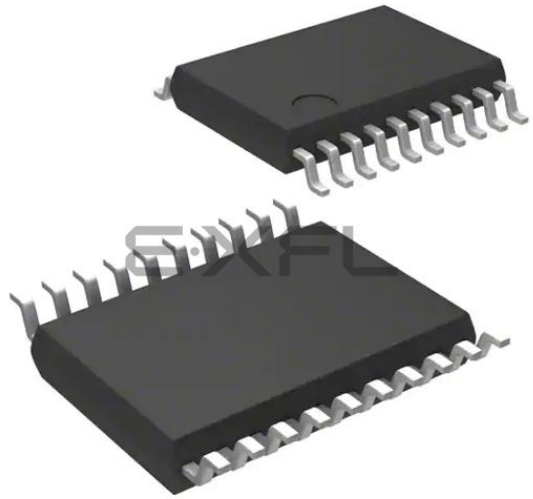

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Applications of "Embedded - Microcontrollers"

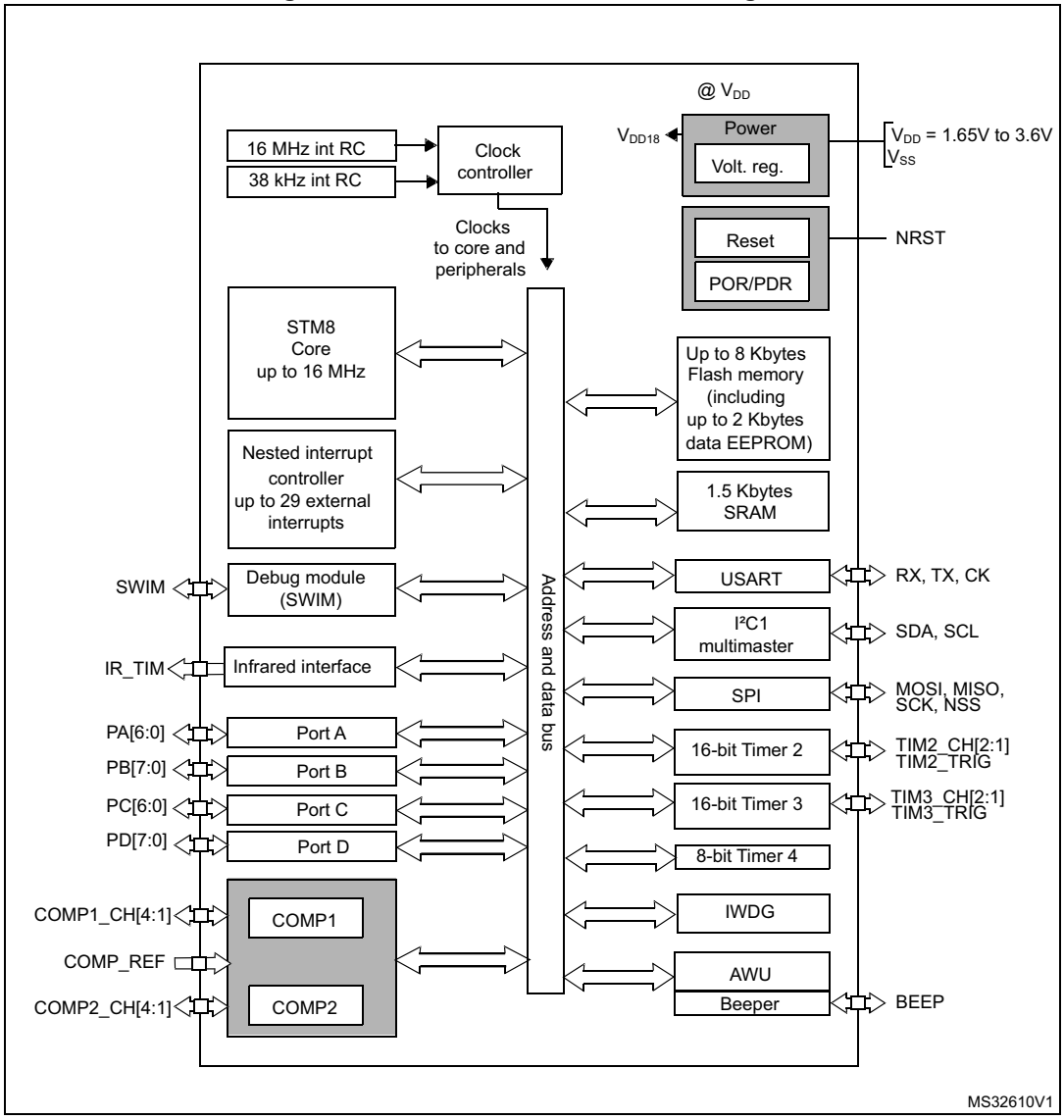
Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f3p6tr

Contents

List of figures

3 Product overview

Figure 1. STM8L101xx device block diagram



Legend:

AWU: Auto-wakeup unit
Int. RC: internal RC oscillator
I²C: Inter-integrated circuit multimaster interface
POR/PDR: Power on reset / power down reset
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous / asynchronous receiver / transmitter
IWDG: Independent watchdog

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 bytes)			

Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	Breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	Breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	Breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	Breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	Breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	Breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	Debug module control register 1	0x00
0x00 7F97		DM_CR2	Debug module control register 2	0x00
0x00 7F98		DM_CSR1	Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	Enable function register	0xFF

1. Refer to *Table 7: General hardware register map on page 25* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated row of the memory.

All option bytes can be modified only in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

Refer to the STM8L Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 10. Option bytes

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT1	ROP[7:0]								0x00
0x4807	-	-	Must be programmed to 0x00								0x00
0x4802	UBC (User Boot code size)	OPT2	UBC[7:0]								0x00
0x4803	DATASIZE	OPT3	DATASIZE[7:0]								0x00
0x4808	Independent watchdog option	OPT4 [1:0]	Reserved						IWDG _HALT	IWDG _HW	0x00

Table 11. Option byte description

OPT1	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) Refer to *Read-out protection* section in the STM8L reference manual (RM0013) for details.
OPT2	**UBC[7:0]** *Size of the user boot code area* 0x00: no UBC 0x01-0x02: UBC contains only the interrupt vectors. 0x03: Page 0 and 1 reserved for the interrupt vectors. Page 2 is available to store user boot code. Memory is write protected ... 0x7F - Page 0 to 126 reserved for UBC, memory is write protected Refer to *User boot area (UBC)* section in the STM8L reference manual (RM0013) for more details. UBC[7] is forced to 0 internally by HW.

9 Electrical parameters

9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A= 25 °C and T_A = T_A max (given by the selected temperature range).

Note: The values given at 85 °C <T_A ≤ 125 °C are only valid for suffix 3 versions.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

9.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3 V. They are given only as design guidelines and are not tested.

9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

Figure 9. Pin loading conditions

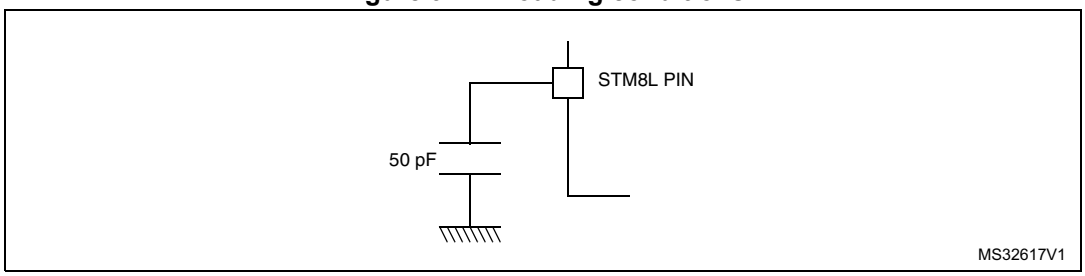


Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	-25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	-5	
	Injected current on any other pin (2)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	±25	

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 18. Total current consumption in Run mode (1)

Symbol	Parameter	Conditions(2)		Typ	Max(3)	Unit
$I_{DD\ (Run)}$	Supply current in Run mode(4) (5)	Code executed from RAM	f_{MASTER} = 2 MHz	0.39	0.60	mA
			f_{MASTER} = 4 MHz	0.55	0.70	
			f_{MASTER} = 8 MHz	0.90	1.20	
			f_{MASTER} = 16 MHz	1.60	2.10(6)	
		Code executed from Flash	f_{MASTER} = 2 MHz	0.55	0.70	
			f_{MASTER} = 4 MHz	0.88	1.80	
			f_{MASTER} = 8 MHz	1.50	2.50	
			f_{MASTER} = 16 MHz	2.70	3.50	

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{MASTER}$
3. Maximum values are given for T_A = –40 to 125 °C.
4. CPU executing typical data processing.
5. An approximate value of $I_{DD(Run)}$ can be given by the following formula: $I_{DD(Run)} = f_{MASTER}$ x 150 µA/MHz +215 µA.
6. Tested in production.

Figure 11. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 2 MHz

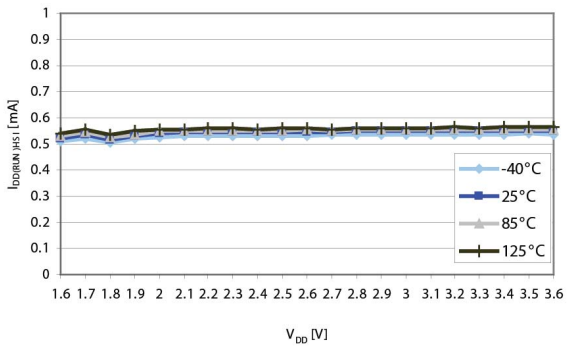
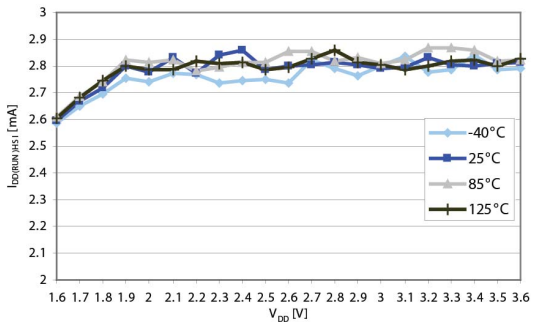


Figure 12. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Table 25. Flash program memory (continued)

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET}	Data retention (program memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	years
	Data retention (data memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	
	Data retention (data memory) after 300k erase/write cycles at T_A = +125 °C	T_{RET} = 85 °C	1(1)	-	-	
N_{RW}	Erase/write cycles (program memory)	See notes (1)(2)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)	See notes (1)(3)	300(1)(4)	-	-	

1. Data based on characterization results, not tested in production.
2. Retention guaranteed after cycling is 10 years at 55 °C.
3. Retention guaranteed after cycling is 1 year at 55 °C.
4. Data based on characterization performed on the whole data memory (2 Kbytes).

9.3.6 I/O port pin characteristics

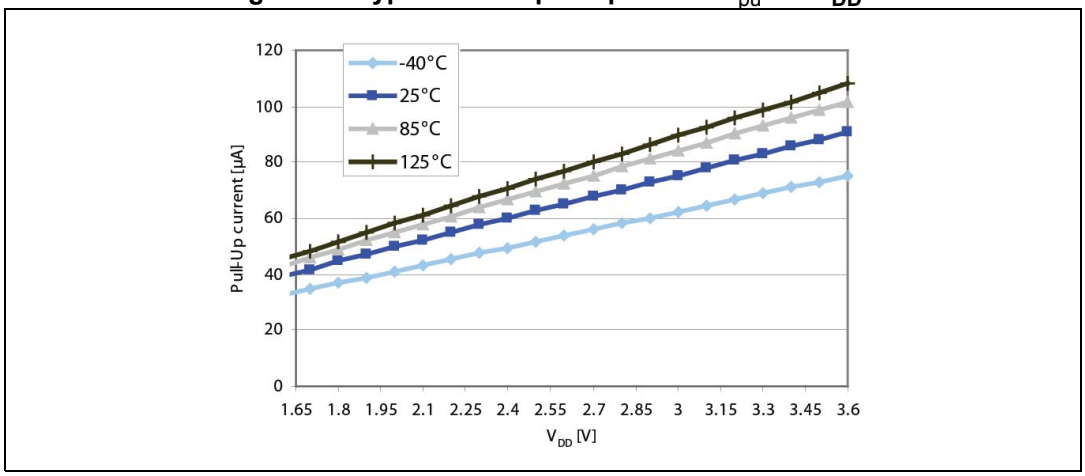
General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 26. I/O static characteristics (1)

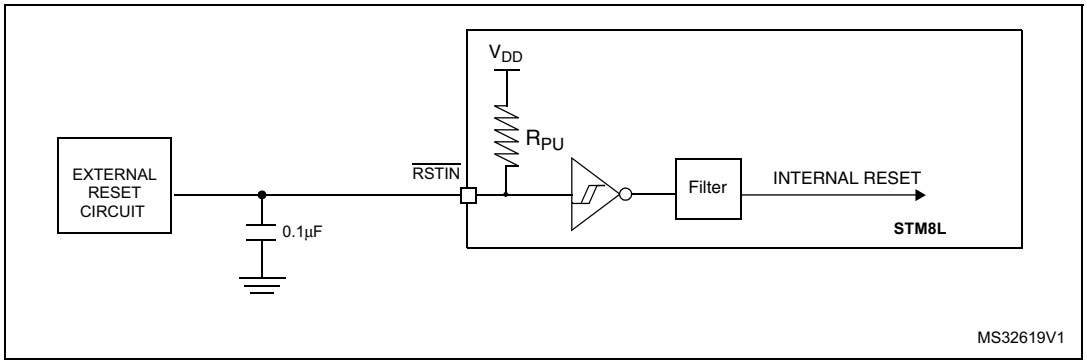
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Standard I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	V
		True open drain I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Standard I/Os	0.70 x V_{DD}	-	V_{DD}+0.3	V
		True open drain I/Os V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		True open drain I/Os V_{DD} ≥ 2 V			5.5	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	250	-	

Figure 31. Typical NRST pull-up current I_{pu} vs. V_{DD}



The reset network shown in *Figure 32* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 30*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 32. Recommended NRST pin configuration



1. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected.
2. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.

Inter IC control interface (I2C)

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

The STM8L I^2C interface meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 32. I2C characteristics

Symbol	Parameter	Standard mode I2C		Fast mode I2C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0 (3)	-	0 (4)	900 (3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SCK} must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance
For other speed ranges, achieved speed can have ±2% tolerance
The above variations depend on the accuracy of the external components used.

Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 37. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 40*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

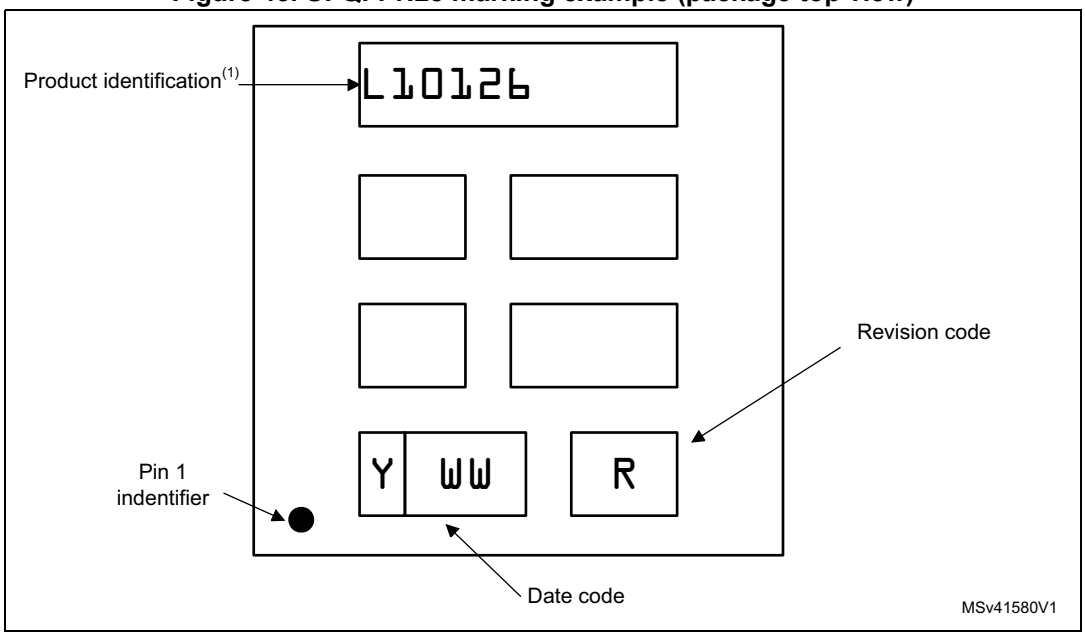
Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. UFQFPN28 marking example (package top view)



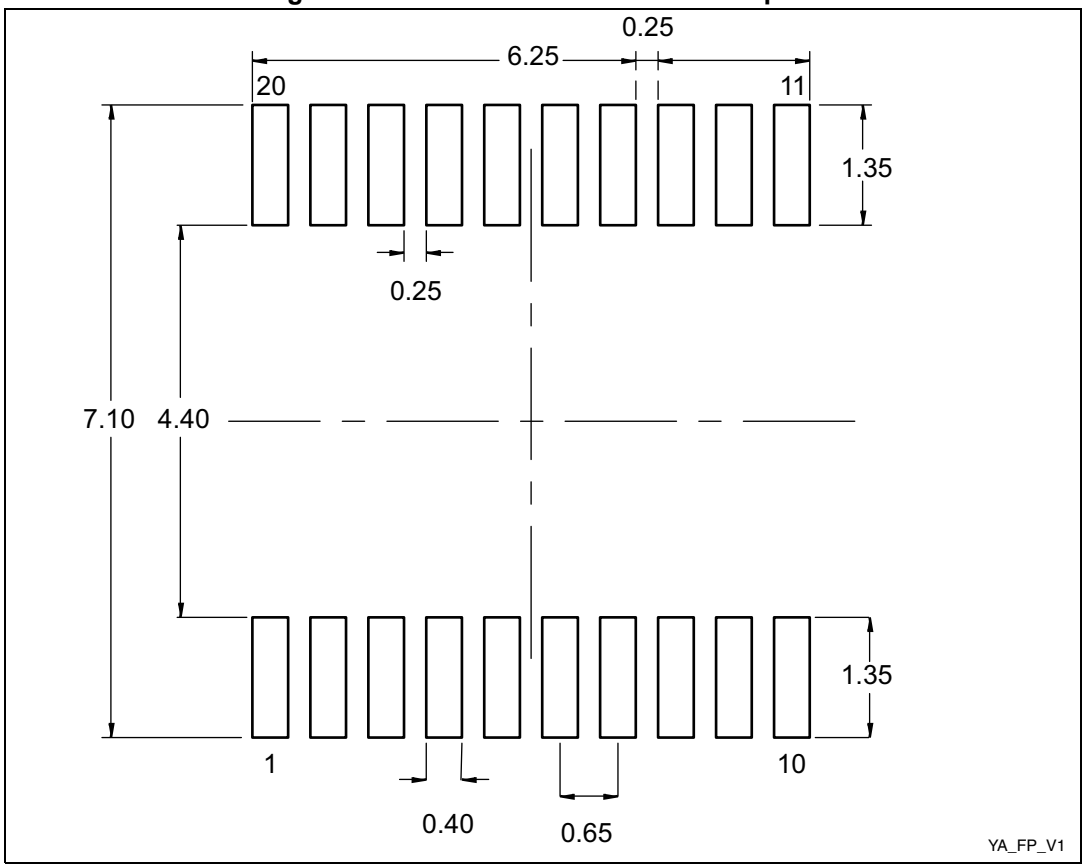
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data (continued)

Dim.	mm				inches[1]	
	Min	Typ	Max	Min	Typ	Max
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039
Number of pins	20					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 50. TSSOP20 recommended footprint

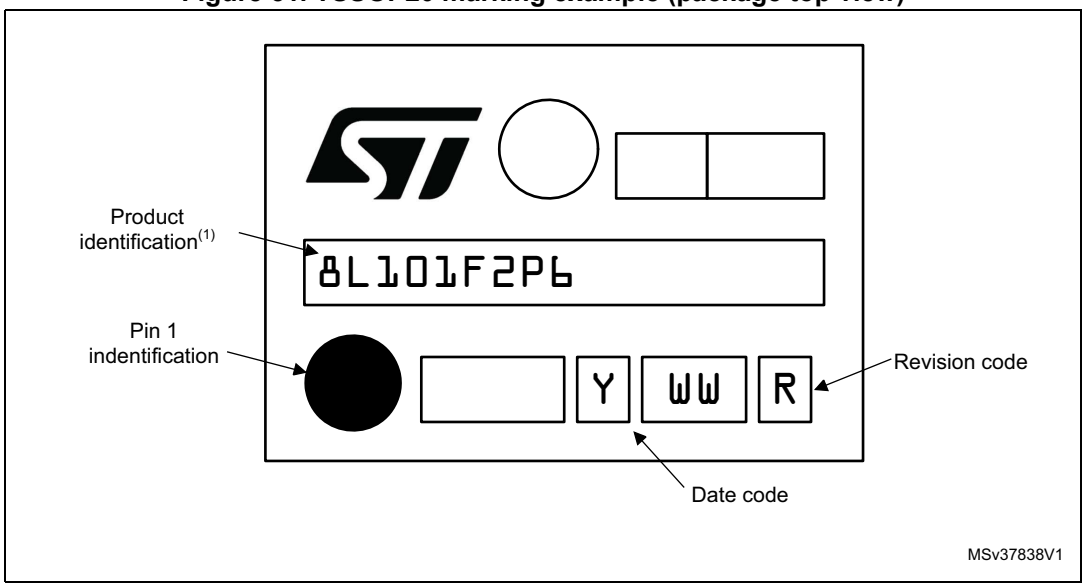


1. Dimensions are in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

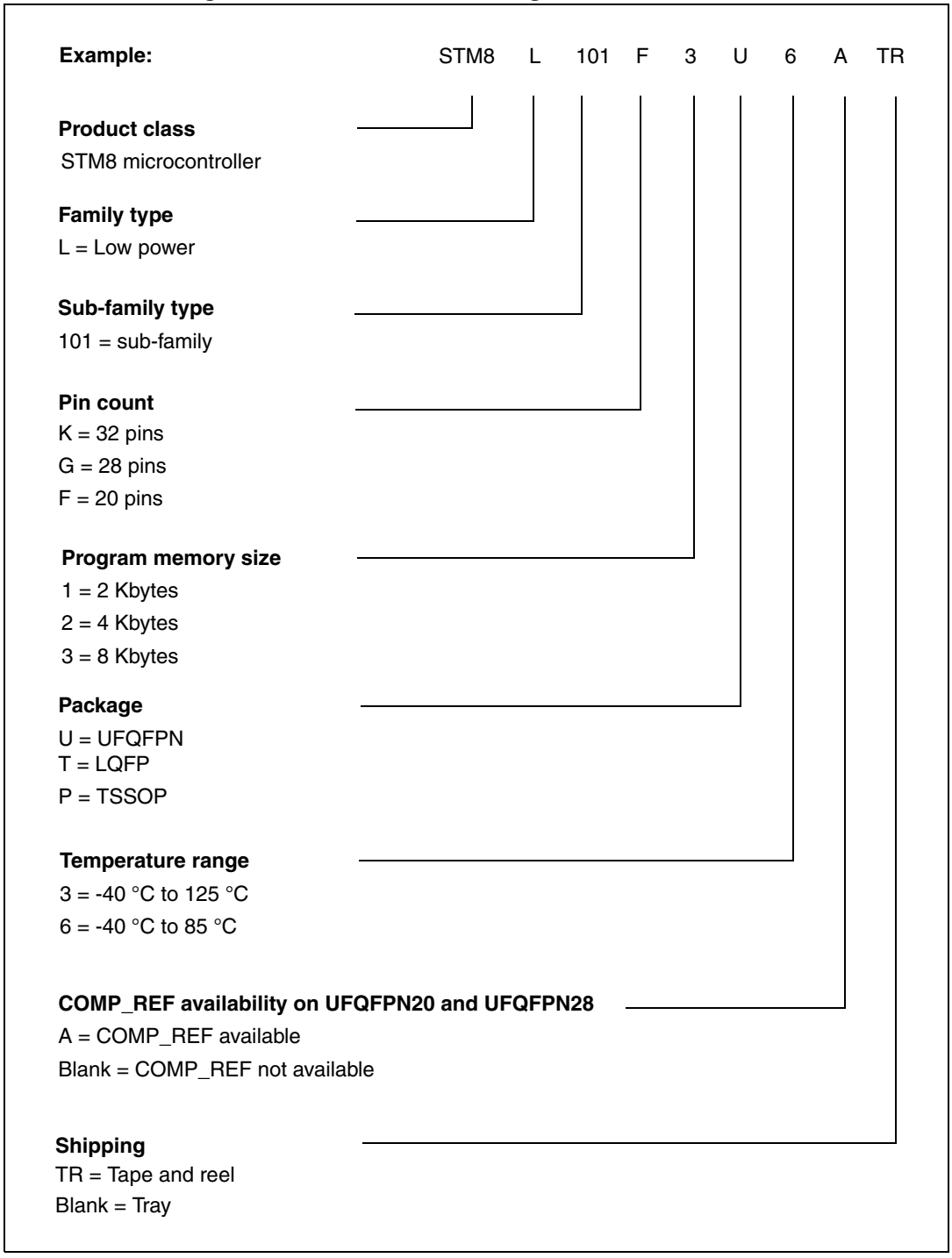
Figure 51. TSSOP20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

11 Device ordering information

Figure 52. STM8L101xx ordering information scheme



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows the users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows the users to specify the components that they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows the user to assemble and link their application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user's application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

13 Revision history

Table 44. Document revision history

Date	Revision	Changes
19-Dec-2008	1	Initial release.
22-Apr-2009	2	Added TSSOP28 package Modified packages on first page COMPx_OUT pins removed Added *Figure 6: 28-pin TSSOP package pinout on page 17* Modified *Section 9: Electrical parameters on page 37*. Updated UBC[7:0] description in *Section 7: Option bytes*. Updated low power current consumption on cover page. Updated *Table 13: Voltage characteristics*, *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V*, *Table 26: I/O static characteristics*, *Table 30: NRST pin characteristics*, and *Section 9.3.9: EMC characteristics*. Updated PA1/NRST, PC0 and PC1 in *Table 4: STM8L101xx pin description*. Added ECC feature. Changed internal RC frequency to 38 kHz. Updated electrical characteristics in *Table 16*, *Table 18*, *Table 19*, *Table 20*, *Table 22*, *Table 23*, and *Table 26*.
24-Apr-2009	3	Corrected title on cover page. Changed VFQFPN32 to WFQFPN32 and updated *Table 39: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data*. Updated *Table 13*, *Table 26*, and *Table 33*.
14-May-2009	4	Replaced WFQFPN20 3 x 3 mm 0.8 mm package by UFQFPN20 3 x 3 mm 0.6 mm package (first page, *Table 16: General operating conditions on page 40*, *Table 38: Thermal characteristics on page 63*, *Section 10.2: Package mechanical data on page 67*) Added one UFQFPN20 version with COMP_REF Modified *Figure 40: LQFP32 recommended footprint(1) on page 69* Added I_{PROG} values in *Table 25: Flash program memory on page 47* Updated *Table 31: SPI characteristics on page 55*
15-May-2009	5	Added STM8L101F3U6ATR part number in *Section 4: Pin description on page 15* and in *Figure 47: STM8L101xx ordering information scheme on page 74*