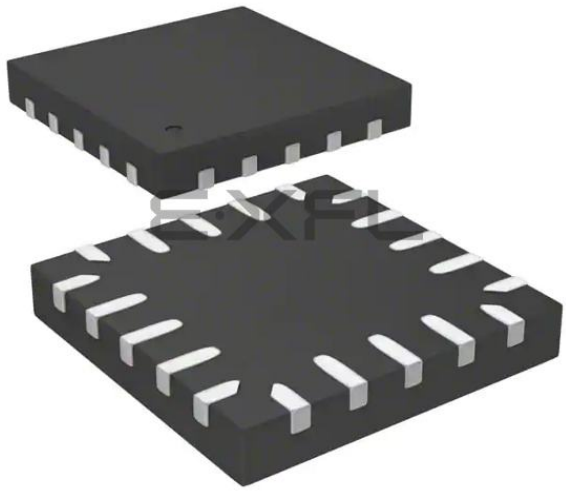

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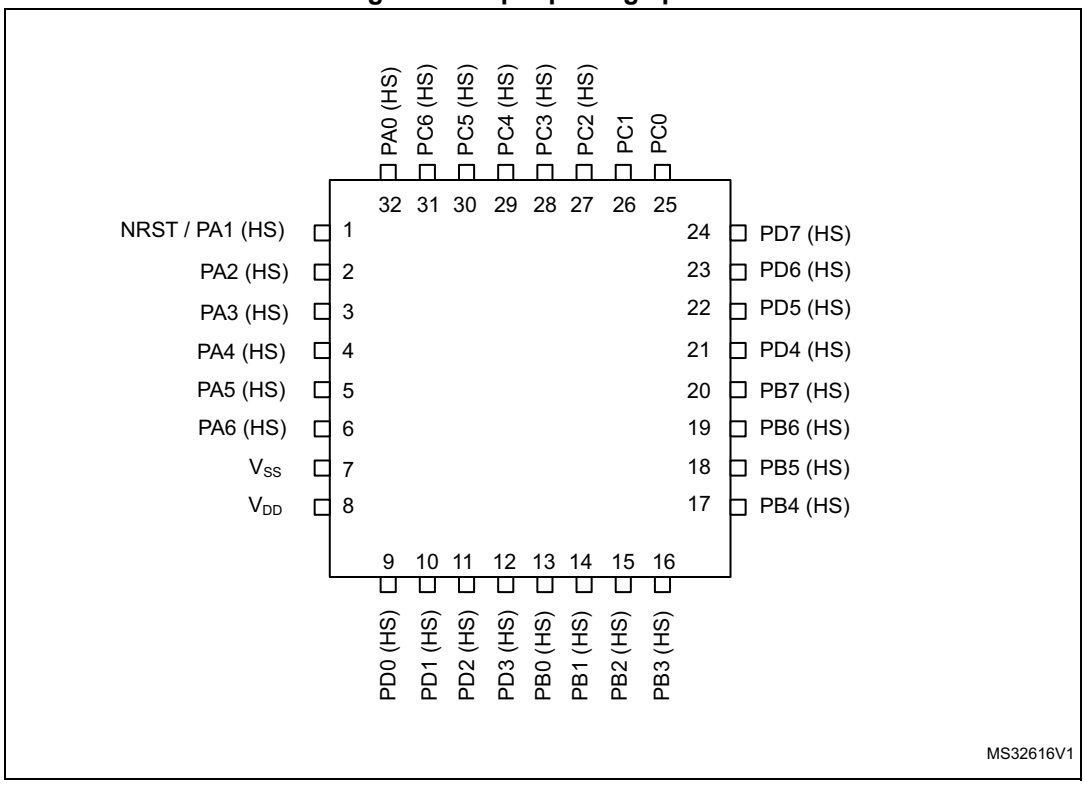
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN
Supplier Device Package	20-UFQFPN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101f3u6tr

Contents

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5285		TIM3_SR1	TIM3 status register 1	0x00
0x00 5286		TIM3_SR2	TIM3 status register 2	0x00
0x00 5287		TIM3_EGR	TIM3 event generation register	0x00
0x00 5288		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5289		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 528A		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 528B		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528C		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528D		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528E		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 528F		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 5290		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 5291		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 5292		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5293		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5294		TIM3_BKR	TIM3 break register	0x00
0x00 5295		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5296 to 0x00 52DF	Reserved area (74 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E4		TIM4_SR1	TIM4 Status register 1	0x00
0x00 52E5		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E6		TIM4_CNTR	TIM4 counter	0x00
0x00 52E7		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E8		TIM4_ARR	TIM4 auto-reload register low	0xFF

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)	Vector address
27	USART	Transmission complete/transmit data register empty	-	-	Yes	Yes(1)	0x00 8074
28	USART	Receive Register DATA FULL/overrun/idle line detected/parity error	-	-	Yes	Yes(1)	0x00 8078
29	I2C	I2C interrupt(2)	Yes	Yes	Yes	Yes(1)	0x00 807C

1. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. Refer to Section *Wait for event (WFE) mode* in the RM0013 reference manual.
2. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

Table 11. Option byte description (continued)

OPT3	**DATASIZE[7:0]** Size of the data EEPROM area 0x00: no data EEPROM area (1) 0x01: 1 page reserved for data storage from 0x9FC0 to 0x9FFF(1) 0x02: 2 pages reserved for data storage from 0x9F80 to 0x9FFF(1) ... (1) 0x20: 32 pages reserved for data storage from 0x9800 to 0x9FFF(1) Refer to *Data EEPROM (DATA)* section in the STM8L reference manual (RM0013) for more details. DATASIZE[7:6] are forced to 0 internal by HW.
OPT4	**IWDG_HW:** *Independent watchdog* 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: *Independent window watchdog reset on Halt/Active-halt* 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode

1. 0x00 is the only allowed value for 4 Kbyte STM8L101xx devices.

Caution: After a device reset, read access to the program memory is not guaranteed if address 0x4807 is not programmed to 0x00.

Figure 16. Typical HSI frequency vs. V_{DD}

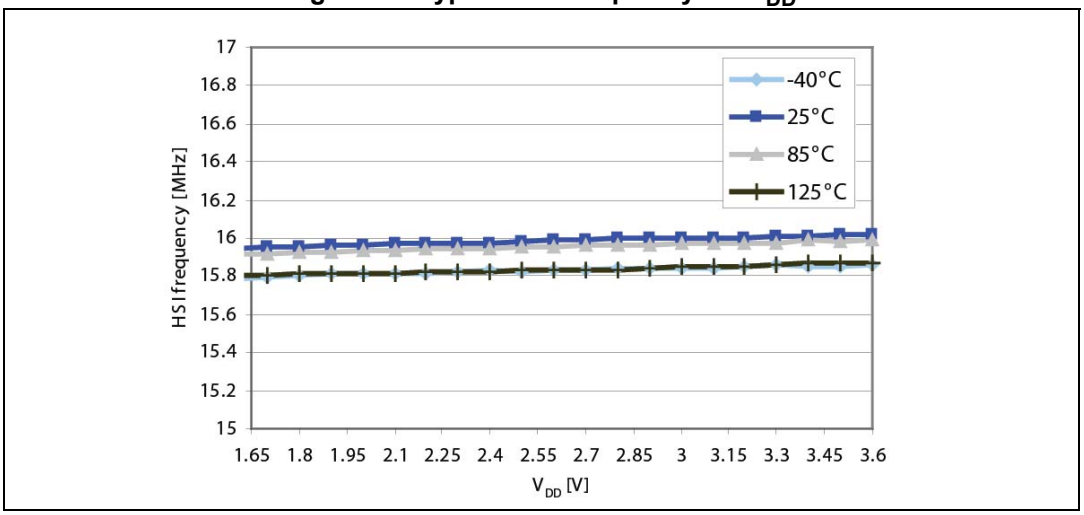


Figure 17. Typical HSI accuracy vs. temperature, V_{DD} = 3 V

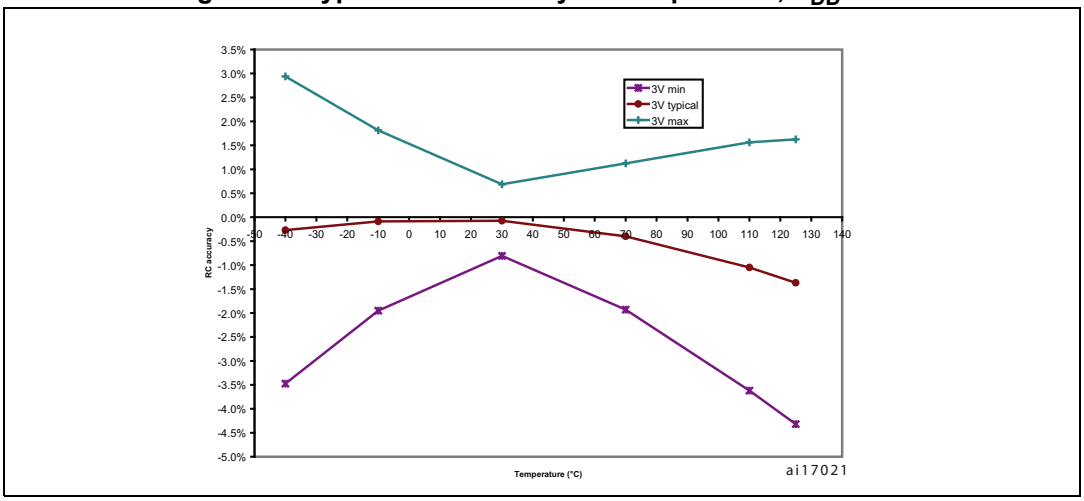
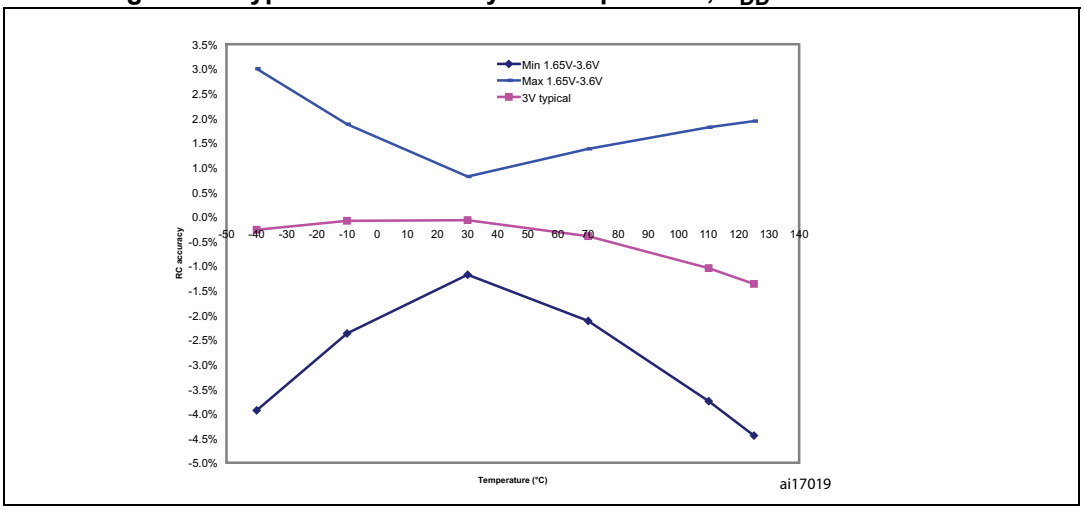


Figure 18. Typical HSI accuracy vs. temperature, V_{DD} = 1.65 V to 3.6 V



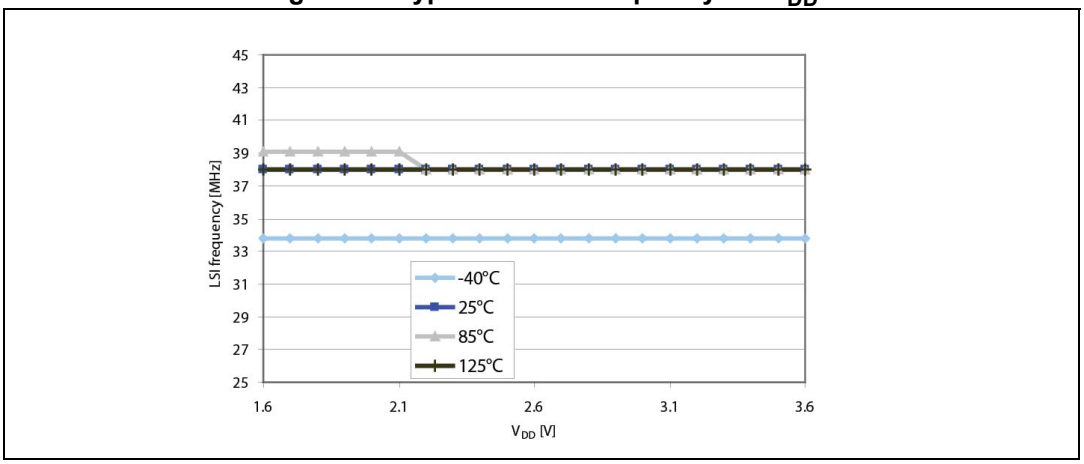
Low speed internal RC oscillator (LSI)

Table 23. LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$f_{drift(LSI)}$	LSI oscillator frequency drift(2)	0 °C ≤T_A ≤85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

Figure 19. Typical LSI RC frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 24. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.4	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 25. Flash program memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{MASTER} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1- or 64-byte (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1- to 64-byte (block) write cycles (on erased byte)	-	-	3	-	ms

Table 25. Flash program memory (continued)

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET}	Data retention (program memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	years
	Data retention (data memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	
	Data retention (data memory) after 300k erase/write cycles at T_A = +125 °C	T_{RET} = 85 °C	1(1)	-	-	
N_{RW}	Erase/write cycles (program memory)	See notes (1)(2)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)	See notes (1)(3)	300(1)(4)	-	-	

1. Data based on characterization results, not tested in production.
2. Retention guaranteed after cycling is 10 years at 55 °C.
3. Retention guaranteed after cycling is 1 year at 55 °C.
4. Data based on characterization performed on the whole data memory (2 Kbytes).

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 26. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Standard I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	V
		True open drain I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Standard I/Os	0.70 x V_{DD}	-	V_{DD}+0.3	V
		True open drain I/Os V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		True open drain I/Os V_{DD} ≥ 2 V			5.5	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	250	-	

NRST pin

The NRST pin input driver is CMOS. A permanent pull-up is present.
$R_{PU(NRST)}$ has the same value as R_{PU} (see *Table 26 on page 48*).

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 30. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2 mA	-	-	V_{DD}-0.8	
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (2)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$t_{OP(NRST)}$	NRST output pulse width	-	20	-	-	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	ns

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (*Figure 30*). Corresponding I_{PU} current characteristics are described in *Figure 31*.
3. Data guaranteed by design, not tested in production.

Figure 30. Typical NRST pull-up resistance R_{PU} vs. V_{DD}

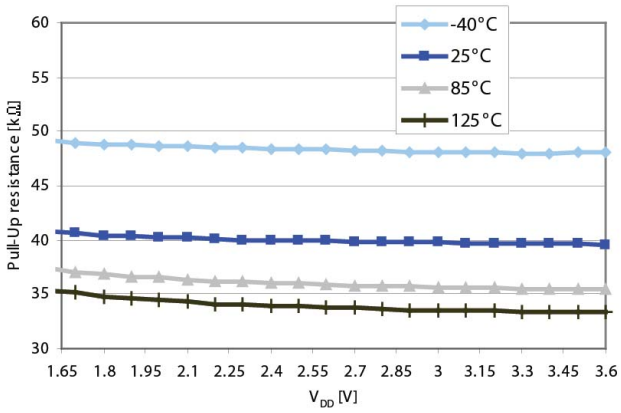


Figure 33. SPI timing diagram - slave mode and CPHA = 0

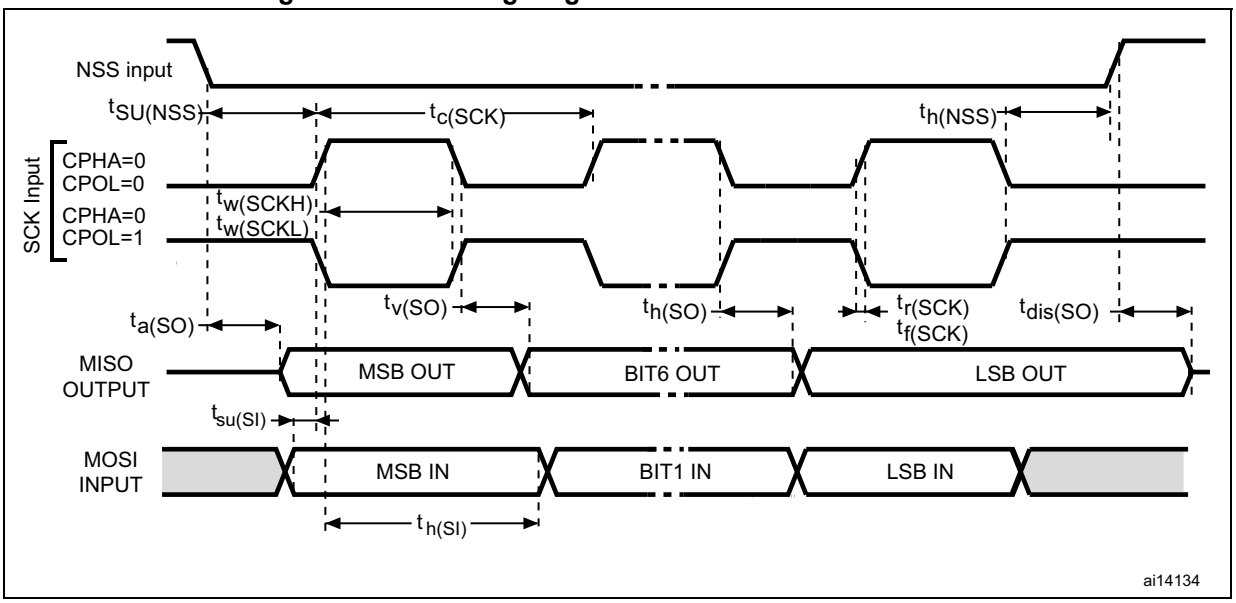
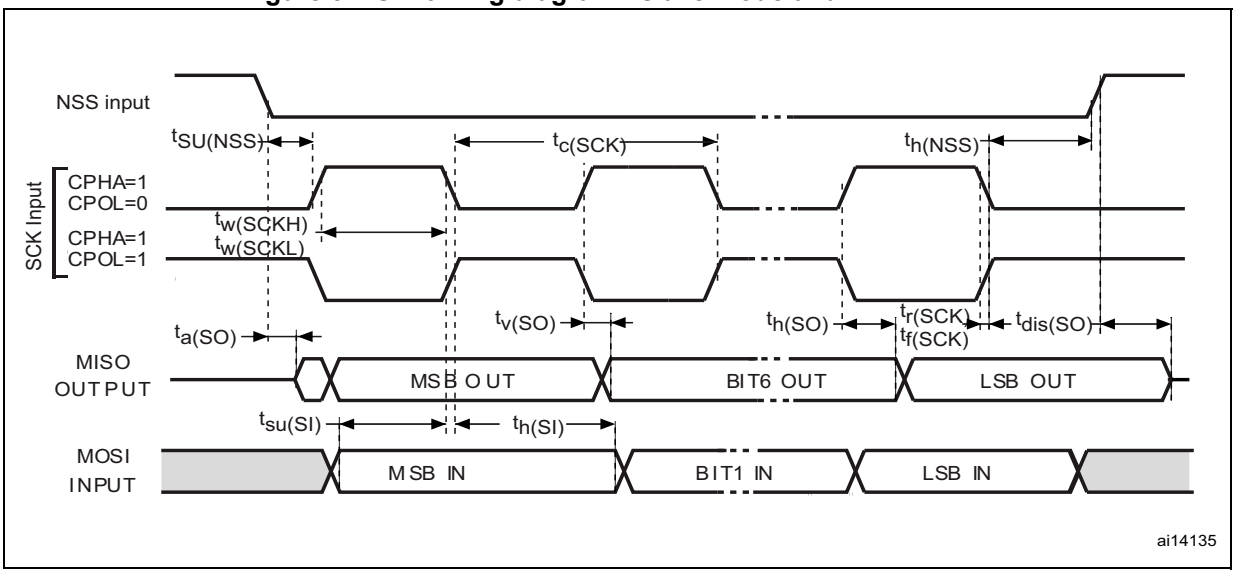
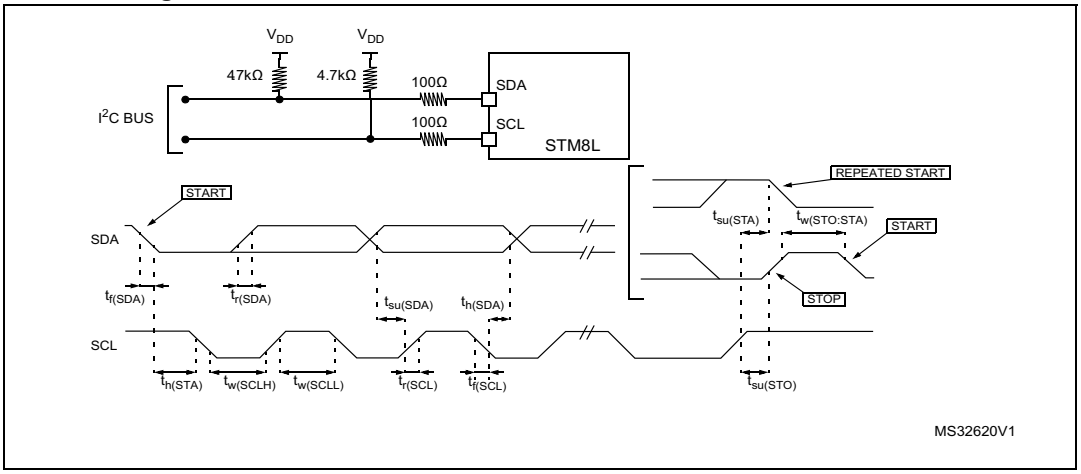


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 36. Typical application with I2C bus and timing diagram 1)



1. Measurement points are done at CMOS levels: 0.3 x V_{DD} and 0.7 x V_{DD}.

9.3.8 Comparator characteristics

Table 33. Comparator characteristics

Symbol	Parameter	Conditions	Min (1)	Typ	Max(1)	Unit
$V_{IN(COMP\_REF)}$	Comparator external reference	-	-0.1	-	V_{DD}-1.25	V
V_{IN}	Comparator input voltage range	-	-0.25	-	V_{DD}+0.25	V
V_{offset}(2)	Comparator offset error	-	-	-	±20	mV
t_{START}	Startup time (after BIAS_EN)	-	-	-	3(1)	µs
$I_{DD(COMP)}$	Analog comparator consumption	-	-	-	25(1)	µA
	Analog comparator consumption during power-down	-	-	-	60(1)	nA
t_{propag}(2)	Comparator propagation delay	100-mV input step with 5-mV overdrive, input rise time = 1 ns	-	-	2(1)	µs

1. Data guaranteed by design, not tested in production.
2. The comparator accuracy depends on the environment. In particular, the following cases may reduce the accuracy of the comparator and must be avoided:
   - Negative injection current on the I/Os close to the comparator inputs
   - Switching on I/Os close to the comparator inputs
   - Negative injection current on not used comparator input.
   - Switching with a high dV/dt on not used comparator input.

   These phenomena are even more critical when a big external serial resistor is added on the inputs.

9.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. Refer to application note *Software techniques for improving microcontrollers EMC performance* (AN1015).

Table 34. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	LQFP32, V_{DD} = 3.3 V	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	LQFP32, V_{DD} = 3.3 V, f_{HSI}	3B
		LQFP32, V_{DD} = 3.3 V, $f_{HSI}/2$	4A

Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 37. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 40*.

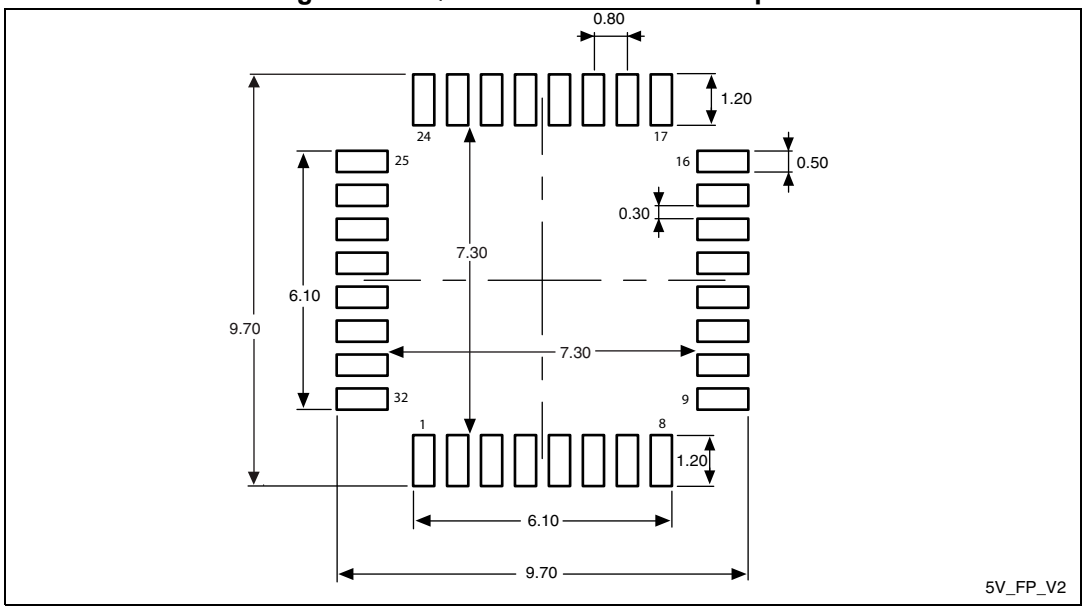
The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Figure 41. LQFP32 recommended footprint

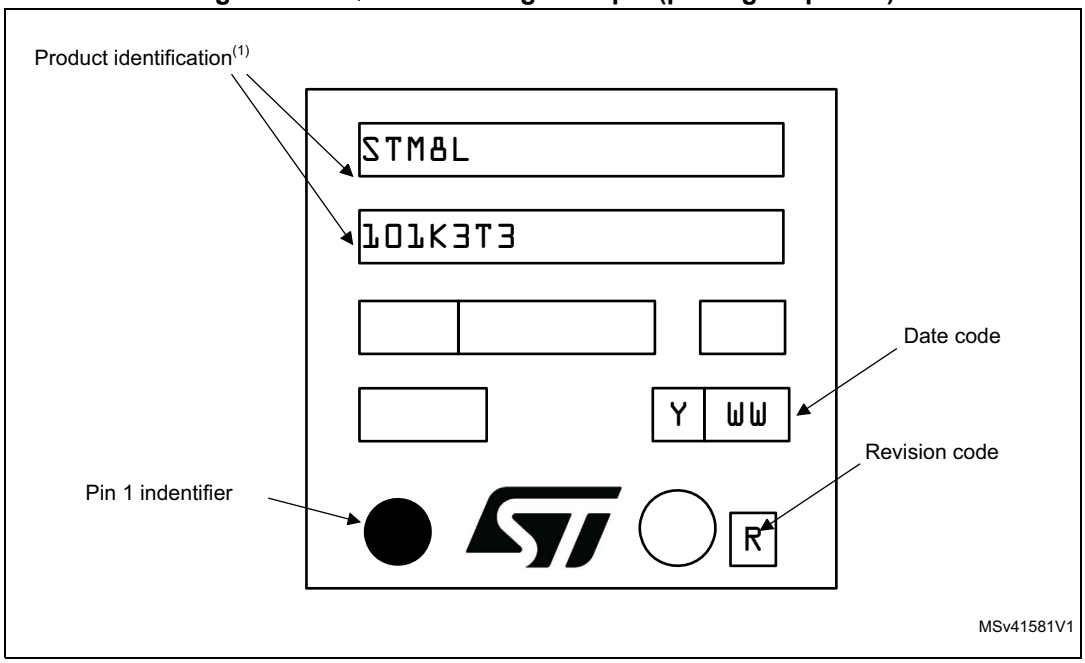


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

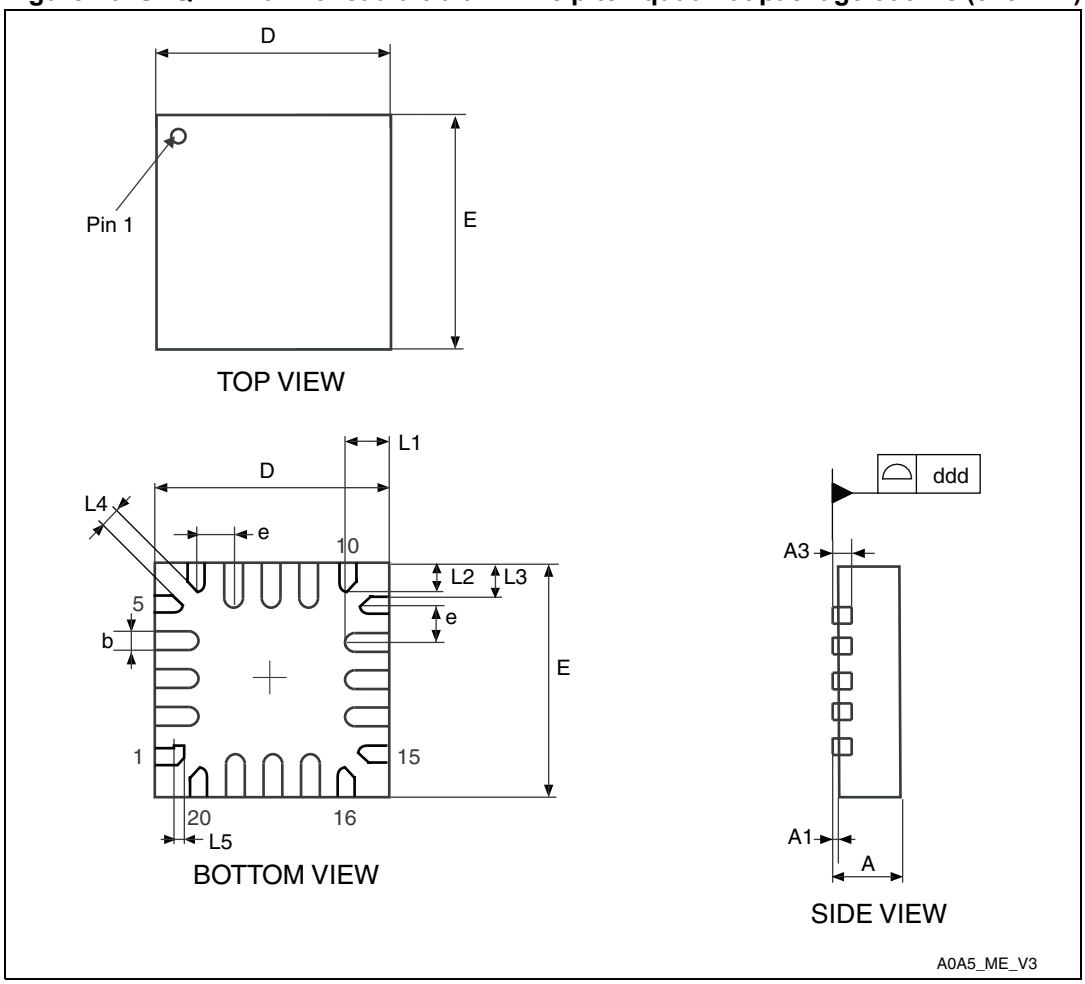
Figure 42. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.4 UFQFPN20 package information

Figure 46. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3 mm)



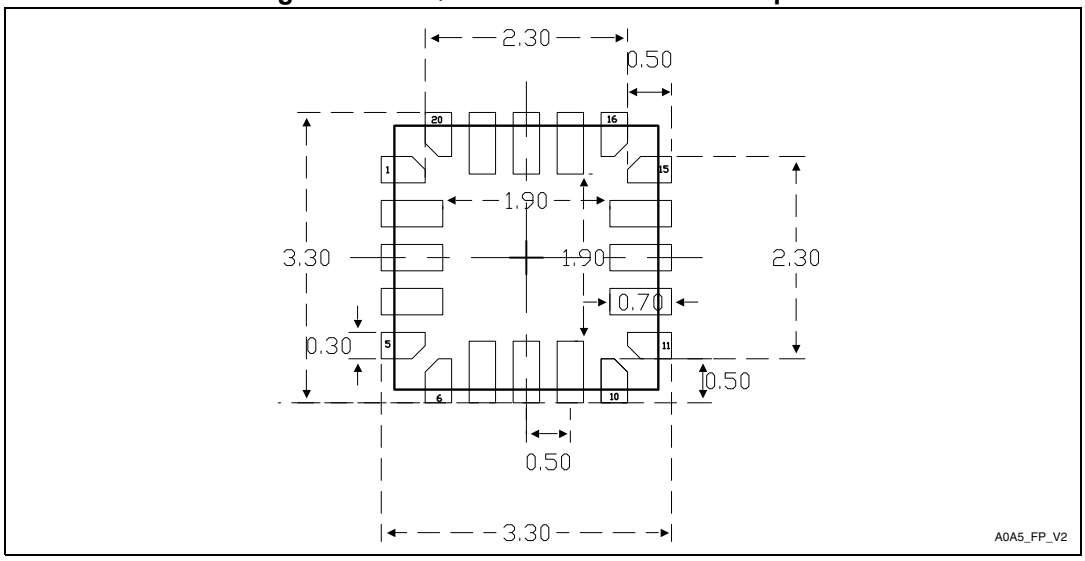
1. Drawing is not to scale.

Table 42. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd	-	0.050	-	-	0.0020	-

1. Values in inches are rounded to 4 decimal digits

Figure 47. UFQFPN20 recommended footprint

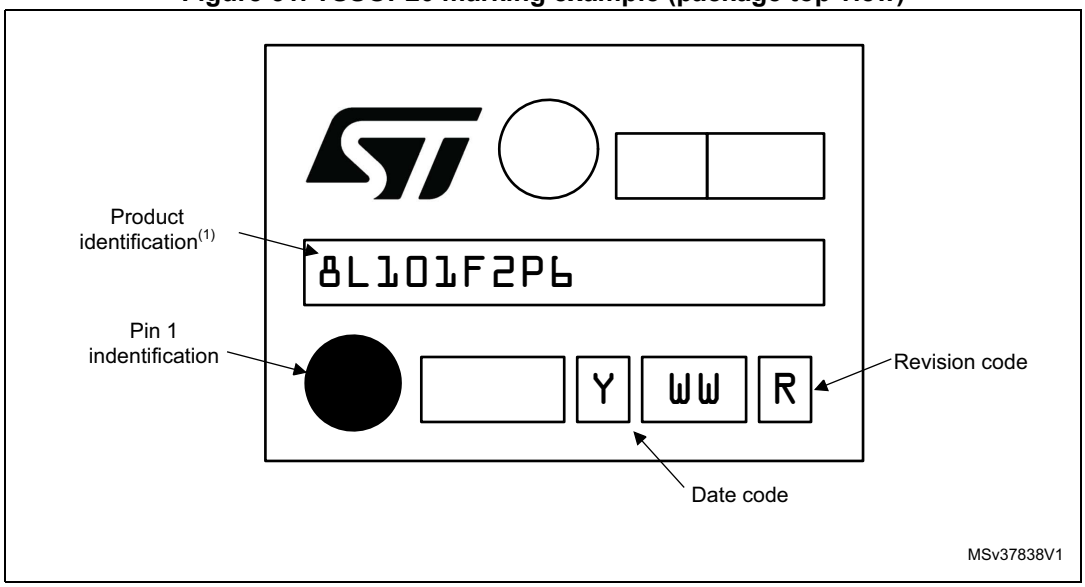


1. Dimensions are in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 51. TSSOP20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows the user to assemble and link their application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user's application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.