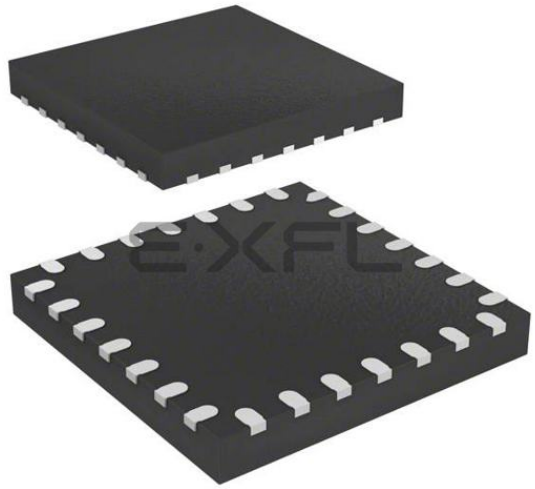

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101g2u6

1 Introduction

This datasheet provides the STM8L101x1 STM8L101x2 STM8L101x3 pinout, ordering information, mechanical and electrical device characteristics.

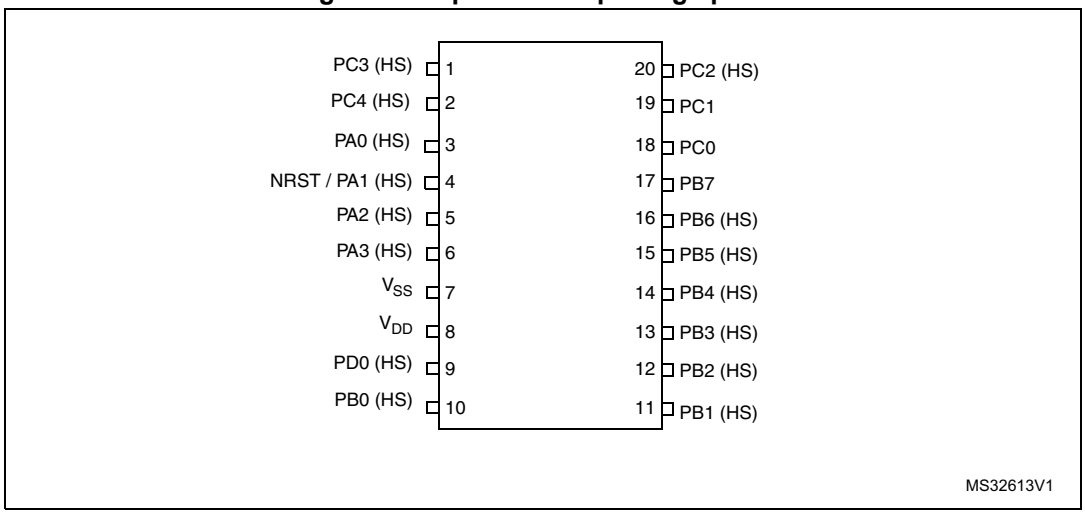
For complete information on the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller memory, registers and peripherals, please refer to the STM8L reference manual.

The STM8L101x1 STM8L101x2 STM8L101x3devices are members of the STM8L low-power 8-bit family. They are
referred to as low-density devices in the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller family reference manual (RM0013) and in the STM8L Flash programming manual (PM0054).

All devices of the SM8L product line provide the following benefits:

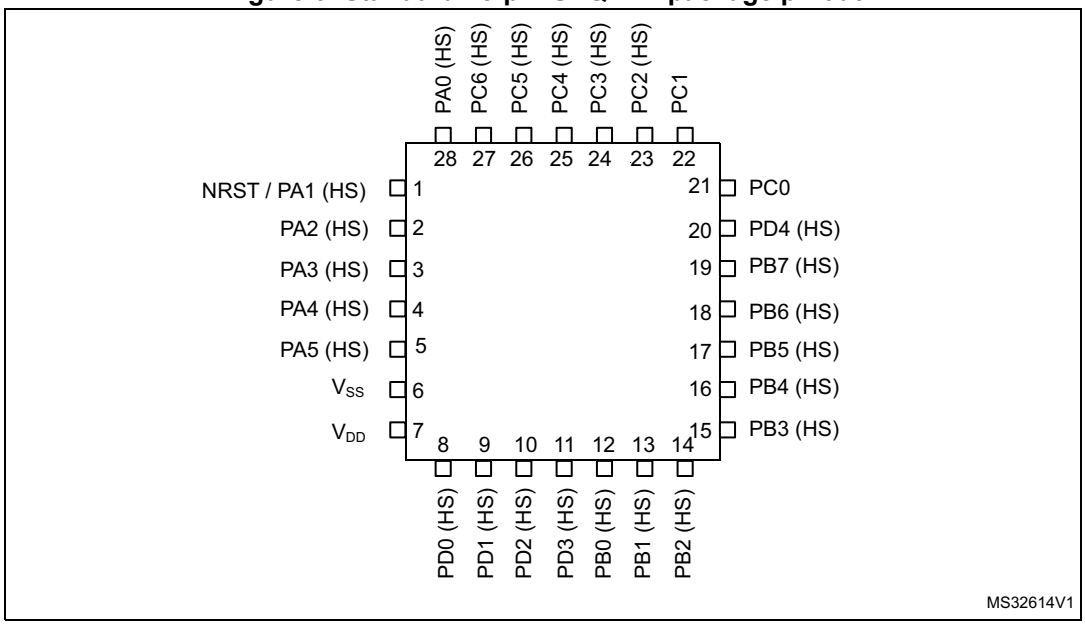
- Reduced system cost
  - Up to 8 Kbytes of low-density embedded Flash program memory including up to 2 Kbytes of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs.
  - Smaller battery and cheaper power supplies.
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MH, 0.8 µA in Active-halt mode, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Product family operating from 1.65 V to 3.6 V supply.

Figure 4. 20-pin TSSOP package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

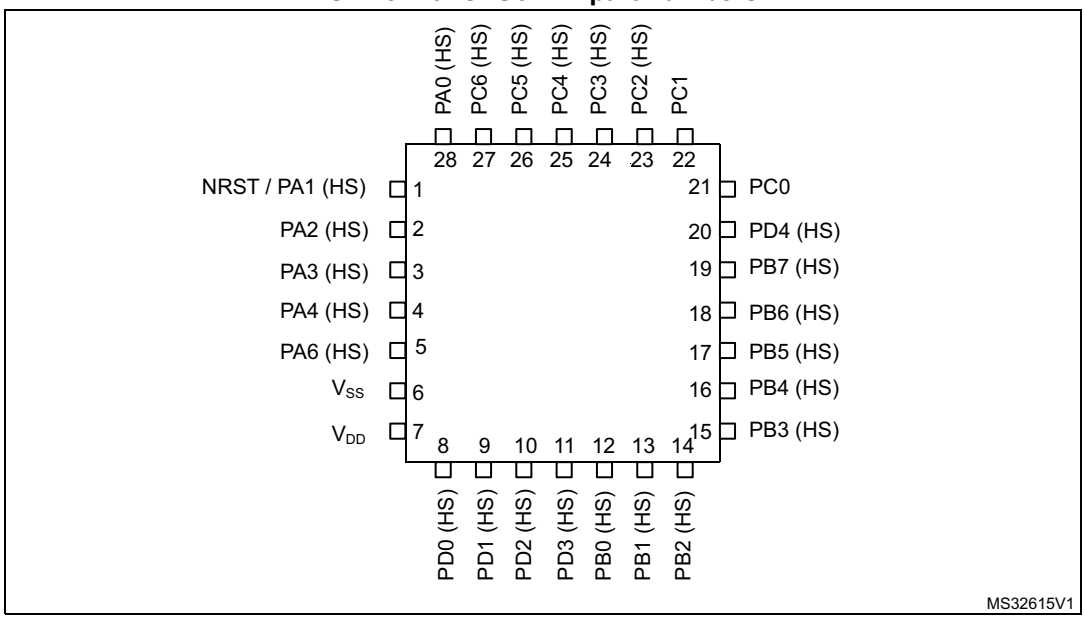
Figure 5. Standard 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 28-pin UFQFPN package. It is available on Port A6 in the Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers.

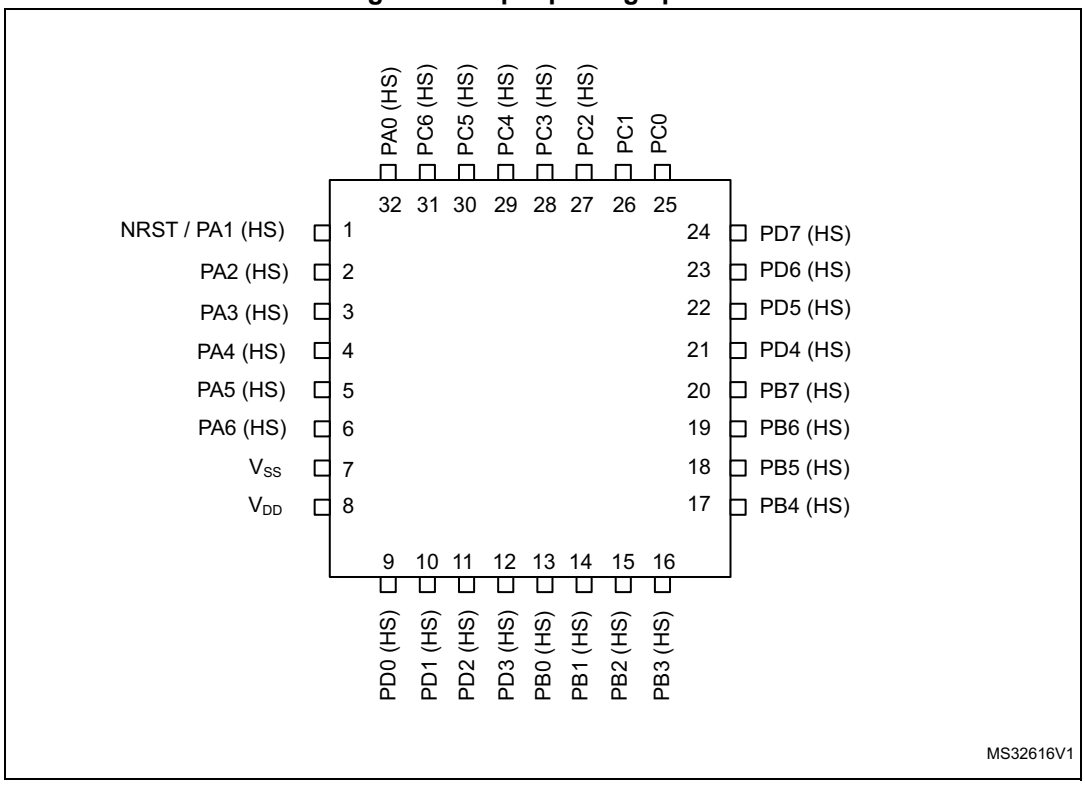
Figure 6. 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Warning: For the STM8L101G3U6ATR and STM8L101G2U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	26	26	30	PC5	I/O	**X**	X	X	HS	X	X	**Port C5**	-
-	-	-	27	27	31	PC6	I/O	**X**	X	X	HS	X	X	**Port C6**	-
20	20	3	28	28	32	PA0(5)/SWIM/ BEEP/IR_TIM (6)	I/O	X	**X**(5)	X	HS(6)	X	X	**Port A0**	SWIM input and output /Beep output/Timer Infrared output

1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1.5 Kbytes	0x00 0000	0x00 05FF
Flash program memory	2 Kbytes	0x00 8000	0x00 87FF
	4 Kbytes	0x00 8000	0x00 8FFF
	8 Kbytes	0x00 8000	0x00 9FFF

Note: 2 Kbytes of Data EEPROM is only available on devices with 8 Kbytes flash program memory.

Table 6. I/O Port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xxx
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xxx
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xxx
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xxx
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5250	TIM2	TIM2_CR1	TIM2 control register 1	0x00
0x00 5251		TIM2_CR2	TIM2 control register 2	0x00
0x00 5252		TIM2_SMCR	TIM2 slave mode control register	0x00
0x00 5253		TIM2_ETR	TIM2 external trigger register	0x00
0x00 5254		TIM2_IER	TIM2 interrupt enable register	0x00
0x00 5255		TIM2_SR1	TIM2 status register 1	0x00
0x00 5256		TIM2_SR2	TIM2 status register 2	0x00
0x00 5257		TIM2_EGR	TIM2 event generation register	0x00
0x00 5258		TIM2_CCMR1	TIM2 capture/compare mode register 1	0x00
0x00 5259		TIM2_CCMR2	TIM2 capture/compare mode register 2	0x00
0x00 525A		TIM2_CCER1	TIM2 capture/compare enable register 1	0x00
0x00 525B		TIM2_CNTRH	TIM2 counter high	0x00
0x00 525C		TIM2_CNTRL	TIM2 counter low	0x00
0x00 525D		TIM2_PSCR	TIM2 prescaler register	0x00
0x00 525E		TIM2_ARRH	TIM2 auto-reload register high	0xFF
0x00 525F		TIM2_ARRL	TIM2 auto-reload register low	0xFF
0x00 5260		TIM2_CCR1H	TIM2 capture/compare register 1 high	0x00
0x00 5261		TIM2_CCR1L	TIM2 capture/compare register 1 low	0x00
0x00 5262		TIM2_CCR2H	TIM2 capture/compare register 2 high	0x00
0x00 5263		TIM2_CCR2L	TIM2 capture/compare register 2 low	0x00
0x00 5264		TIM2_BKR	TIM2 break register	0x00
0x00 5265		TIM2_OISR	TIM2 output idle state register	0x00
0x00 5266 to 0x00 527F	Reserved area (26 bytes)			

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated row of the memory.

All option bytes can be modified only in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

Refer to the STM8L Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 10. Option bytes

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT1	ROP[7:0]								0x00
0x4807	-	-	Must be programmed to 0x00								0x00
0x4802	UBC (User Boot code size)	OPT2	UBC[7:0]								0x00
0x4803	DATASIZE	OPT3	DATASIZE[7:0]								0x00
0x4808	Independent watchdog option	OPT4 [1:0]	Reserved						IWDG _HALT	IWDG _HW	0x00

Table 11. Option byte description

OPT1	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) Refer to *Read-out protection* section in the STM8L reference manual (RM0013) for details.
OPT2	**UBC[7:0]** *Size of the user boot code area* 0x00: no UBC 0x01-0x02: UBC contains only the interrupt vectors. 0x03: Page 0 and 1 reserved for the interrupt vectors. Page 2 is available to store user boot code. Memory is write protected ... 0x7F - Page 0 to 126 reserved for UBC, memory is write protected Refer to *User boot area (UBC)* section in the STM8L reference manual (RM0013) for more details. UBC[7] is forced to 0 internally by HW.

8 Unique ID

STM8L101xx devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory
- To activate secure boot processes.

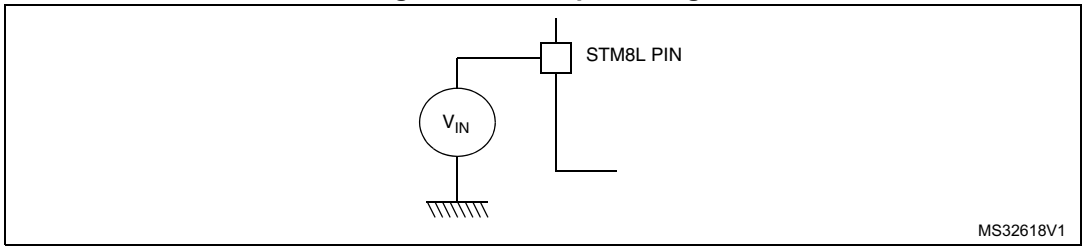
Table 12. Unique ID registers (96 bits)

Address	Content description	Unique ID bits							
		7	6	5	4	3	2	1	0
0x4925	X co-ordinate on the wafer	U_ID[7:0]							
0x4926		U_ID[15:8]							
0x4927	Y co-ordinate on the wafer	U_ID[23:16]							
0x4928		U_ID[31:24]							
0x4929	Wafer number	U_ID[39:32]							
0x492A	Lot number	U_ID[47:40]							
0x492B		U_ID[55:48]							
0x492C		U_ID[63:56]							
0x492D		U_ID[71:64]							
0x492E		U_ID[79:72]							
0x492F		U_ID[87:80]							
0x4930		U_ID[95:88]							

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on true open drain pins (PC0 and PC1)(1)	V_{SS}-0.3	V_{DD} + 4.0	
	Input voltage on any other pin (2)	V_{SS}-0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		-

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

Table 18. Total current consumption in Run mode (1)

Symbol	Parameter	Conditions(2)		Typ	Max(3)	Unit
$I_{DD\ (Run)}$	Supply current in Run mode(4) (5)	Code executed from RAM	f_{MASTER} = 2 MHz	0.39	0.60	mA
			f_{MASTER} = 4 MHz	0.55	0.70	
			f_{MASTER} = 8 MHz	0.90	1.20	
			f_{MASTER} = 16 MHz	1.60	2.10(6)	
		Code executed from Flash	f_{MASTER} = 2 MHz	0.55	0.70	
			f_{MASTER} = 4 MHz	0.88	1.80	
			f_{MASTER} = 8 MHz	1.50	2.50	
			f_{MASTER} = 16 MHz	2.70	3.50	

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{MASTER}$
3. Maximum values are given for T_A = –40 to 125 °C.
4. CPU executing typical data processing.
5. An approximate value of $I_{DD(Run)}$ can be given by the following formula: $I_{DD(Run)} = f_{MASTER}$ x 150 µA/MHz +215 µA.
6. Tested in production.

Figure 11. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 2 MHz

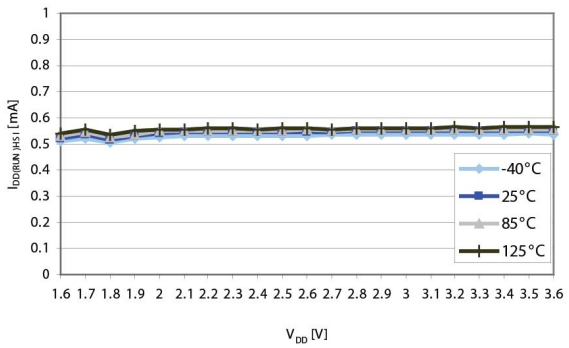
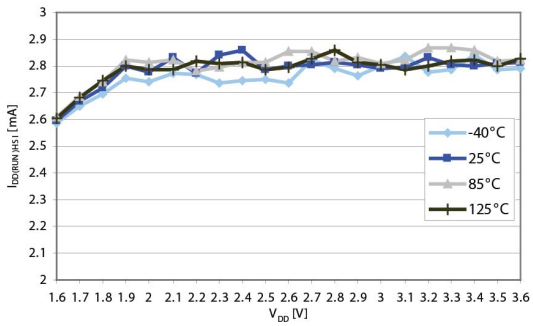


Figure 12. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Figure 33. SPI timing diagram - slave mode and CPHA = 0

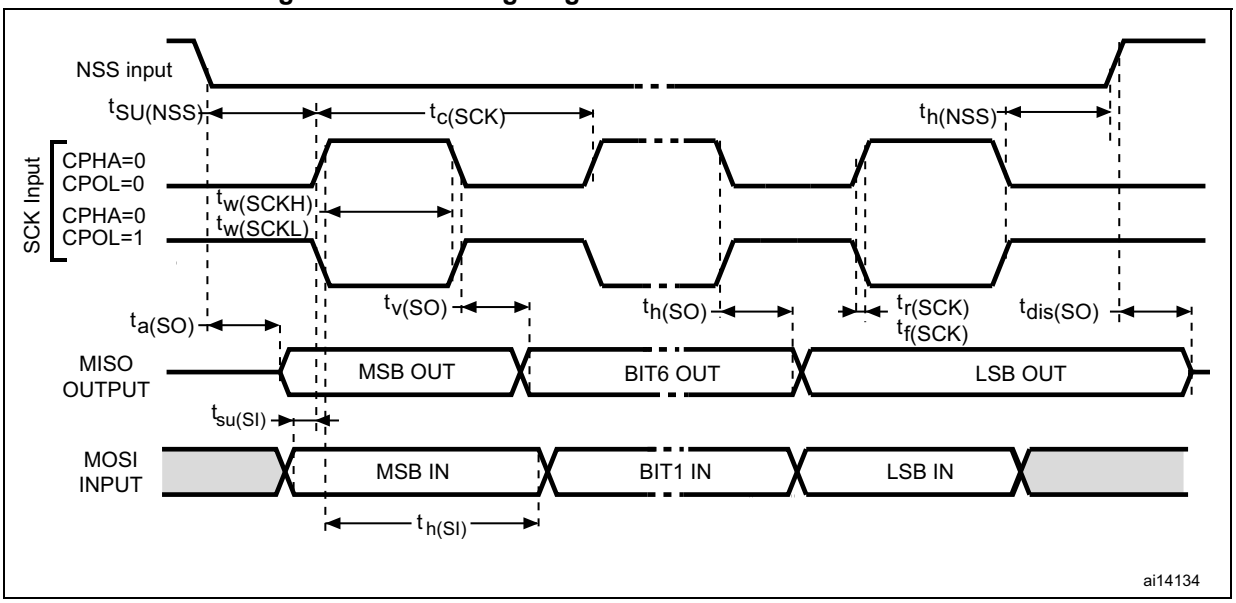
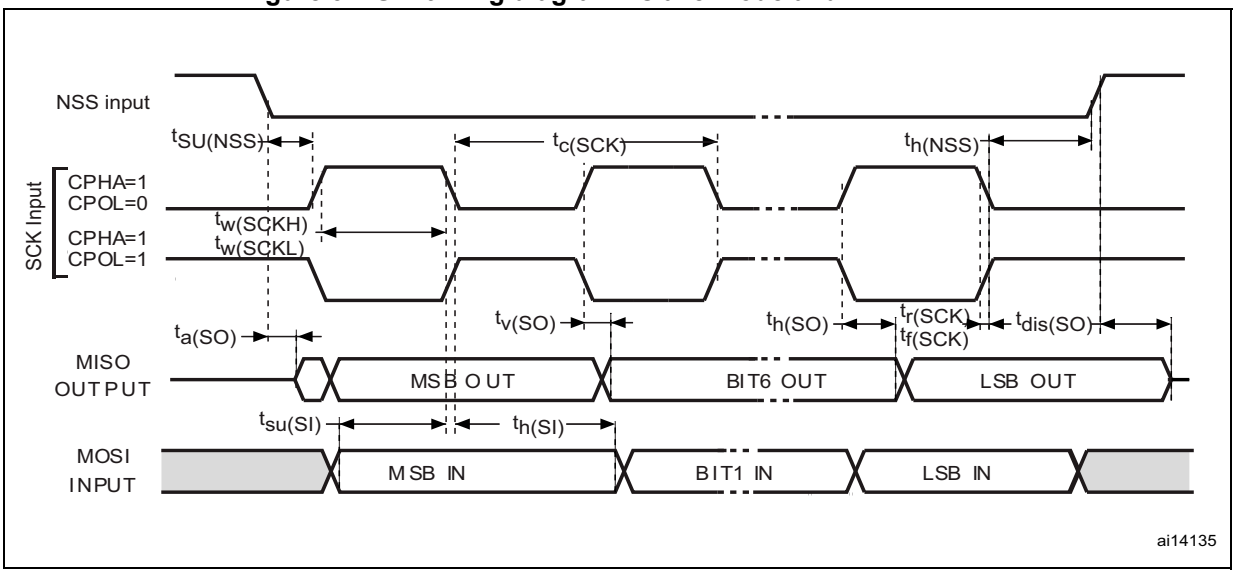


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Inter IC control interface (I2C)

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

The STM8L I^2C interface meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 32. I2C characteristics

Symbol	Parameter	Standard mode I2C		Fast mode I2C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0 (3)	-	0 (4)	900 (3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SCK} must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance
For other speed ranges, achieved speed can have ±2% tolerance
The above variations depend on the accuracy of the external components used.

Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 35. EMI data (1)

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. 16 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = +25 °C, LQFP32 conforming to IEC61967-2	0.1 MHz to 30 MHz	-3	dBµV
			30 MHz to 130 MHz	-6	
			130 MHz to 1 GHz	-5	
			SAE EMI Level	1	-

1. Not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin).

This test conforms to the JESD22-A114A/A115A standard.

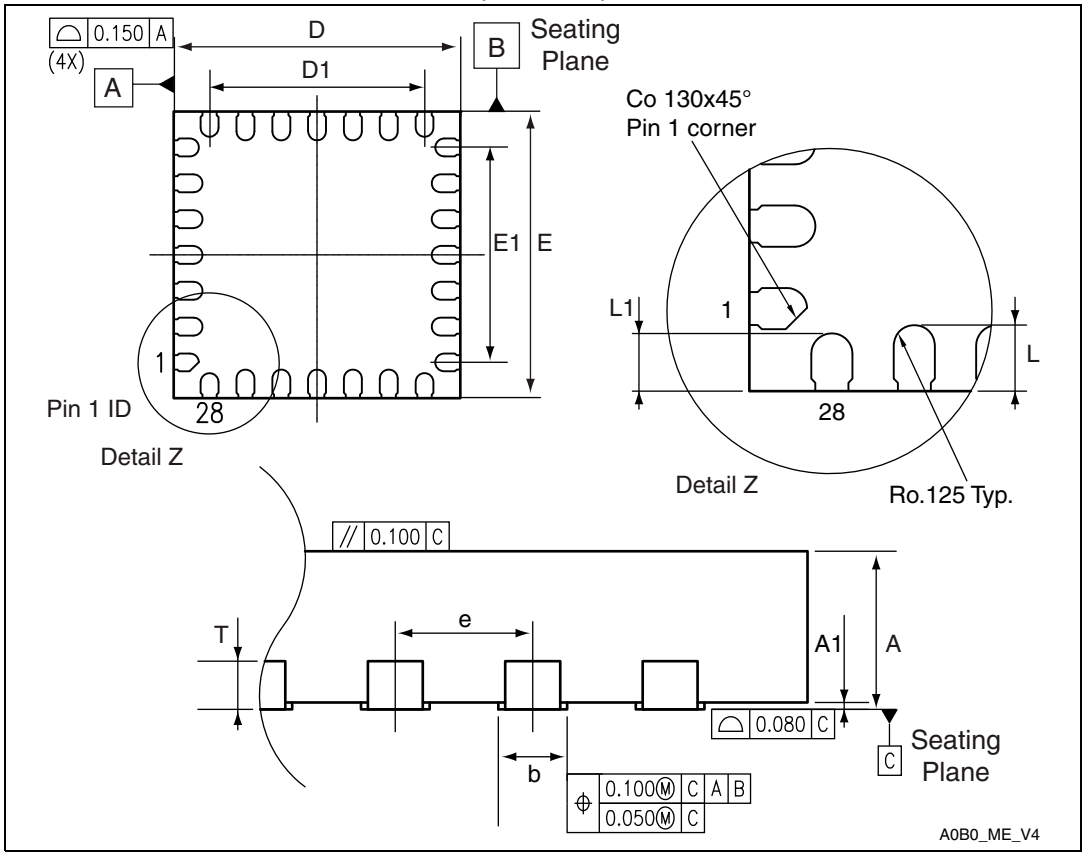
Table 36. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value (1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)		500	

1. Data based on characterization results, not tested in production.

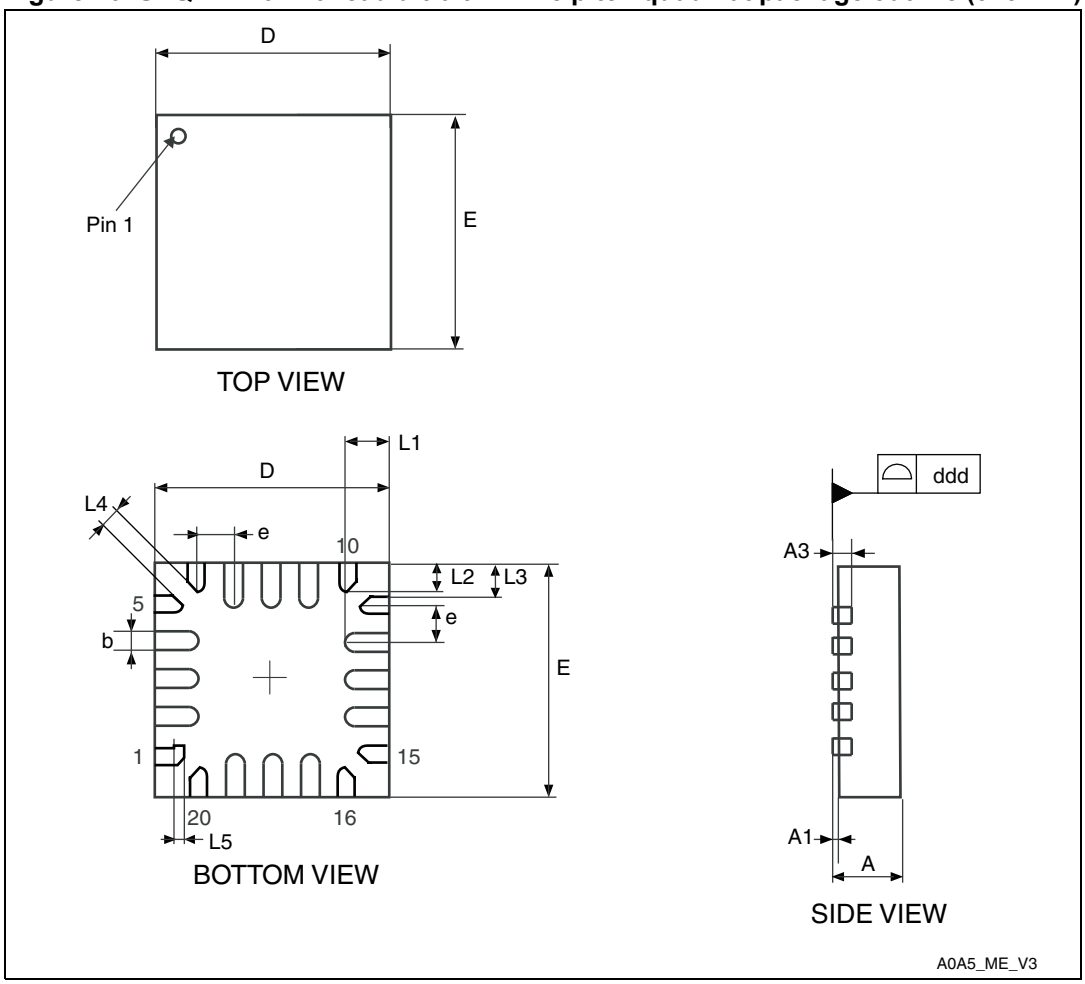
10.3 UFQFPN28 package information

Figure 43. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4 mm)



10.4 UFQFPN20 package information

Figure 46. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package outline (3x3 mm)



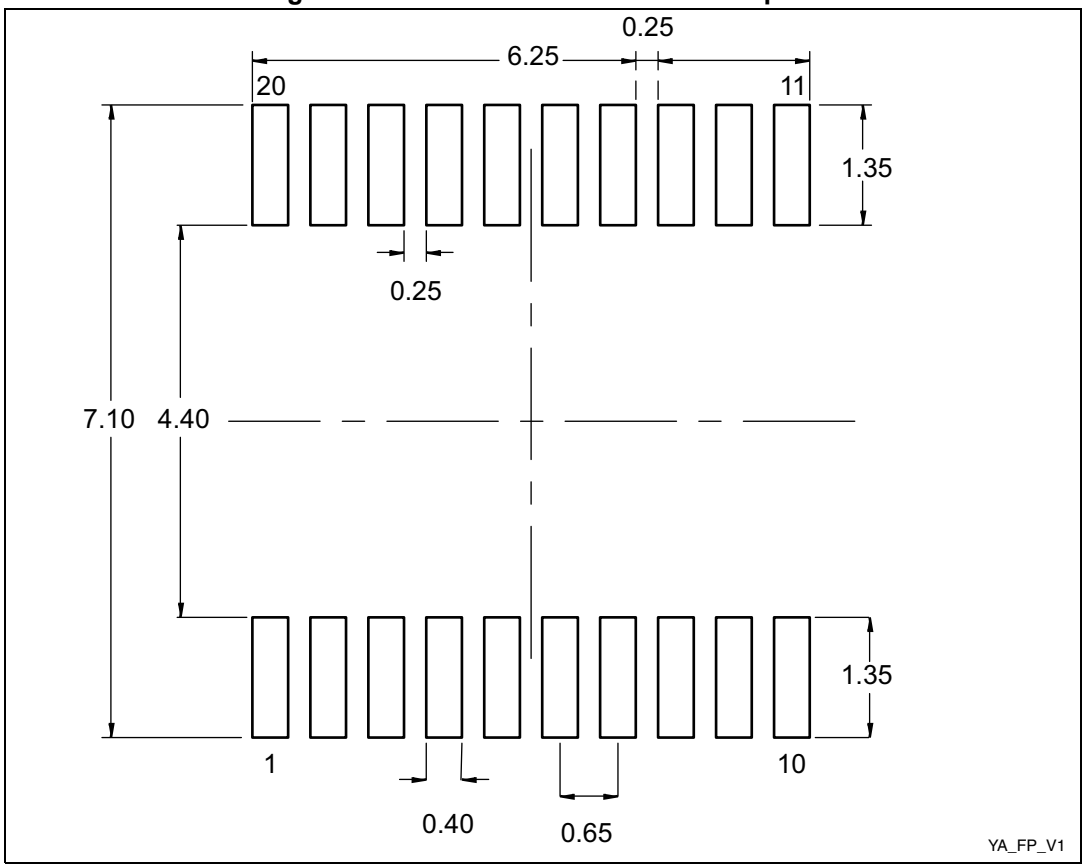
1. Drawing is not to scale.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data (continued)

Dim.	mm				inches[1]	
	Min	Typ	Max	Min	Typ	Max
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039
Number of pins	20					

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 50. TSSOP20 recommended footprint



1. Dimensions are in millimeters.

Table 44. Document revision history (continued)

Date	Revision	Changes
14-Oct-2010	11	Added STM8L101F1 devices: Modified *Table 1: Device summary on page 1*, *Table 2: STM8L101xx device feature summary on page 9* and *Table 5: Flash and RAM boundary addresses on page 24* Modified warning below *Figure 3 on page 16* and below*Table 4: STM8L101xx pin description on page 20* Modified *Figure 52: STM8L101xx ordering information scheme on page 79* Modified text above *Figure 32: Recommended NRST pin configuration on page 54* Modified *Figure 32 on page 54*
02-Aug-2013	12	Added “The RAM content is preserved” in halt mode *Section 3.6: Low power modes* Reformatted *Figure 2: Standard 20-pin UFQFPN package pinout*, *Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 5: Standard 28-pin UFQFPN package pinout*, *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers* and *Figure 7: 32-pin package pinout* Corrected NRST/PA1 pin OD output capability in *Table 4: STM8L101xx pin description* and corrected note *2.* and *4.* Added note “Slope control of all GPIO can be programmed except...” in *Table 4: STM8L101xx pin description* Added note under *Table 5: Flash and RAM boundary addresses* Replaced UM0320 with UM0470 in *Section 7: Option bytes* Updated OPT2 and OPT3 in *Table 10: Option bytes* Added additional note *2.* references in *Table 22: HSI oscillator characteristics* Added note *2.* under *Table 17: Operating conditions at power-up / power-down* and under *Figure 32: Recommended NRST pin configuration* Corrected ‘SCK output’ in *Figure 35: SPI timing diagram - master mode(1)* Added top view in *Figure 43: UFQFPN20 3 x 3 mm 0.6 mm package outline* Repositioned the package layout and footprint for all packages. Replaced “Standard ports” with “High sink ports” Replaced “TIMx_TRIG” with “TIMx_ETR” Replaced all ‘"Data guaranteed, each individual device tested in production” notes with “Tested in production”
31-Mar-2014	13	Updated L3 value on *Table 42*, added note 2) and 3) on *Table 43*