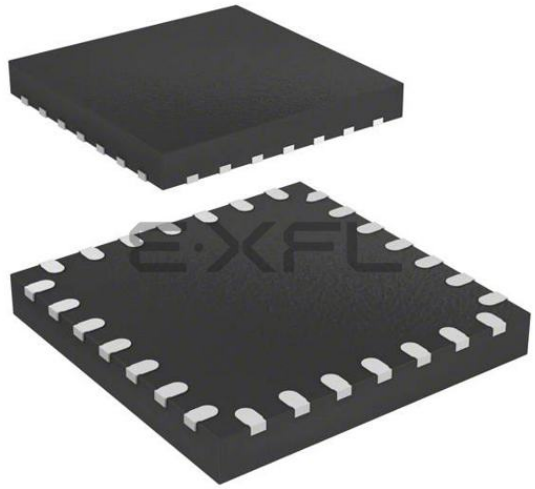

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101g2u6a

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3.10 Auto-wakeup counter

The auto-wakeup (AWU) counter is used to wakeup the device from Active-halt mode.

3.11 General purpose and basic timers

STM8L101xx devices contain two 16-bit general purpose timers (TIM2 and TIM3) and one 8-bit basic timer (TIM4).

16-bit general purpose timers

The 16-bit timers consist of 16-bit up/down auto-reload counters driven by a programmable prescaler. They perform a wide range of functions, including:

- Time base generation
- Measuring the pulse lengths of input signals (input capture)
- Generating output waveforms (output compare, PWM and One pulse mode)
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

8-bit basic timer

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow.

3.12 Beeper

The STM8L101xx devices include a beeper function used to generate a beep signal in the range of 1, 2 or 4 kHz when the LSI clock is operating at a frequency of 38 kHz.

3.13 Infrared (IR) interface

The STM8L101xx devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

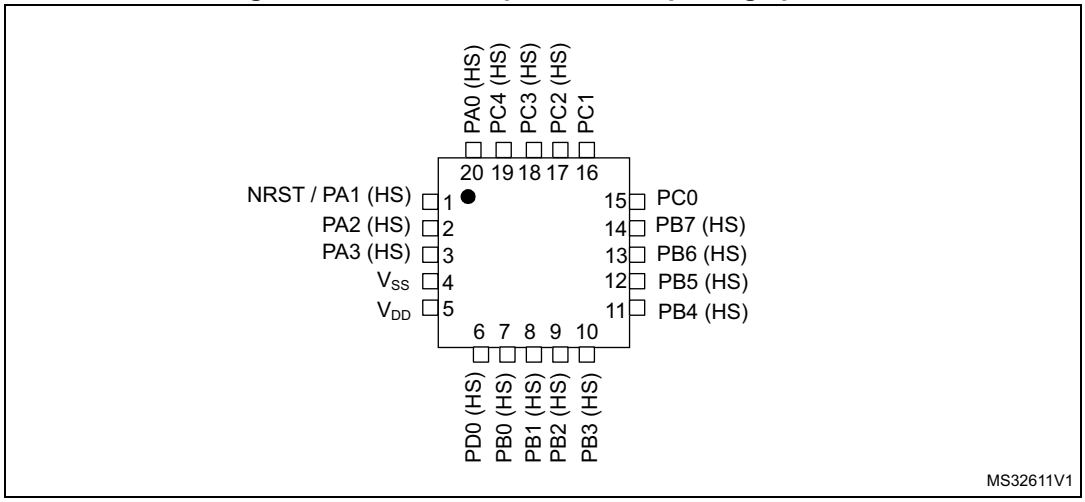
3.14 Comparators

The STM8L101xx features two zero-crossing comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal (comparison with ground) or external (comparison to a reference pin voltage).

Each comparator is connected to 4 channels, which can be used to generate interrupt, timer input capture or timer break. Their polarity can be inverted.

4 Pin description

Figure 2. Standard 20-pin UFQFPN package pinout

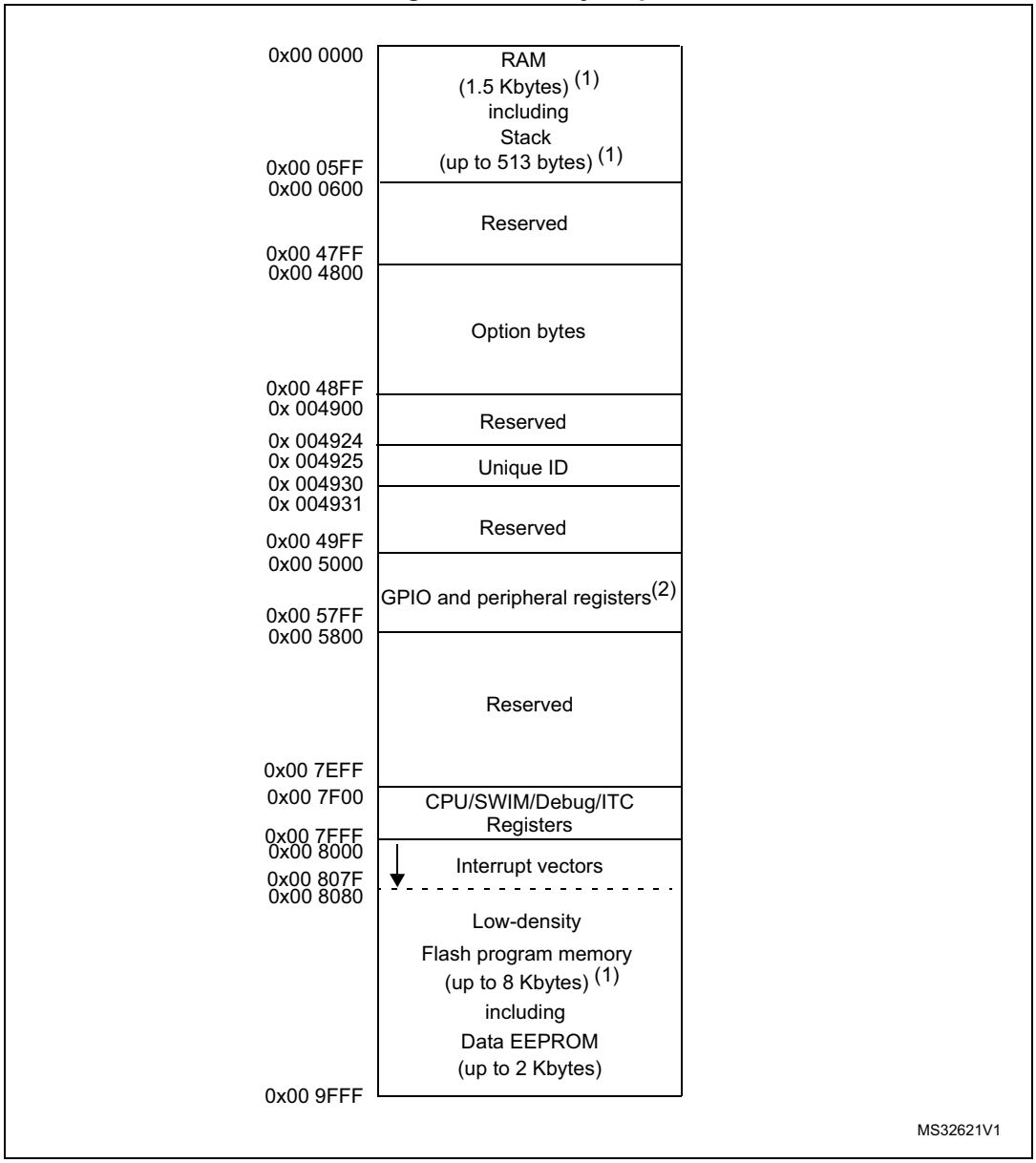


1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 20-pin UFQFPN package. It is available on Port A6 in the Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers.

5 Memory and register map

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR	AWU control/status register	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 51FF	Reserved area (268 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205 to 0x00 520F	Reserved area (11 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02

Table 8. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
0x00 7F78 to 0x00 7F79	Reserved area (2 bytes)			
0x00 7F80	SWIM	SWIM_CSR	SWIM control status register	0x00
0x00 7F81 to 0x00 7F8F	Reserved area (15 bytes)			
0x00 7F90	DM	DM_BK1RE	Breakpoint 1 register extended byte	0xFF
0x00 7F91		DM_BK1RH	Breakpoint 1 register high byte	0xFF
0x00 7F92		DM_BK1RL	Breakpoint 1 register low byte	0xFF
0x00 7F93		DM_BK2RE	Breakpoint 2 register extended byte	0xFF
0x00 7F94		DM_BK2RH	Breakpoint 2 register high byte	0xFF
0x00 7F95		DM_BK2RL	Breakpoint 2 register low byte	0xFF
0x00 7F96		DM_CR1	Debug module control register 1	0x00
0x00 7F97		DM_CR2	Debug module control register 2	0x00
0x00 7F98		DM_CSR1	Debug module control/status register 1	0x10
0x00 7F99		DM_CSR2	Debug module control/status register 2	0x00
0x00 7F9A		DM_ENFCTR	Enable function register	0xFF

1. Refer to *Table 7: General hardware register map on page 25* (addresses 0x00 50A0 to 0x00 50A5) for a list of external interrupt registers.

7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated row of the memory.

All option bytes can be modified only in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 10* for details on option byte addresses.

Refer to the STM8L Flash programming manual (PM0054) and STM8 SWIM and Debug Manual (UM0470) for information on SWIM programming procedures.

Table 10. Option bytes

Addr.	Option name	Option byte No.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
0x4800	Read-out protection (ROP)	OPT1	ROP[7:0]								0x00
0x4807	-	-	Must be programmed to 0x00								0x00
0x4802	UBC (User Boot code size)	OPT2	UBC[7:0]								0x00
0x4803	DATASIZE	OPT3	DATASIZE[7:0]								0x00
0x4808	Independent watchdog option	OPT4 [1:0]	Reserved						IWDG _HALT	IWDG _HW	0x00

Table 11. Option byte description

OPT1	**ROP[7:0]** *Memory readout protection (ROP)* 0xAA: Enable readout protection (write access via SWIM protocol) Refer to *Read-out protection* section in the STM8L reference manual (RM0013) for details.
OPT2	**UBC[7:0]** *Size of the user boot code area* 0x00: no UBC 0x01-0x02: UBC contains only the interrupt vectors. 0x03: Page 0 and 1 reserved for the interrupt vectors. Page 2 is available to store user boot code. Memory is write protected ... 0x7F - Page 0 to 126 reserved for UBC, memory is write protected Refer to *User boot area (UBC)* section in the STM8L reference manual (RM0013) for more details. UBC[7] is forced to 0 internally by HW.

Table 11. Option byte description (continued)

OPT3	**DATASIZE[7:0]** Size of the data EEPROM area 0x00: no data EEPROM area (1) 0x01: 1 page reserved for data storage from 0x9FC0 to 0x9FFF(1) 0x02: 2 pages reserved for data storage from 0x9F80 to 0x9FFF(1) ... (1) 0x20: 32 pages reserved for data storage from 0x9800 to 0x9FFF(1) Refer to *Data EEPROM (DATA)* section in the STM8L reference manual (RM0013) for more details. DATASIZE[7:6] are forced to 0 internal by HW.
OPT4	**IWDG_HW:** *Independent watchdog* 0: Independent watchdog activated by software 1: Independent watchdog activated by hardware
	IWDG_HALT: *Independent window watchdog reset on Halt/Active-halt* 0: Independent watchdog continues running in Halt/Active-halt mode 1: Independent watchdog stopped in Halt/Active-halt mode

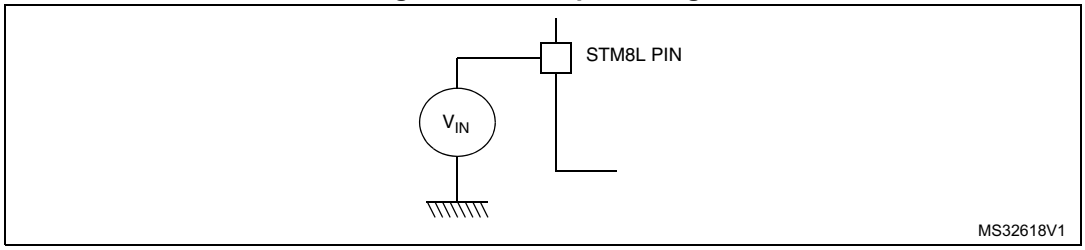
1. 0x00 is the only allowed value for 4 Kbyte STM8L101xx devices.

Caution: After a device reset, read access to the program memory is not guaranteed if address 0x4807 is not programmed to 0x00.

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on true open drain pins (PC0 and PC1)(1)	V_{SS}-0.3	V_{DD} + 4.0	
	Input voltage on any other pin (2)	V_{SS}-0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		-

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

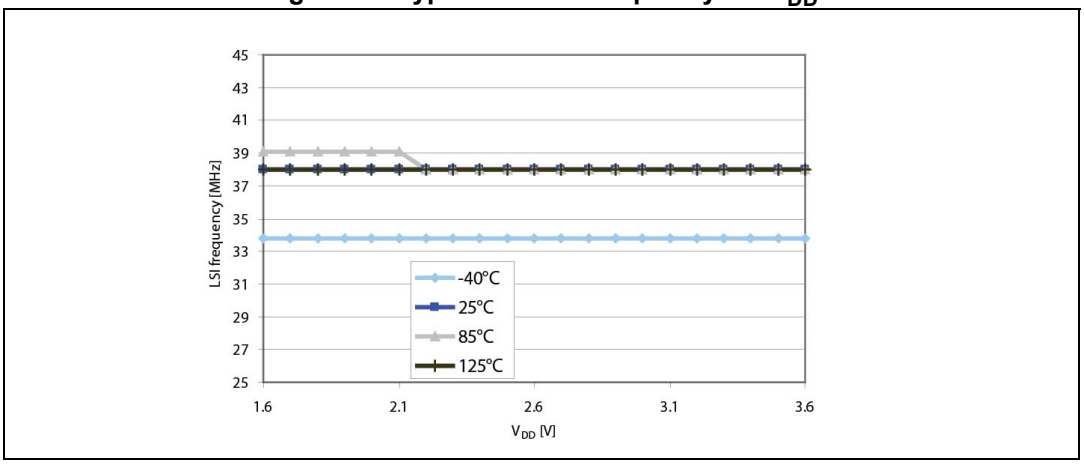
Low speed internal RC oscillator (LSI)

Table 23. LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$f_{drift(LSI)}$	LSI oscillator frequency drift(2)	0 °C ≤T_A ≤85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

Figure 19. Typical LSI RC frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 24. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.4	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 25. Flash program memory

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{MASTER} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1- or 64-byte (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1- to 64-byte (block) write cycles (on erased byte)	-	-	3	-	ms

Figure 33. SPI timing diagram - slave mode and CPHA = 0

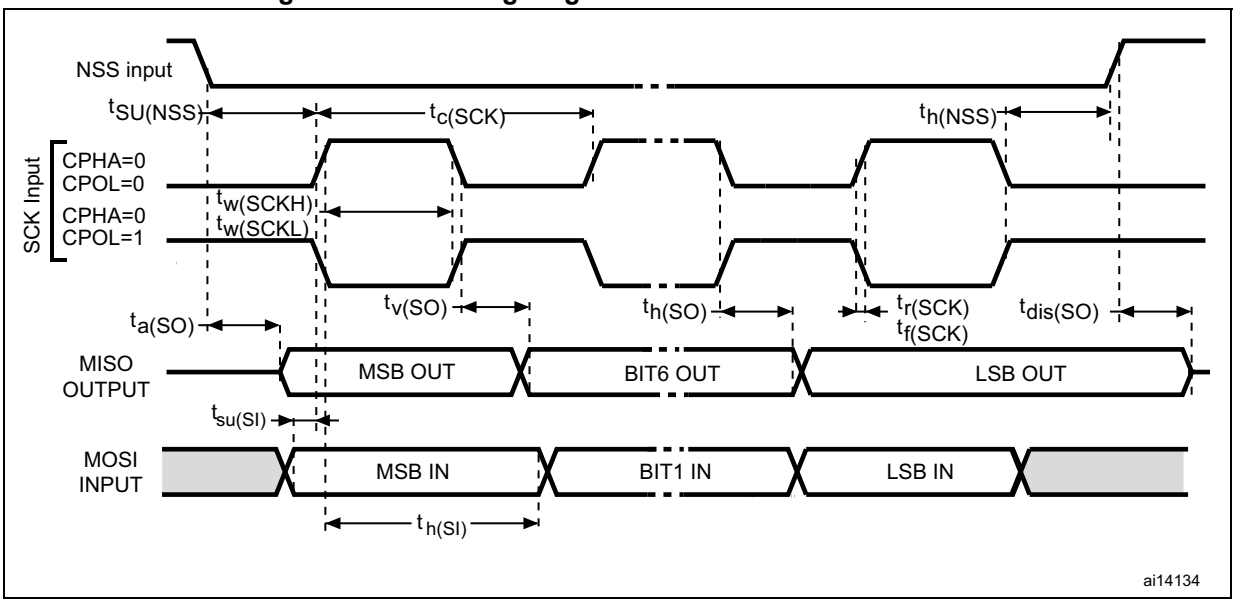
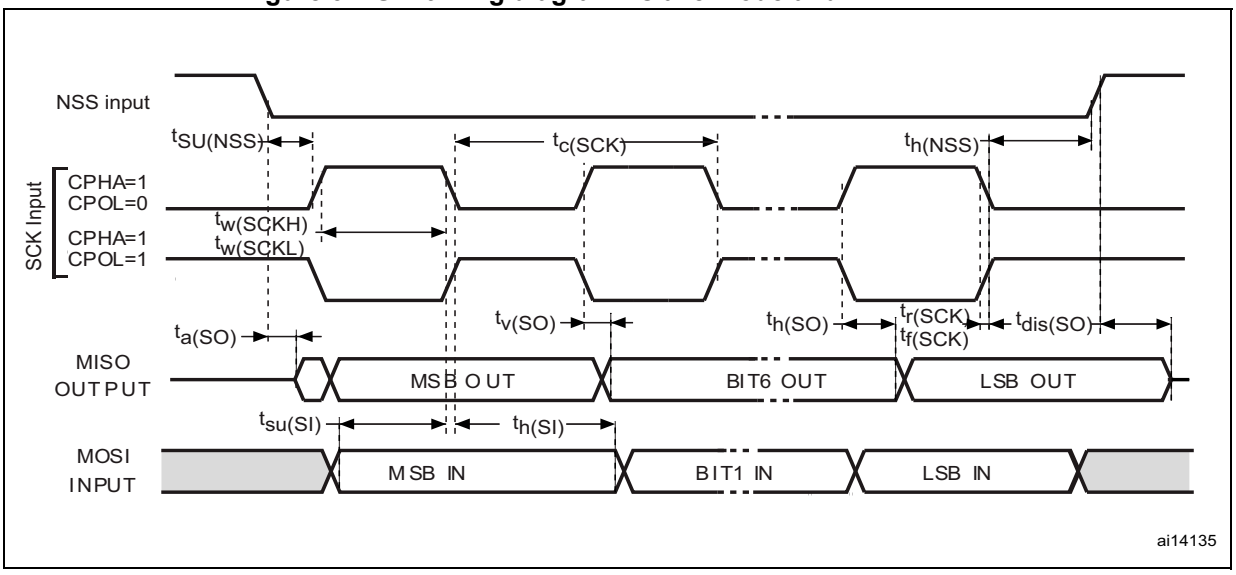


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



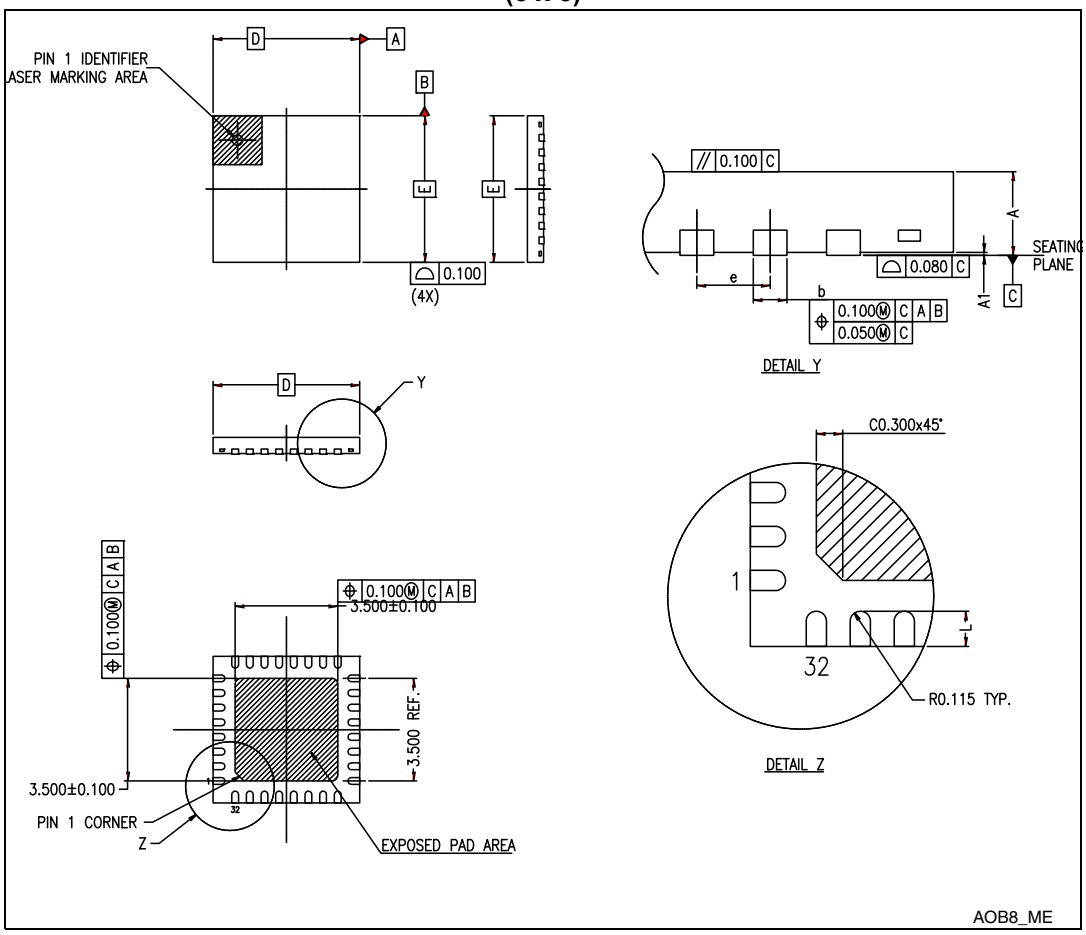
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 UFQFPN32 package information

Figure 37. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)

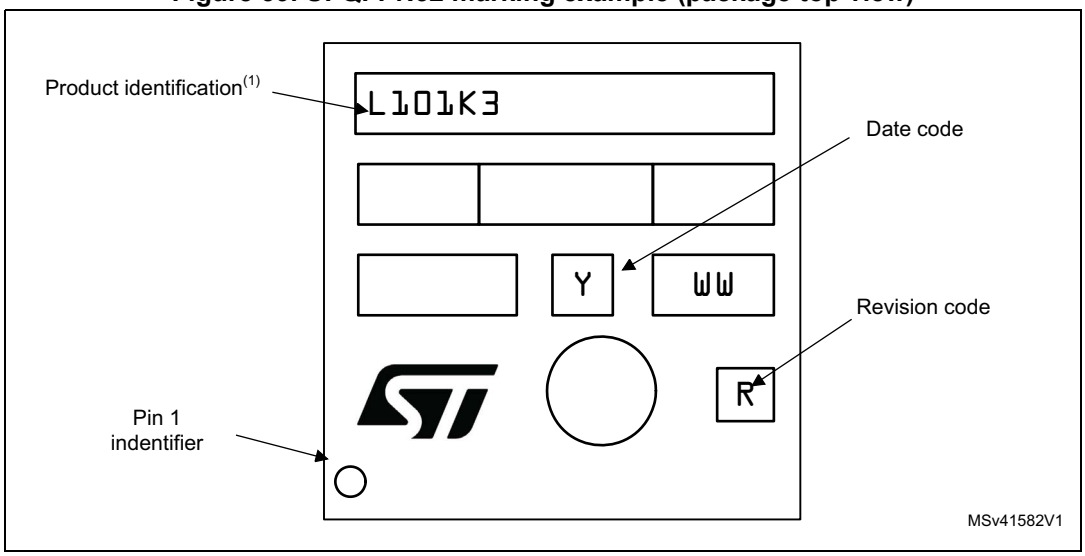


1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 39. UFQFPN32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.3 UFQFPN28 package information

Figure 43. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4 mm)

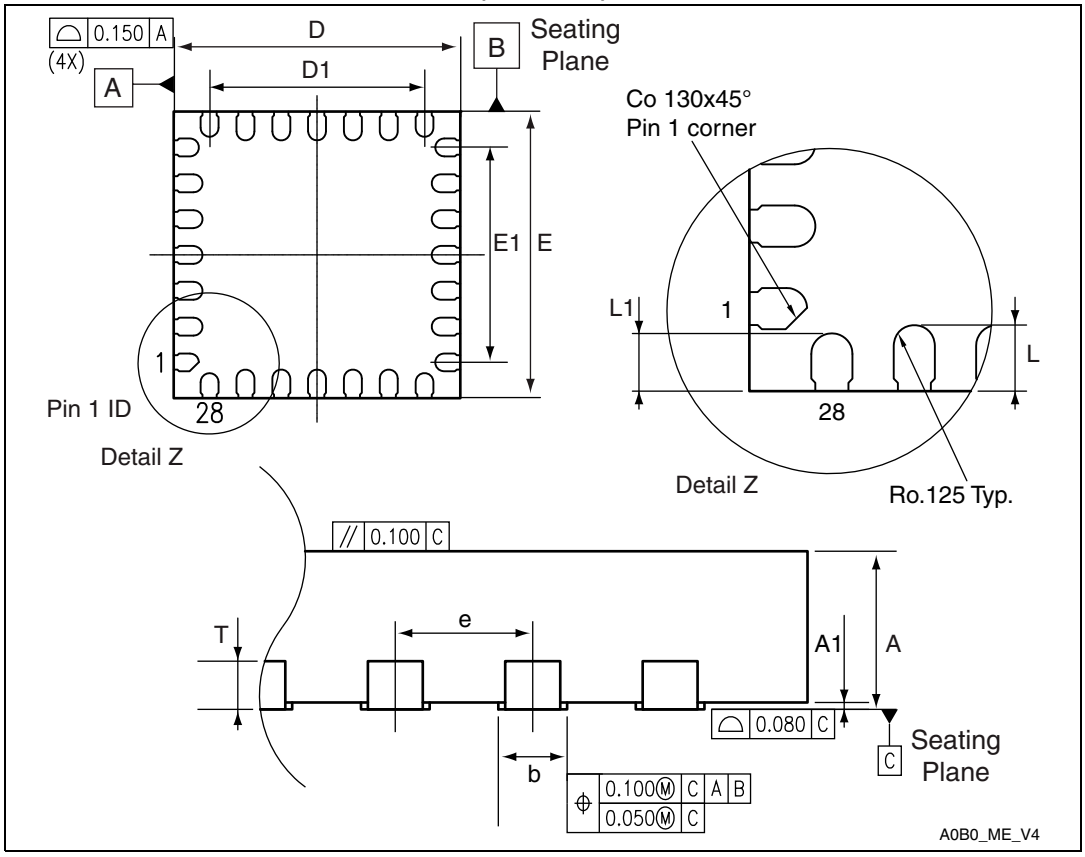
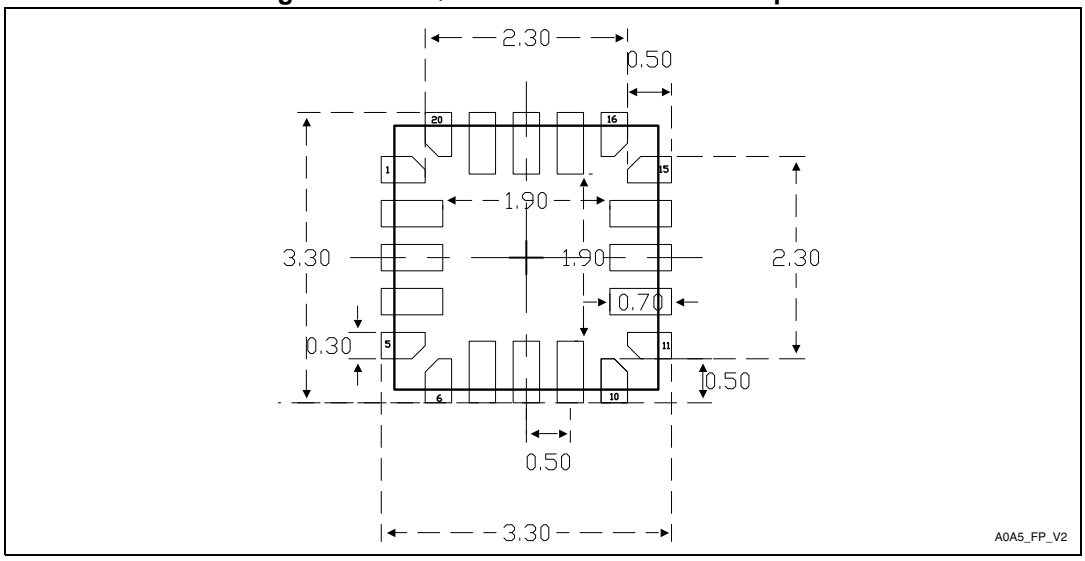


Table 42. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd	-	0.050	-	-	0.0020	-

1. Values in inches are rounded to 4 decimal digits

Figure 47. UFQFPN20 recommended footprint

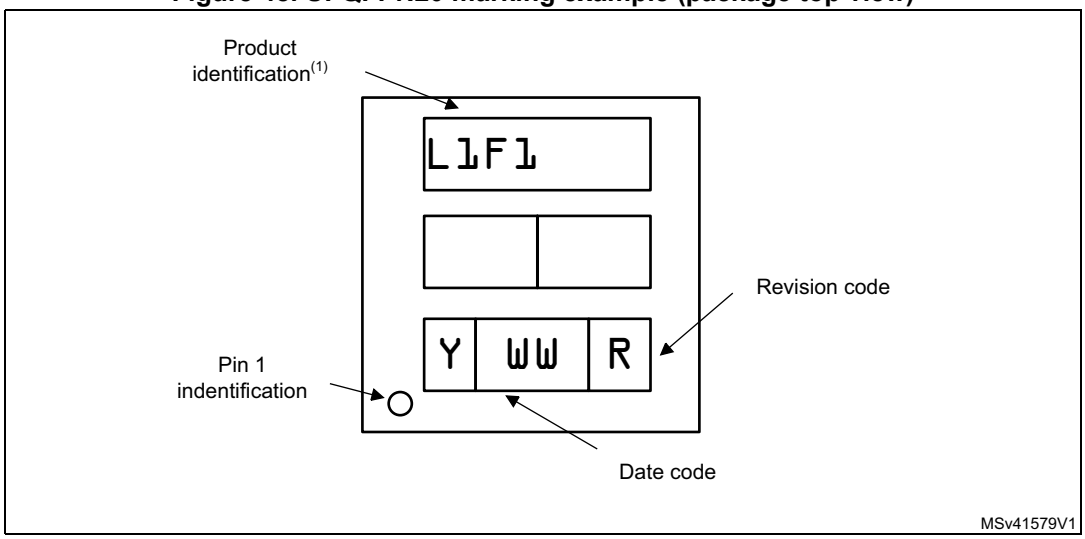


1. Dimensions are in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

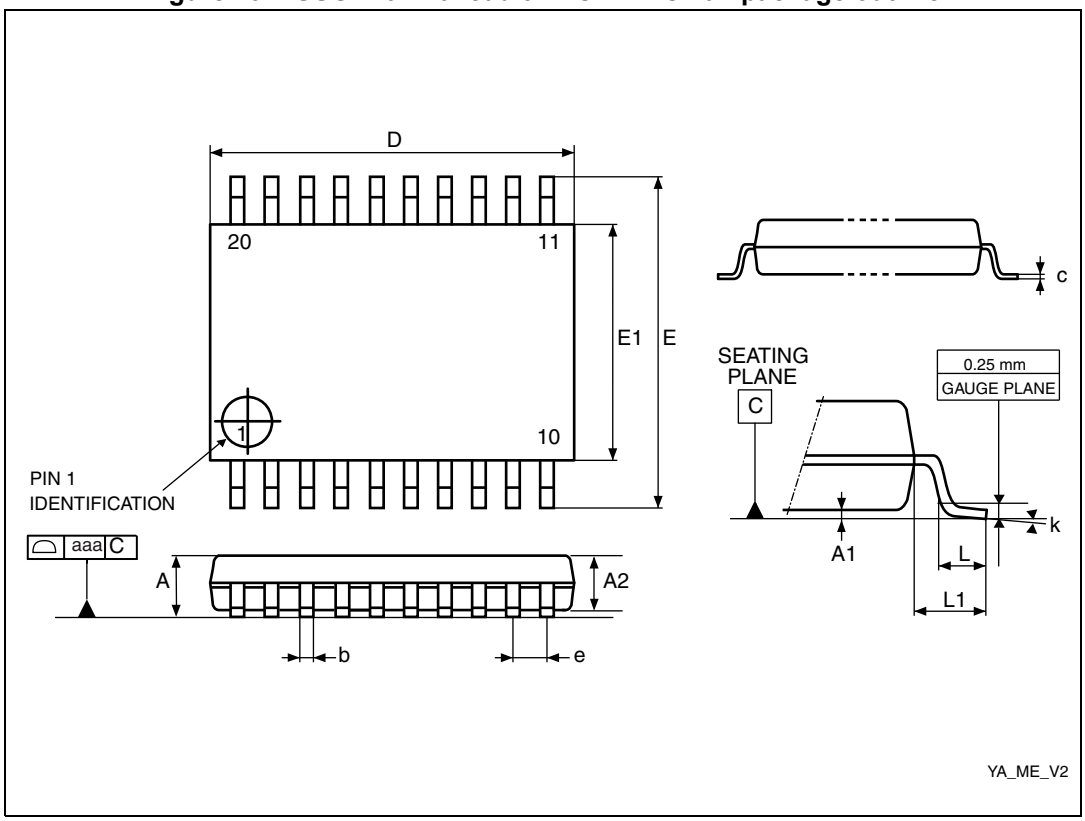
Figure 48. UFQFPN20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.5 TSSOP20 package information

Figure 49. TSSOP20 - 20-lead thin shrink small package outline



1. Drawing is not to scale.

Table 43. TSSOP20 - 20-lead thin shrink small package mechanical data

Dim.	mm				inches(1)	
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
CP	-	-	0.100	-	-	0.0039
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	0.1693	0.0256	-
L	0.450	0.600	0.750	0.1693	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

12 STM8 development tools

Development tools for the STM8 microcontrollers include the full-featured STice emulation system supported by a complete software tool package including C compiler, assembler and integrated development environment with high-level language debugger. In addition, the STM8 is to be supported by a complete range of tools including starter kits, evaluation boards and a low-cost in-circuit debugger/programmer.

12.1 Emulation and in-circuit debugging tools

The STice emulation system offers a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8 application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including profiling and coverage to help detect and eliminate bottlenecks in application execution and dead code when fine tuning an application.

In addition, STice offers in-circuit debugging and programming of STM8 microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows the users to order exactly what they need to meet their development requirements and to adapt their emulation system to support existing and future ST microcontrollers.

STice key features

- Occurrence and time profiling and code coverage (new features)
- Program and data trace recording up to 128 KB records
- Read/write on the fly of memory during emulation
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows the users to specify the components that they need to meet their development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows the user to assemble and link their application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user's application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.