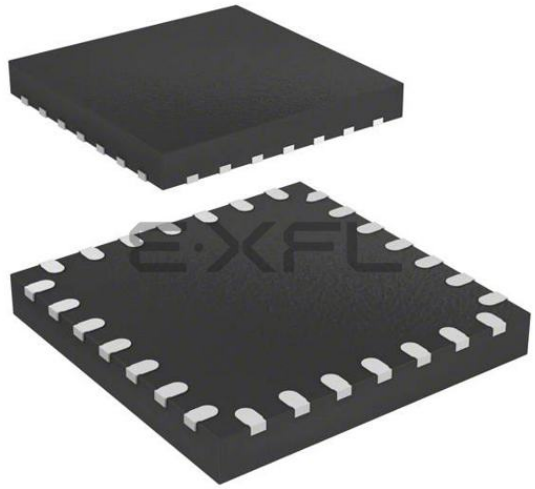

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101g2u6tr

List of figures

1 Introduction

This datasheet provides the STM8L101x1 STM8L101x2 STM8L101x3 pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller memory, registers and peripherals, please refer to the STM8L reference manual.

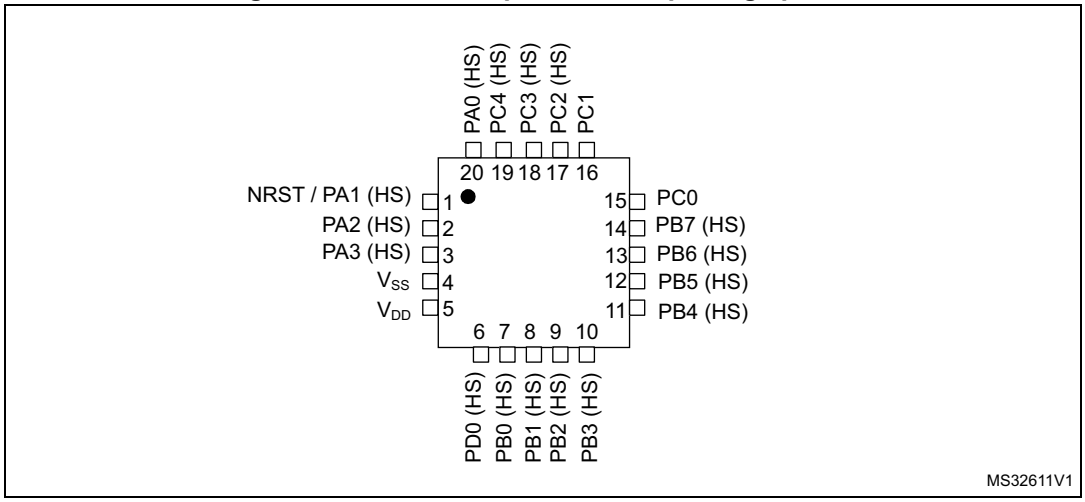
The STM8L101x1 STM8L101x2 STM8L101x3devices are members of the STM8L low-power 8-bit family. They are
referred to as low-density devices in the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller family reference manual (RM0013) and in the STM8L Flash programming manual (PM0054).

All devices of the SM8L product line provide the following benefits:

- Reduced system cost
  - Up to 8 Kbytes of low-density embedded Flash program memory including up to 2 Kbytes of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs.
  - Smaller battery and cheaper power supplies.
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MH, 0.8 µA in Active-halt mode, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Product family operating from 1.65 V to 3.6 V supply.

4 Pin description

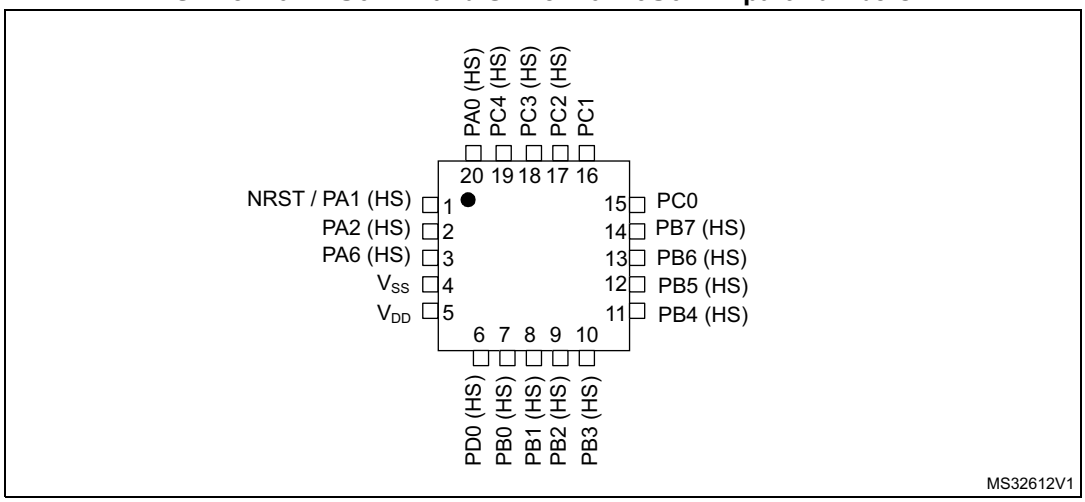
Figure 2. Standard 20-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 20-pin UFQFPN package. It is available on Port A6 in the Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers.

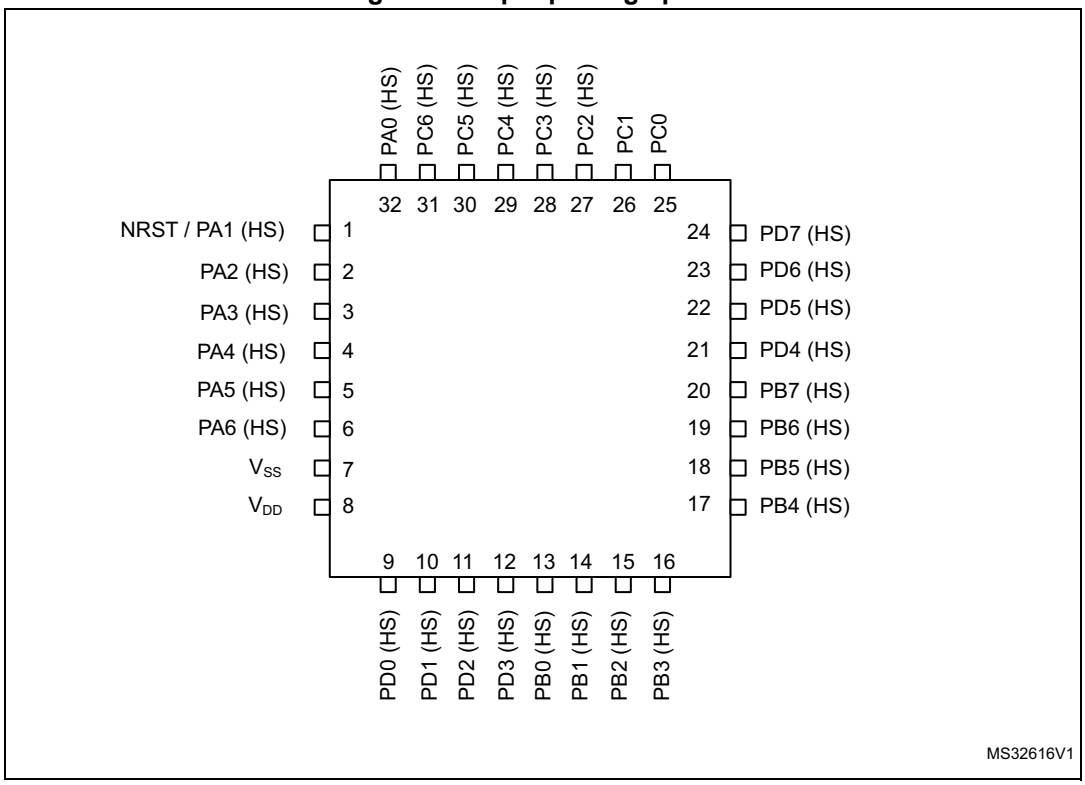
Figure 3. 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers



1. Please refer to the warning below.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Warning: **For the STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 3. Legend/abbreviation for table 4

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. STM8L101xx pin description

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	1	4	1	1	1	NRST/PA1(2)	I/O	-	**X**	-	HS	-	X	**Reset**	PA1
2	2	5	2	2	2	PA2	I/O	**X**	X	X	HS	X	X	**Port A2**	-
3	-	6	3	3	3	PA3	I/O	**X**	X	X	HS	X	X	**Port A3**	-
-	-	-	4	4	4	PA4/TIM2_BKIN	I/O	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input
-	-	-	5	-	5	PA5/TIM3_BKIN	I/O	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input
-	3	-	-	5	6	PA6/COMP_REF	I/O	**X**	X	X	HS	X	X	**Port A6**	Comparator external reference
4	4	7	6	6	7	V_{SS}	S	-	-	-	-	-	-	Ground	
5	5	8	7	7	8	V_{DD}	S	-	-	-	-	-	-	Power supply	
6	6	9	8	8	9	PD0/TIM3_CH2/ COMP1_CH3	I/O	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / Comparator 1 - channel 3
-	-	-	9	9	10	PD1/TIM3_ETR/ COMP1_CH4	I/O	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / Comparator 1 - channel 4
-	-	-	10	10	11	PD2/ COMP2_CH3	I/O	**X**	X	X	HS	X	X	**Port D2**	Comparator 2 - channel 3
-	-	-	11	11	12	PD3/ COMP2_CH4	I/O	**X**	X	X	HS	X	X	**Port D3**	Comparator 2 - channel 4

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	26	26	30	PC5	I/O	**X**	X	X	HS	X	X	**Port C5**	-
-	-	-	27	27	31	PC6	I/O	**X**	X	X	HS	X	X	**Port C6**	-
20	20	3	28	28	32	PA0(5)/SWIM/ BEEP/IR_TIM (6)	I/O	X	**X**(5)	X	HS(6)	X	X	**Port A0**	SWIM input and output /Beep output/Timer Infrared output

1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 521E to 0x00 522F	Reserved area (18 bytes)			
0x00 5230	USART	USART_SR	USART status register	0xC0
0x00 5231		USART_DR	USART data register	0xXX
0x00 5232		USART_BRR1	USART baud rate register 1	0x00
0x00 5233		USART_BRR2	USART baud rate register 2	0x00
0x00 5234		USART_CR1	USART control register 1	0x00
0x00 5235		USART_CR2	USART control register 2	0x00
0x00 5236		USART_CR3	USART control register 3	0x00
0x00 5237		USART_CR4	USART control register 4	0x00
0x00 5238 to 0x00 524F	Reserved area (18 bytes)			

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5285		TIM3_SR1	TIM3 status register 1	0x00
0x00 5286		TIM3_SR2	TIM3 status register 2	0x00
0x00 5287		TIM3_EGR	TIM3 event generation register	0x00
0x00 5288		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5289		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 528A		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 528B		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528C		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528D		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528E		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 528F		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 5290		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 5291		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 5292		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5293		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5294		TIM3_BKR	TIM3 break register	0x00
0x00 5295		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5296 to 0x00 52DF	Reserved area (74 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E4		TIM4_SR1	TIM4 Status register 1	0x00
0x00 52E5		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E6		TIM4_CNTR	TIM4 counter	0x00
0x00 52E7		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E8		TIM4_ARR	TIM4 auto-reload register low	0xFF

6 Interrupt vector mapping

Table 9. Interrupt mapping

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)	Vector address
-	RESET	Reset	Yes	Yes	Yes	Yes	0x00 8000
-	TRAP	Software interrupt	-	-	-	-	0x00 8004
0	-	Reserved	-	-	-	-	0x00 8008
1	FLASH	EOP/WR_PG_DIS	-	-	Yes	Yes(1)	0x00 800C
2-3	-	Reserved	-	-	-	-	0x00 8010 -0x00 8017
4	AWU	Auto wakeup from Halt	-	Yes	Yes	Yes(1)	0x00 8018
5	-	Reserved	-	-	-	-	0x00 801C
6	EXTIB	External interrupt port B	Yes	Yes	Yes	Yes	0x00 8020
7	EXTID	External interrupt port D	Yes	Yes	Yes	Yes	0x00 8024
8	EXTI0	External interrupt 0	Yes	Yes	Yes	Yes	0x00 8028
9	EXTI1	External interrupt 1	Yes	Yes	Yes	Yes	0x00 802C
10	EXTI2	External interrupt 2	Yes	Yes	Yes	Yes	0x00 8030
11	EXTI3	External interrupt 3	Yes	Yes	Yes	Yes	0x00 8034
12	EXTI4	External interrupt 4	Yes	Yes	Yes	Yes	0x00 8038
13	EXTI5	External interrupt 5	Yes	Yes	Yes	Yes	0x00 803C
14	EXTI6	External interrupt 6	Yes	Yes	Yes	Yes	0x00 8040
15	EXTI7	External interrupt 7	Yes	Yes	Yes	Yes	0x00 8044
16	-	Reserved	-	-	-	-	0x00 8048
17	-	Reserved	-	-	-	-	0x00 804C -0x00 804F
18	COMP	Comparators	-	-	Yes	Yes(1)	0x00 8050
19	TIM2	Update /Overflow/Trigger/Break	-	-	Yes	Yes	0x00 8054
20	TIM2	Capture/Compare	-	-	Yes	Yes	0x00 8058
21	TIM3	Update /Overflow/Break	-	-	Yes	Yes(1)	0x00 805C
22	TIM3	Capture/Compare	-	-	Yes	Yes(1)	0x00 8060
23-24	-	Reserved	-	-	-	-	0x00 8064-0x00 806B
25	TIM4	Update /Trigger	-	-	Yes	Yes(1)	0x00 806C
26	SPI	End of Transfer	Yes	Yes	Yes	Yes(1)	0x00 8070

Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power line (source)	80	mA
I_{VSS}	Total current out of V_{SS} ground line (sink)	80	
I_{IO}	Output current sunk by IR_TIM pin (with high sink LED driver capability)	80	
	Output current sunk by any other I/O and control pin	25	
	Output current sourced by any I/Os and control pin	-25	
$I_{INJ(PIN)}$	Injected current on true open-drain pins (PC0 and PC1)(1)	-5	
	Injected current on any other pin (2)	±5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) (3)	±25	

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	° C
T_J	Maximum junction temperature	150	

Table 19. Total current consumption in Wait mode(1)

Symbol	Parameter	Conditions		Typ	Max(2)	Unit
$I_{DD\ (Wait)}$	Supply current in Wait mode	CPU not clocked, all peripherals off, HSI internal RC osc.	f_{MASTER} = 2 MHz	245	400	µA
			f_{MASTER} = 4 MHz	300	450	
			f_{MASTER} = 8 MHz	380	600	
			f_{MASTER} = 16 MHz	510	800	

1. Based on characterization results, unless otherwise specified.
2. Maximum values are given for T_A = -40 to 125 °C.

Figure 13. $I_{DD(WAIT)}$ vs. V_{DD}, f_{CPU} = 2 MHz

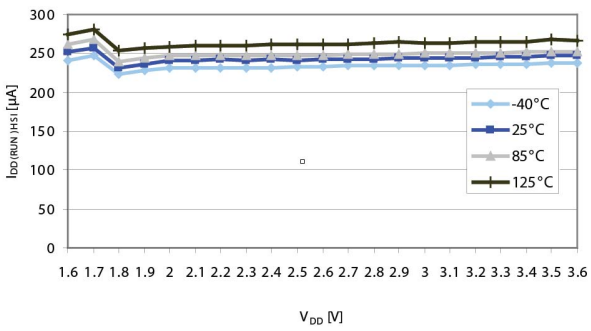
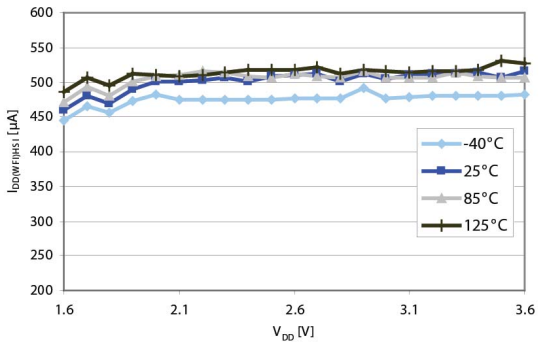


Figure 14. $I_{DD(WAIT)}$ vs. V_{DD}, f_{CPU} = 16 MHz



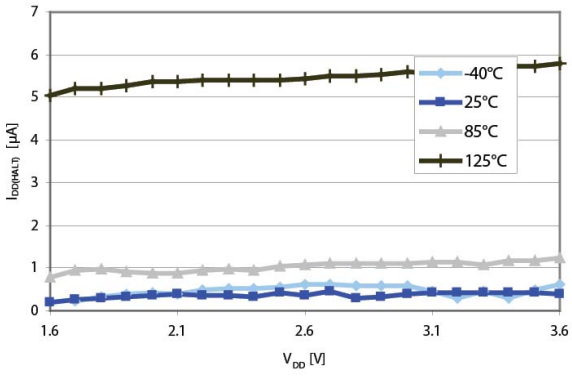
1. Typical current consumption measured with code executed from Flash.

Table 20. Total current consumption and timing in Halt and Active-halt mode at V_{DD} = 1.65 V to 3.6 V (1)(2)

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(AH)}$	Supply current in Active-halt mode	LSI RC osc. (at 37 kHz)	T_A = -40 °C to 25 °C	0.8	2	µA
			T_A = 55 °C	1	2.5	µA
			T_A = 85 °C	1.4	3.2	µA
			T_A = 105 °C	2.9	7.5	µA
			T_A = 125 °C	5.8	13	µA
$I_{DD(WUFAH)}$	Supply current during wakeup time from Active-halt mode	-	-	2	-	mA
$t_{WU(AH)}$(3)	Wakeup time from Active-halt mode to Run mode	f_{CPU}= 16 MHz		4	6.5	µs
$I_{DD(Halt)}$	Supply current in Halt mode	T_A = -40 °C to 25 °C		0.35	1.2(4)	µA
		T_A = 55 °C		0.6	1.8	µA
		T_A = 85 °C		1	2.5(4)	µA
		T_A = 105 °C		2.5	6.5	µA
		T_A = 125 °C		5.4	12(4)	µA
$I_{DD(WUFH)}$	Supply current during wakeup time from Halt mode			2	-	mA
$t_{WU(Halt)}$(3)	Wakeup time from Halt mode to Run mode	f_{CPU} = 16 MHz		4	6.5	µs

1. T_A = -40 to 125 °C, no floating I/O, unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Measured from interrupt event to interrupt vector fetch.
   To get t_{WU} for another CPU frequency use t_{WU}(FREQ) = t_{WU}(16 MHz) + 1.5 (T_{FREQ}-$T_{16\ MHz}$).
   The first word of interrupt routine is fetched 5 CPU cycles after t_{WU}.
4. Tested in production.

Figure 15. Typ. $I_{DD(Halt)}$ vs. V_{DD}, f_{CPU} = 2 MHz and 16 MHz



1. Typical current consumption measured with code executed from Flash.

Table 25. Flash program memory (continued)

Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
I_{prog}	Programming/ erasing consumption	T_A=+25 °C, V_{DD} = 3.0 V	-	0.7	-	mA
		T_A=+25 °C, V_{DD} = 1.8 V	-		-	
t_{RET}	Data retention (program memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	years
	Data retention (data memory) after 10k erase/write cycles at T_A = +85 °C	T_{RET} = 55 °C	20(1)	-	-	
	Data retention (data memory) after 300k erase/write cycles at T_A = +125 °C	T_{RET} = 85 °C	1(1)	-	-	
N_{RW}	Erase/write cycles (program memory)	See notes (1)(2)	10(1)	-	-	kcycles
	Erase/write cycles (data memory)	See notes (1)(3)	300(1)(4)	-	-	

1. Data based on characterization results, not tested in production.
2. Retention guaranteed after cycling is 10 years at 55 °C.
3. Retention guaranteed after cycling is 1 year at 55 °C.
4. Data based on characterization performed on the whole data memory (2 Kbytes).

9.3.6 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 26. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage(2)	Standard I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	V
		True open drain I/Os	V_{SS}-0.3	-	0.3 x V_{DD}	
V_{IH}	Input high level voltage (2)	Standard I/Os	0.70 x V_{DD}	-	V_{DD}+0.3	V
		True open drain I/Os V_{DD} < 2 V	0.70 x V_{DD}	-	5.2	
		True open drain I/Os V_{DD} ≥ 2 V			5.5	
V_{hys}	Schmitt trigger voltage hysteresis (3)	Standard I/Os	-	200	-	mV
		True open drain I/Os	-	250	-	

9.3.7 Communication interfaces

Serial peripheral interface (SPI)

Unless otherwise specified, the parameters given in *Table 31* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 31. SPI characteristics

Symbol	Parameter	Conditions(1)	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	30	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 x T_{MASTER}	-	
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	80	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{MASTER} = 8 MHz, f_{SCK}= 4 MHz	105	145	
$t_{su(MI)}$(2) $t_{su(SI)}$(2)	Data input setup time	Master mode	30	-	
		Slave mode	3	-	
$t_{h(MI)}$(2) $t_{h(SI)}$(2)	Data input hold time	Master mode	15	-	
		Slave mode	0	-	
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode	-	3x T_{MASTER}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	30	-	
$t_{v(SO)}$(2)	Data output valid time	Slave mode (after enable edge)	-	60	
$t_{v(MO)}$(2)	Data output valid time	Master mode (after enable edge)	-	20	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(2)		Master mode (after enable edge)	1	-	

1. Parameters are given by selecting 10-MHz I/O output frequency.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and max time is for the maximum time to put the data in Hi-Z.

Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 37. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 40*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 38. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W
	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	25	°C/W
	Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm	80	°C/W
	Thermal resistance junction-ambient UFQFPN 20 - 3 x 3 mm - 0.6 mm	102	°C/W
	Thermal resistance junction-ambient TSSOP 20	110	°C/W

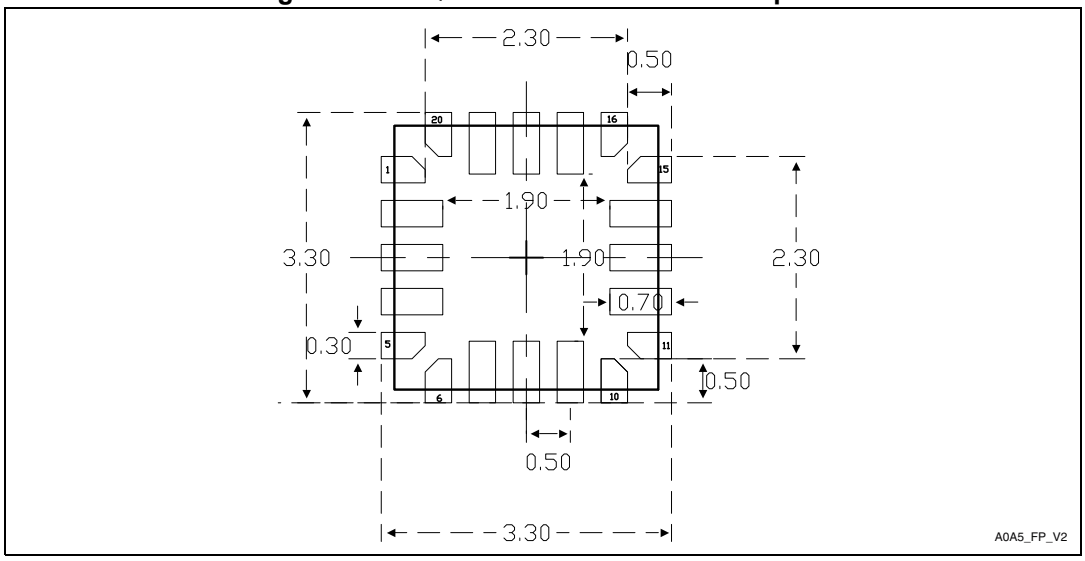
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

Table 42. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd	-	0.050	-	-	0.0020	-

1. Values in inches are rounded to 4 decimal digits

Figure 47. UFQFPN20 recommended footprint



1. Dimensions are in millimeters.

Table 44. Document revision history (continued)

Date	Revision	Changes
14-Oct-2010	11	Added STM8L101F1 devices: Modified *Table 1: Device summary on page 1*, *Table 2: STM8L101xx device feature summary on page 9* and *Table 5: Flash and RAM boundary addresses on page 24* Modified warning below *Figure 3 on page 16* and below*Table 4: STM8L101xx pin description on page 20* Modified *Figure 52: STM8L101xx ordering information scheme on page 79* Modified text above *Figure 32: Recommended NRST pin configuration on page 54* Modified *Figure 32 on page 54*
02-Aug-2013	12	Added “The RAM content is preserved” in halt mode *Section 3.6: Low power modes* Reformatted *Figure 2: Standard 20-pin UFQFPN package pinout*, *Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 5: Standard 28-pin UFQFPN package pinout*, *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers* and *Figure 7: 32-pin package pinout* Corrected NRST/PA1 pin OD output capability in *Table 4: STM8L101xx pin description* and corrected note *2.* and *4.* Added note “Slope control of all GPIO can be programmed except...” in *Table 4: STM8L101xx pin description* Added note under *Table 5: Flash and RAM boundary addresses* Replaced UM0320 with UM0470 in *Section 7: Option bytes* Updated OPT2 and OPT3 in *Table 10: Option bytes* Added additional note *2.* references in *Table 22: HSI oscillator characteristics* Added note *2.* under *Table 17: Operating conditions at power-up / power-down* and under *Figure 32: Recommended NRST pin configuration* Corrected ‘SCK output’ in *Figure 35: SPI timing diagram - master mode(1)* Added top view in *Figure 43: UFQFPN20 3 x 3 mm 0.6 mm package outline* Repositioned the package layout and footprint for all packages. Replaced “Standard ports” with “High sink ports” Replaced “TIMx_TRIG” with “TIMx_ETR” Replaced all ‘"Data guaranteed, each individual device tested in production” notes with “Tested in production”
31-Mar-2014	13	Updated L3 value on *Table 42*, added note 2) and 3) on *Table 43*