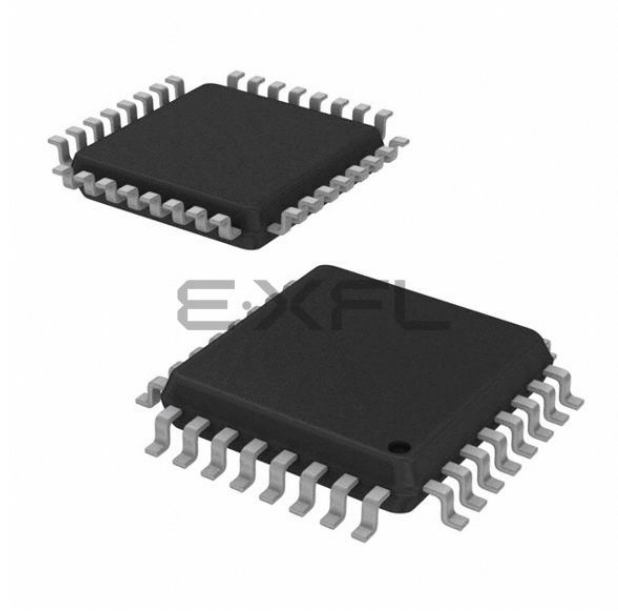

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101k3t6tr

1 Introduction

This datasheet provides the STM8L101x1 STM8L101x2 STM8L101x3 pinout, ordering information, mechanical and electrical device characteristics.

For complete information on the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller memory, registers and peripherals, please refer to the STM8L reference manual.

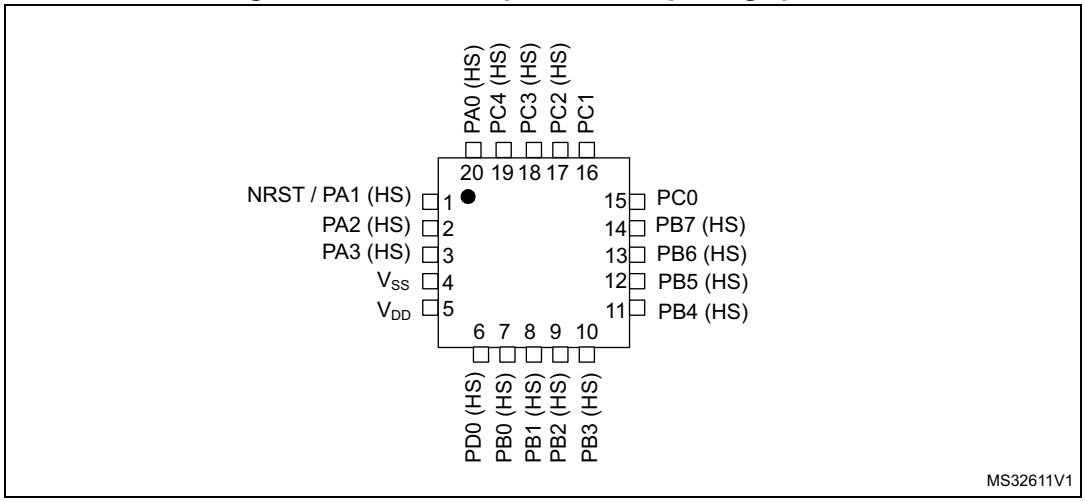
The STM8L101x1 STM8L101x2 STM8L101x3devices are members of the STM8L low-power 8-bit family. They are
referred to as low-density devices in the STM8L101x1 STM8L101x2 STM8L101x3 microcontroller family reference manual (RM0013) and in the STM8L Flash programming manual (PM0054).

All devices of the SM8L product line provide the following benefits:

- Reduced system cost
  - Up to 8 Kbytes of low-density embedded Flash program memory including up to 2 Kbytes of data EEPROM
  - High system integration level with internal clock oscillators and watchdogs.
  - Smaller battery and cheaper power supplies.
- Low power consumption and advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Less than 150 µA/MH, 0.8 µA in Active-halt mode, and 0.3 µA in Halt mode
  - Clock gated system and optimized power management
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Product family operating from 1.65 V to 3.6 V supply.

4 Pin description

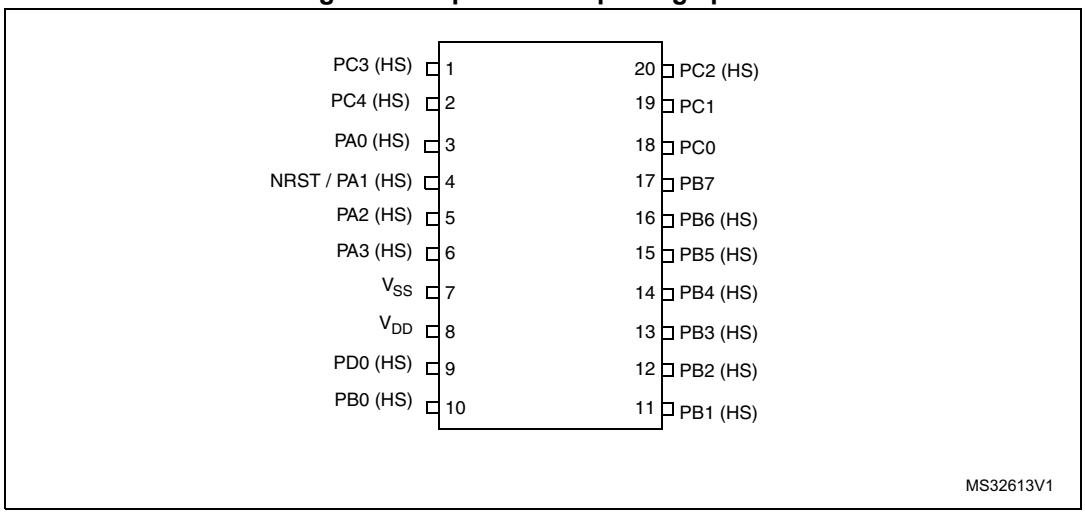
Figure 2. Standard 20-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

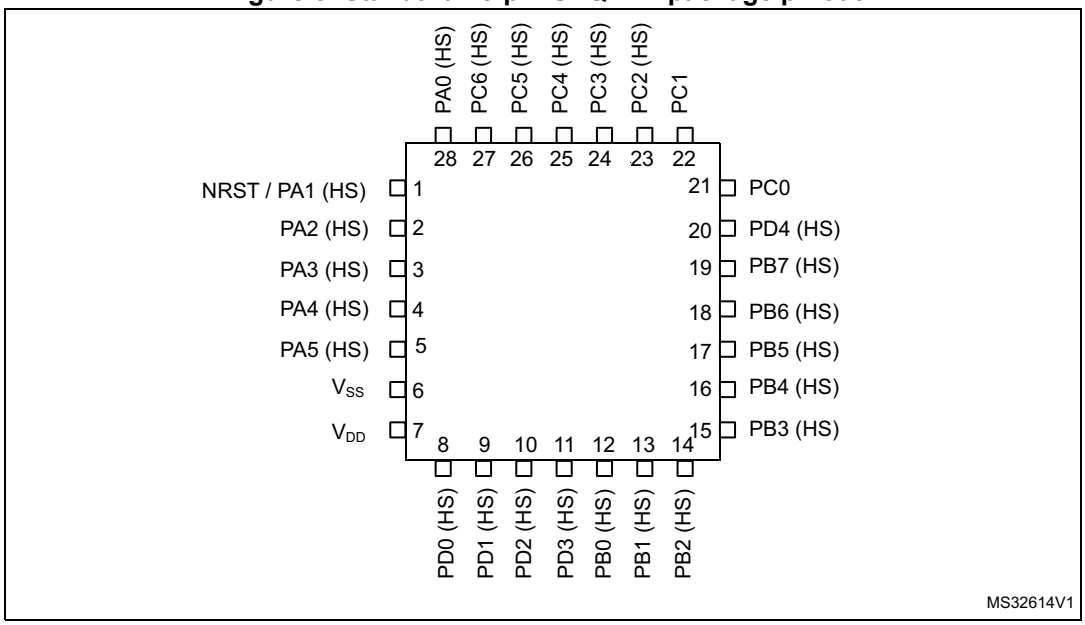
Note: The COMP_REF pin is not available in this standard 20-pin UFQFPN package. It is available on Port A6 in the Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers.

Figure 4. 20-pin TSSOP package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

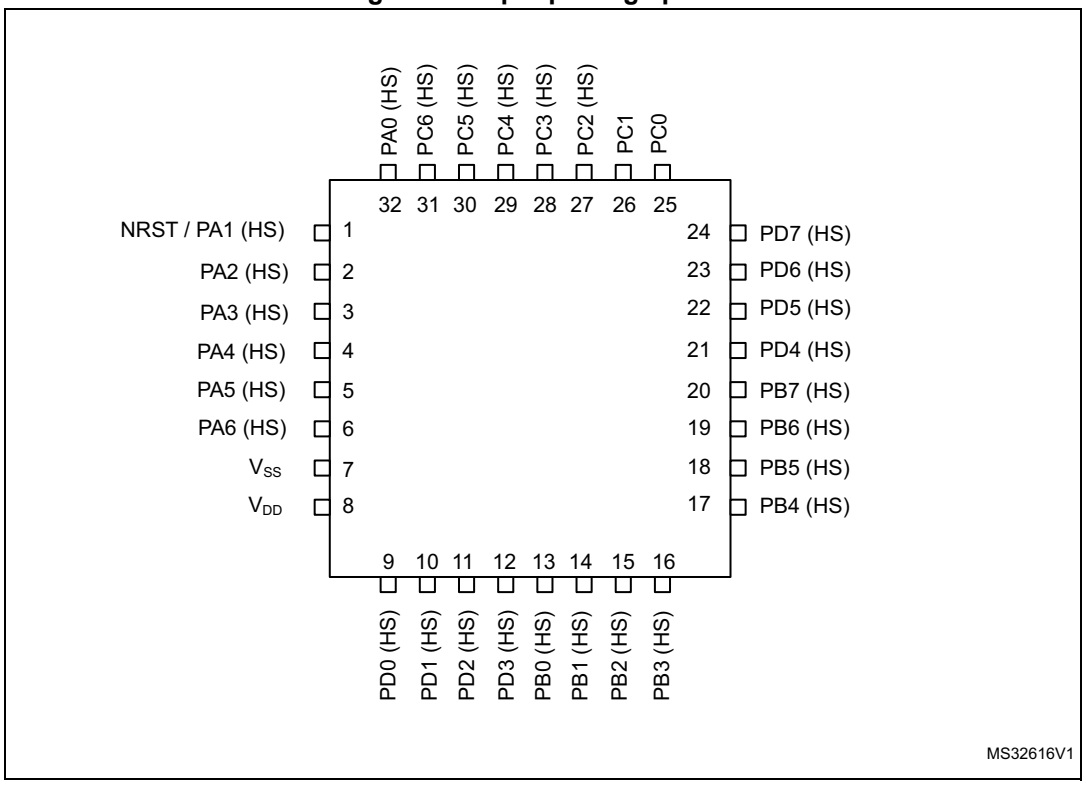
Figure 5. Standard 28-pin UFQFPN package pinout



1. HS corresponds to 20 mA high sink/source capability.
2. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Note: The COMP_REF pin is not available in this standard 28-pin UFQFPN package. It is available on Port A6 in the Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers.

Figure 7. 32-pin package pinout



1. Example given for the UFQFPN32 package. The pinout is the same for the LQFP32 package.
2. HS corresponds to 20 mA high sink/source capability.
3. High sink LED driver capability available on PA0. Refer to the description of the IR_CR register in the STM8L reference manual (RM0013).

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR	AWU control/status register	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 51FF	Reserved area (268 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205 to 0x00 520F	Reserved area (11 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 5280	TIM3	TIM3_CR1	TIM3 control register 1	0x00
0x00 5281		TIM3_CR2	TIM3 control register 2	0x00
0x00 5282		TIM3_SMCR	TIM3 slave mode control register	0x00
0x00 5283		TIM3_ETR	TIM3 external trigger register	0x00
0x00 5284		TIM3_IER	TIM3 interrupt enable register	0x00
0x00 5285		TIM3_SR1	TIM3 status register 1	0x00
0x00 5286		TIM3_SR2	TIM3 status register 2	0x00
0x00 5287		TIM3_EGR	TIM3 event generation register	0x00
0x00 5288		TIM3_CCMR1	TIM3 capture/compare mode register 1	0x00
0x00 5289		TIM3_CCMR2	TIM3 capture/compare mode register 2	0x00
0x00 528A		TIM3_CCER1	TIM3 capture/compare enable register 1	0x00
0x00 528B		TIM3_CNTRH	TIM3 counter high	0x00
0x00 528C		TIM3_CNTRL	TIM3 counter low	0x00
0x00 528D		TIM3_PSCR	TIM3 prescaler register	0x00
0x00 528E		TIM3_ARRH	TIM3 auto-reload register high	0xFF
0x00 528F		TIM3_ARRL	TIM3 auto-reload register low	0xFF
0x00 5290		TIM3_CCR1H	TIM3 capture/compare register 1 high	0x00
0x00 5291		TIM3_CCR1L	TIM3 capture/compare register 1 low	0x00
0x00 5292		TIM3_CCR2H	TIM3 capture/compare register 2 high	0x00
0x00 5293		TIM3_CCR2L	TIM3 capture/compare register 2 low	0x00
0x00 5294		TIM3_BKR	TIM3 break register	0x00
0x00 5295		TIM3_OISR	TIM3 output idle state register	0x00
0x00 5296 to 0x00 52DF	Reserved area (74 bytes)			
0x00 52E0	TIM4	TIM4_CR1	TIM4 control register 1	0x00
0x00 52E1		TIM4_CR2	TIM4 control register 2	0x00
0x00 52E2		TIM4_SMCR	TIM4 Slave mode control register	0x00
0x00 52E3		TIM4_IER	TIM4 interrupt enable register	0x00
0x00 52E4		TIM4_SR1	TIM4 Status register 1	0x00
0x00 52E5		TIM4_EGR	TIM4 event generation register	0x00
0x00 52E6		TIM4_CNTR	TIM4 counter	0x00
0x00 52E7		TIM4_PSCR	TIM4 prescaler register	0x00
0x00 52E8		TIM4_ARR	TIM4 auto-reload register low	0xFF

Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 52E9 to 0x00 52FE	Reserved area (23 bytes)			
0x00 52FF	IRTIM	IR_CR	Infra-red control register	0x00
0x00 5300	COMP	COMP_CR	Comparator control register	0x00
0x00 5301		COMP_CSR	Comparator status register	0x00
0x00 5302		COMP_CCS	Comparator channel selection register	0x00

Table 8. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
0x00 7F00	CPU	A	Accumulator	0x00
0x00 7F01		PCE	Program counter extended	0x00
0x00 7F02		PCH	Program counter high	0x80
0x00 7F03		PCL	Program counter low	0x00
0x00 7F04		XH	X index register high	0x00
0x00 7F05		XL	X index register low	0x00
0x00 7F06		YH	Y index register high	0x00
0x00 7F07		YL	Y index register low	0x00
0x00 7F08		SPH	Stack pointer high	0x05
0x00 7F09		SPL	Stack pointer low	0xFF
0x00 7F0A		CC	Condition code register	0x28
0x00 7F0B to 0x00 7F5F	Reserved area (85 bytes)			
0x00 7F60	CFG	CFG_GCR	Global configuration register	0x00
0x00 7F61 0x00 7F6F	Reserved area (15 bytes)			
0x00 7F70	ITC-SPR (1)	ITC_SPR1	Interrupt Software priority register 1	0xFF
0x00 7F71		ITC_SPR2	Interrupt Software priority register 2	0xFF
0x00 7F72		ITC_SPR3	Interrupt Software priority register 3	0xFF
0x00 7F73		ITC_SPR4	Interrupt Software priority register 4	0xFF
0x00 7F74		ITC_SPR5	Interrupt Software priority register 5	0xFF
0x00 7F75		ITC_SPR6	Interrupt Software priority register 6	0xFF
0x00 7F76		ITC_SPR7	Interrupt Software priority register 7	0xFF
0x00 7F77		ITC_SPR8	Interrupt Software priority register 8	0xFF

Table 9. Interrupt mapping (continued)

IRQ No.	Source block	Description	Wakeup from Halt mode	Wakeup from Active-halt mode	Wakeup from Wait (WFI mode)	Wakeup from Wait (WFE mode)	Vector address
27	USART	Transmission complete/transmit data register empty	-	-	Yes	Yes(1)	0x00 8074
28	USART	Receive Register DATA FULL/overrun/idle line detected/parity error	-	-	Yes	Yes(1)	0x00 8078
29	I2C	I2C interrupt(2)	Yes	Yes	Yes	Yes(1)	0x00 807C

1. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. Refer to Section *Wait for event (WFE) mode* in the RM0013 reference manual.
2. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER} (1)	Master clock frequency	1.65 V ≤V_{DD} < 3.6 V	2	16	MHz
V_{DD}	Standard operating voltage	-	1.65	3.6	V
P_D (2)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP32	-	288	mW
		UFQFPN32	-	288	
		UFQFPN28	-	250	
		TSSOP20	-	181	
		UFQFPN20	-	196	
	Power dissipation at T_A= 125 °C for suffix 3 devices	LQFP32	-	83	
		UFQFPN32	-	185	
		UFQFPN28	-	62	
		TSSOP20	-	45	
		UFQFPN20	-	49	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)	–40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)	–40	125	
T_J	Junction temperature range	-40 °C ≤T_A ≤85 °C (6 suffix version)	- 40	105	°C
		-40 °C ≤T_A ≤125 °C (3 suffix version)	–40	130	°C

1. f_{MASTER} = f_{CPU}
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”

Table 18. Total current consumption in Run mode (1)

Symbol	Parameter	Conditions(2)		Typ	Max(3)	Unit
$I_{DD\ (Run)}$	Supply current in Run mode(4) (5)	Code executed from RAM	f_{MASTER} = 2 MHz	0.39	0.60	mA
			f_{MASTER} = 4 MHz	0.55	0.70	
			f_{MASTER} = 8 MHz	0.90	1.20	
			f_{MASTER} = 16 MHz	1.60	2.10(6)	
		Code executed from Flash	f_{MASTER} = 2 MHz	0.55	0.70	
			f_{MASTER} = 4 MHz	0.88	1.80	
			f_{MASTER} = 8 MHz	1.50	2.50	
			f_{MASTER} = 16 MHz	2.70	3.50	

1. Based on characterization results, unless otherwise specified.
2. All peripherals off, V_{DD} from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}=f_{MASTER}$
3. Maximum values are given for T_A = –40 to 125 °C.
4. CPU executing typical data processing.
5. An approximate value of $I_{DD(Run)}$ can be given by the following formula: $I_{DD(Run)} = f_{MASTER}$ x 150 µA/MHz +215 µA.
6. Tested in production.

Figure 11. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 2 MHz

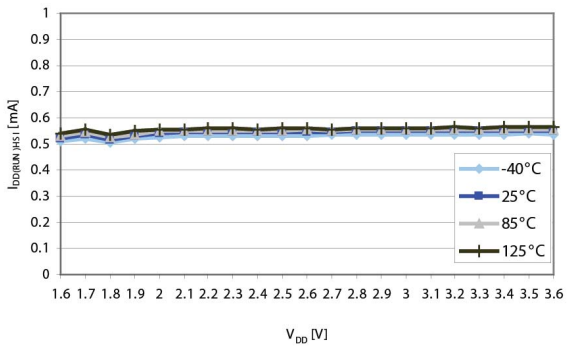
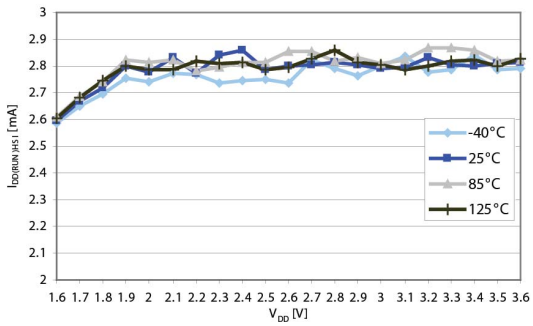


Figure 12. $I_{DD(RUN)}$ vs. V_{DD}, f_{CPU} = 16 MHz



1. Typical current consumption measured with code executed from Flash.

Figure 16. Typical HSI frequency vs. V_{DD}

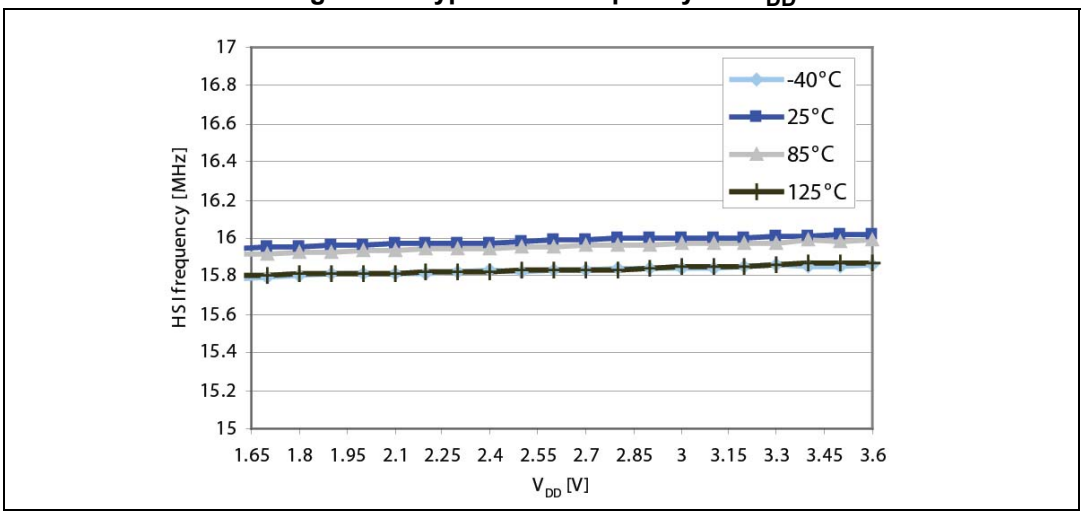


Figure 17. Typical HSI accuracy vs. temperature, V_{DD} = 3 V

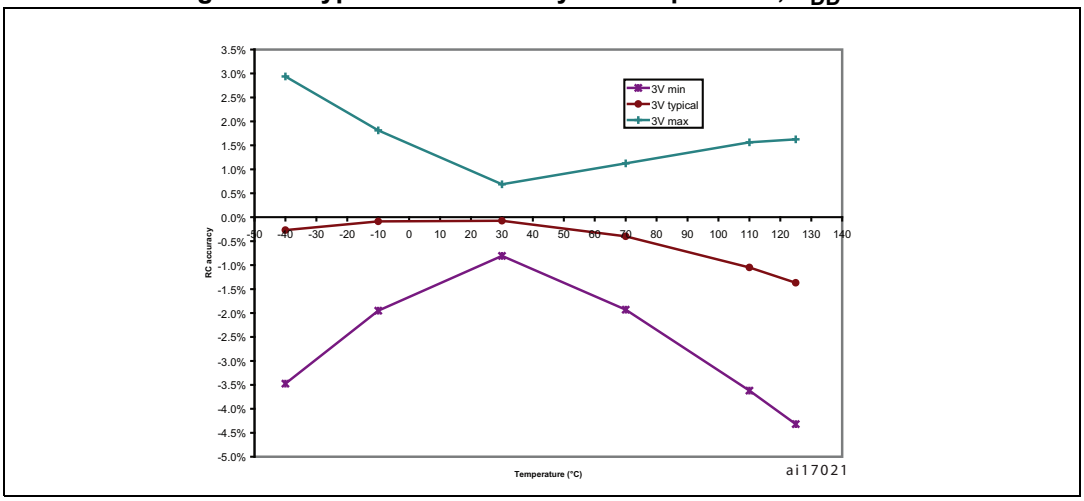


Figure 18. Typical HSI accuracy vs. temperature, V_{DD} = 1.65 V to 3.6 V

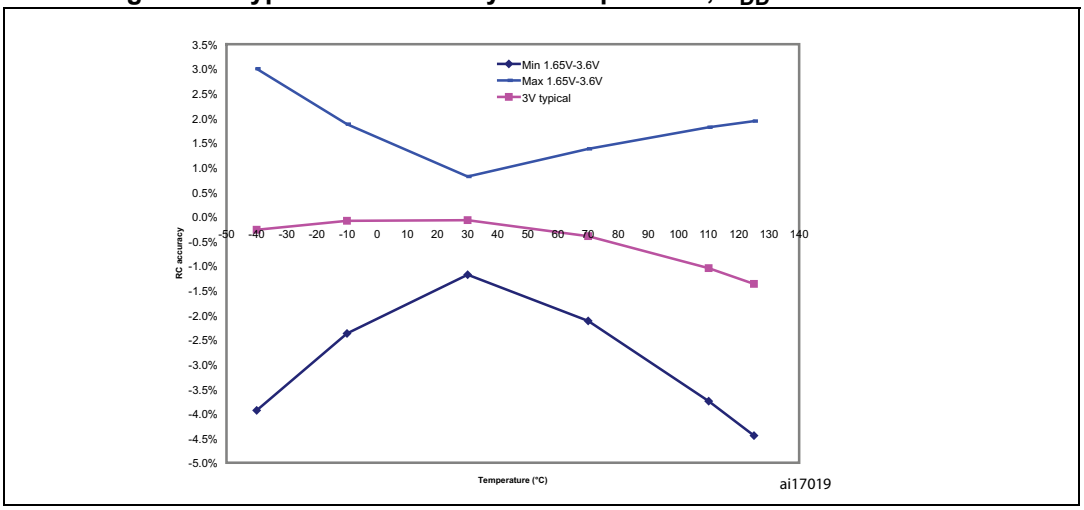


Table 26. I/O static characteristics (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(6)	$V_{IN} = V_{SS}$	30	45	60	kΩ
C_{IO}(7)	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 22*).
7. Data guaranteed by Design, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs. V_{DD} (High sink I/Os)

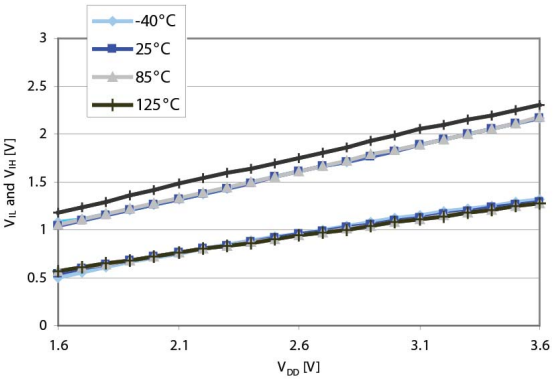


Figure 24. Typ. V_{OL} at V_{DD} = 3.0 V (High sink ports)

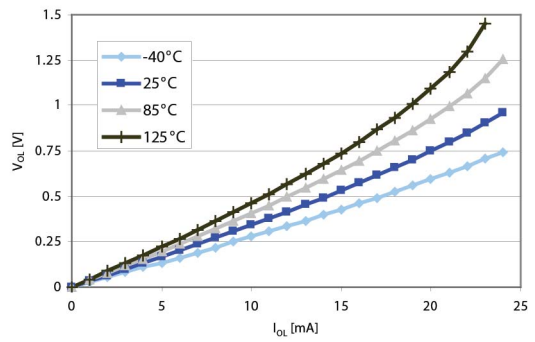


Figure 25. Typ. V_{OL} at V_{DD} = 1.8 V (High sink ports)

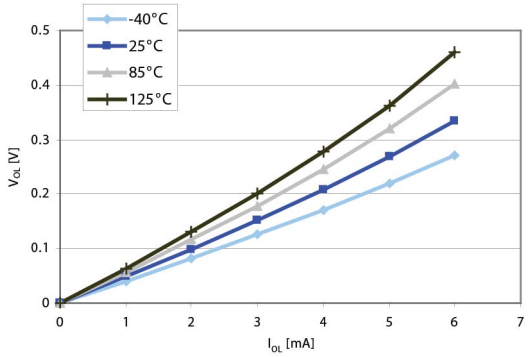


Figure 26. Typ. V_{OL} at V_{DD} = 3.0 V (true open drain ports)

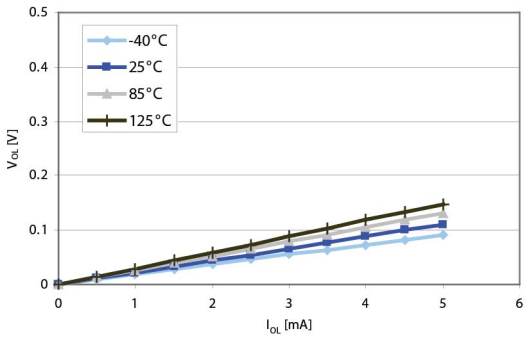


Figure 27. Typ. V_{OL} at V_{DD} = 1.8 V (true open drain ports)

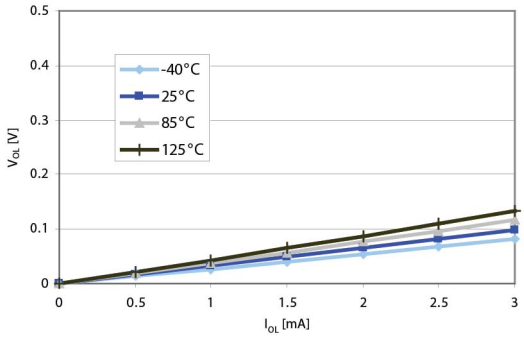


Figure 28. Typ. V_{DD} - V_{OH} at V_{DD} = 3.0 V (High sink ports)

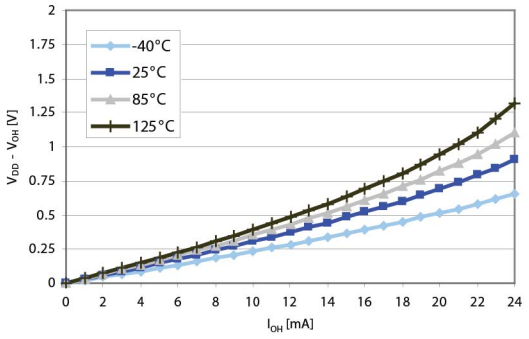


Figure 29. Typ. V_{DD} - V_{OH} at V_{DD} = 1.8 V (High sink ports)

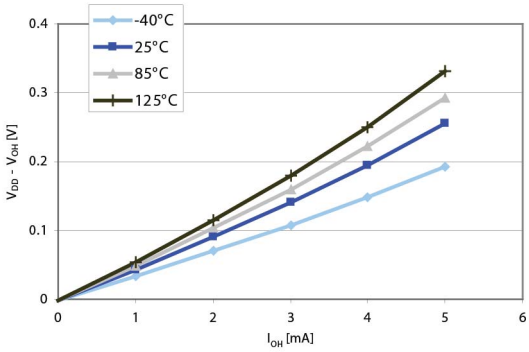


Figure 33. SPI timing diagram - slave mode and CPHA = 0

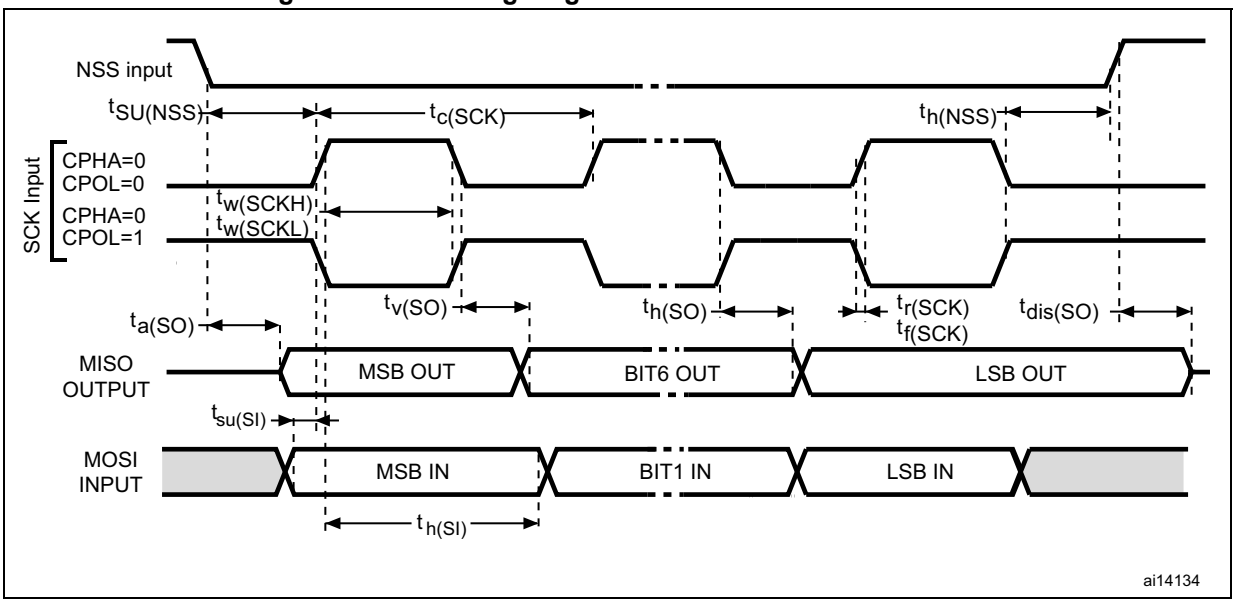
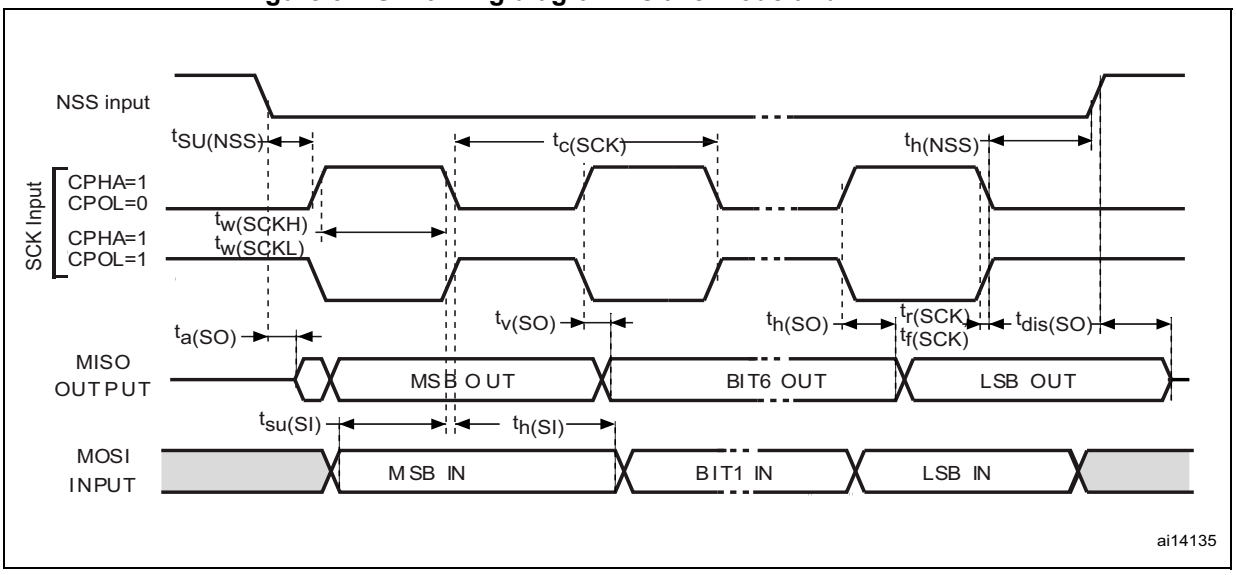


Figure 34. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

9.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. Refer to application note *Software techniques for improving microcontrollers EMC performance* (AN1015).

Table 34. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	LQFP32, V_{DD} = 3.3 V	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	LQFP32, V_{DD} = 3.3 V, f_{HSI}	3B
		LQFP32, V_{DD} = 3.3 V, $f_{HSI}/2$	4A

Static latch-up

- **LU**: 2 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 37. Electrical sensitivities

Symbol	Parameter	Class
LU	Static latch-up class	II

9.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 40*.

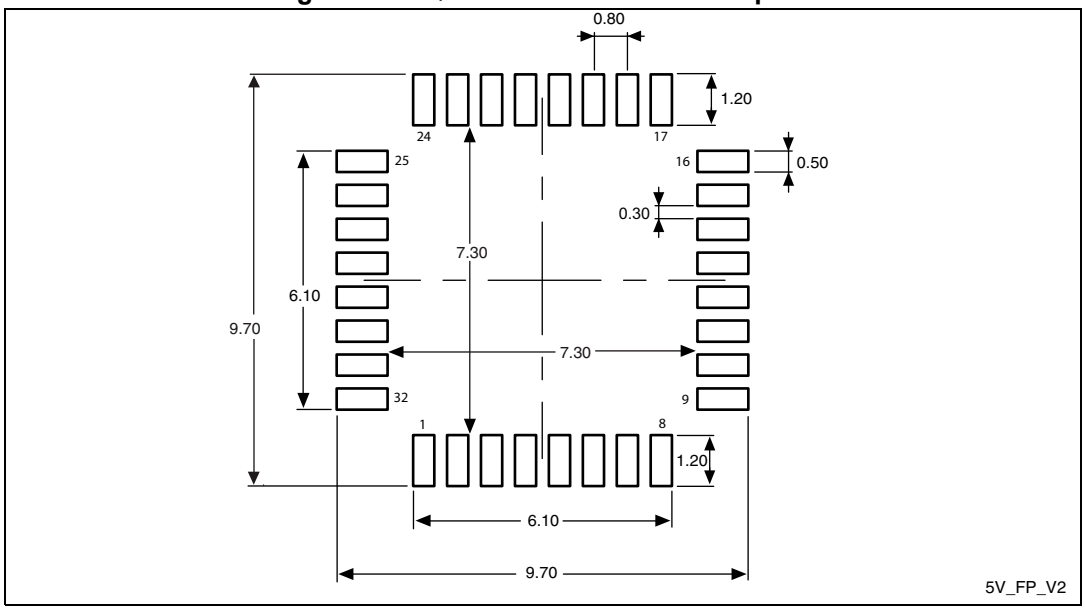
The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Figure 41. LQFP32 recommended footprint

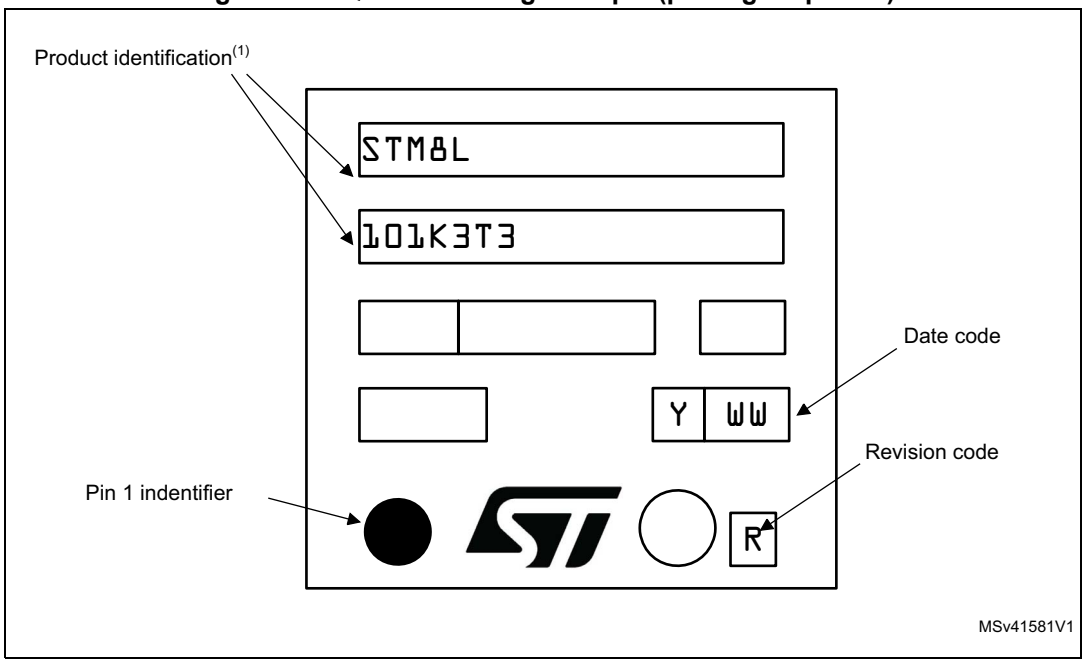


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

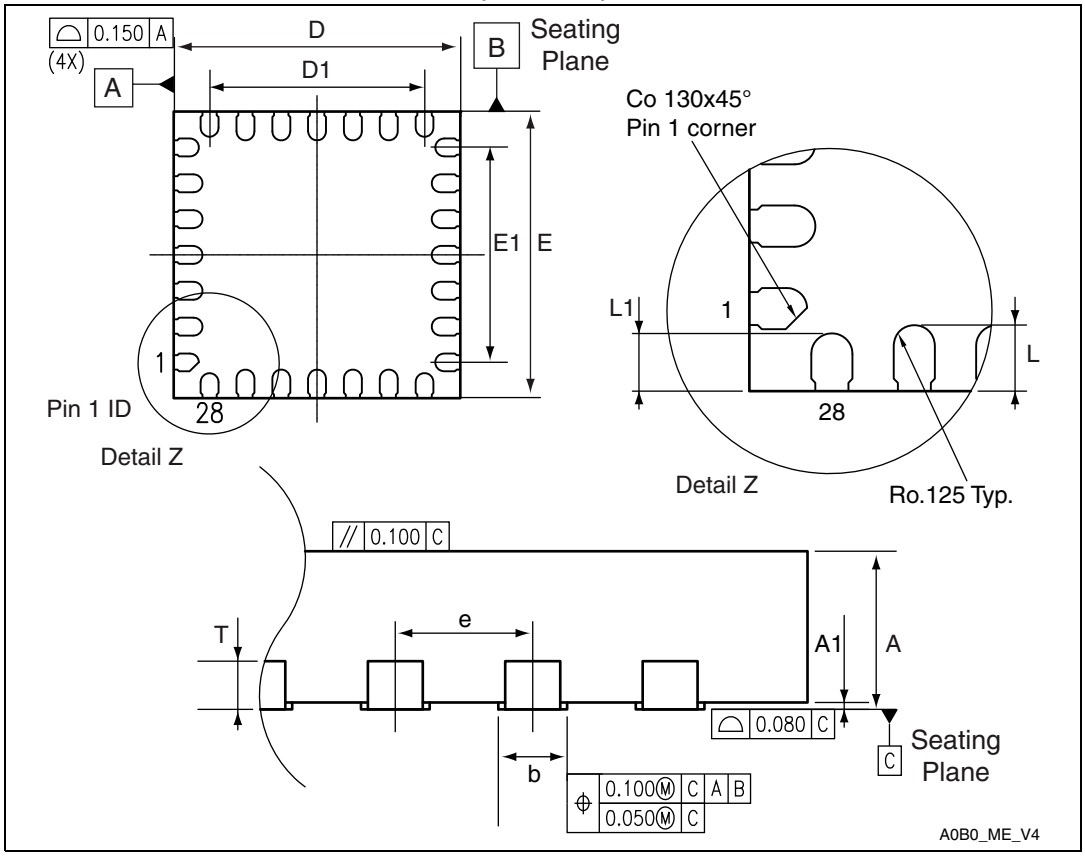
Figure 42. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

10.3 UFQFPN28 package information

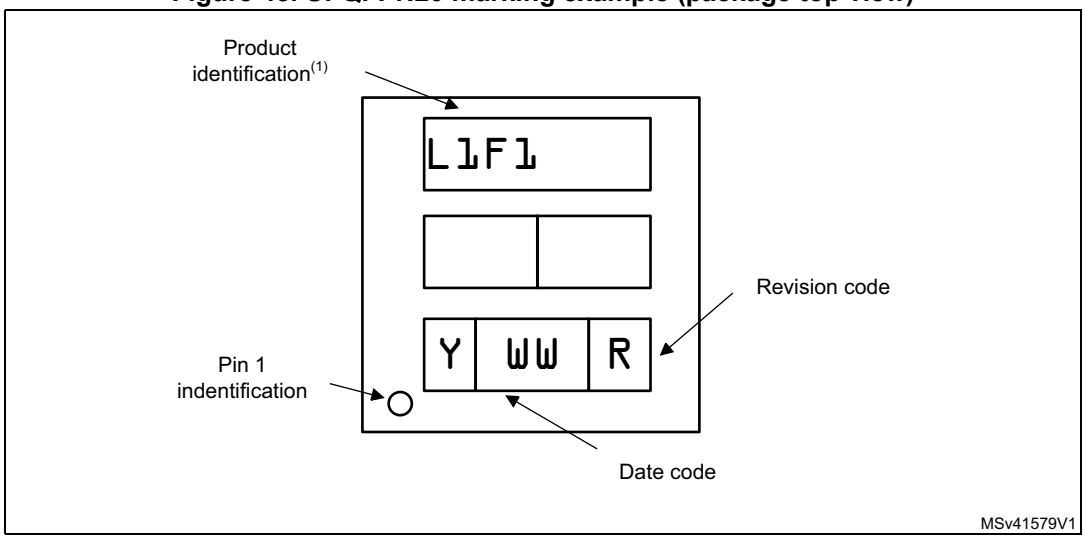
Figure 43. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4 mm)



Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 48. UFQFPN20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 44. Document revision history (continued)

Date	Revision	Changes
14-Oct-2010	11	Added STM8L101F1 devices: Modified *Table 1: Device summary on page 1*, *Table 2: STM8L101xx device feature summary on page 9* and *Table 5: Flash and RAM boundary addresses on page 24* Modified warning below *Figure 3 on page 16* and below*Table 4: STM8L101xx pin description on page 20* Modified *Figure 52: STM8L101xx ordering information scheme on page 79* Modified text above *Figure 32: Recommended NRST pin configuration on page 54* Modified *Figure 32 on page 54*
02-Aug-2013	12	Added “The RAM content is preserved” in halt mode *Section 3.6: Low power modes* Reformatted *Figure 2: Standard 20-pin UFQFPN package pinout*, *Figure 3: 20-pin UFQFPN package pinout for STM8L101F1U6ATR, STM8L101F2U6ATR and STM8L101F3U6ATR part numbers*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 4: 20-pin TSSOP package pinout*, *Figure 5: Standard 28-pin UFQFPN package pinout*, *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers* and *Figure 7: 32-pin package pinout* Corrected NRST/PA1 pin OD output capability in *Table 4: STM8L101xx pin description* and corrected note *2.* and *4.* Added note “Slope control of all GPIO can be programmed except...” in *Table 4: STM8L101xx pin description* Added note under *Table 5: Flash and RAM boundary addresses* Replaced UM0320 with UM0470 in *Section 7: Option bytes* Updated OPT2 and OPT3 in *Table 10: Option bytes* Added additional note *2.* references in *Table 22: HSI oscillator characteristics* Added note *2.* under *Table 17: Operating conditions at power-up / power-down* and under *Figure 32: Recommended NRST pin configuration* Corrected ‘SCK output’ in *Figure 35: SPI timing diagram - master mode(1)* Added top view in *Figure 43: UFQFPN20 3 x 3 mm 0.6 mm package outline* Repositioned the package layout and footprint for all packages. Replaced “Standard ports” with “High sink ports” Replaced “TIMx_TRIG” with “TIMx_ETR” Replaced all ‘"Data guaranteed, each individual device tested in production” notes with “Tested in production”
31-Mar-2014	13	Updated L3 value on *Table 42*, added note 2) and 3) on *Table 43*