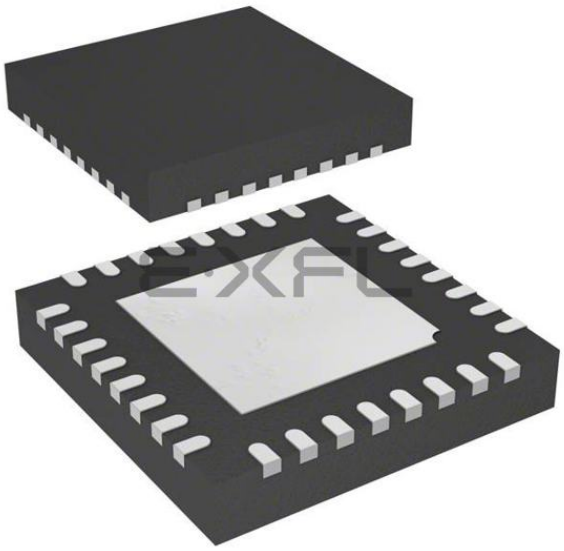

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101k3u6

List of tables

3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It features 21 internal registers, 20 addressing modes including indexed, indirect and relative addressing, and 80 instructions.

3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

3.4 Interrupt controller

The STM8L101xx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 26 interrupt vectors with hardware priority
- Up to 29 external interrupt sources on 10 vectors
- Trap and reset interrupts.

3.5 Memory

The STM8L101xx devices have the following main features:

- 1.5 Kbytes of RAM
- The EEPROM is divided into two memory arrays (see the STM8L reference manual for details on the memory mapping):
  - Up to 8 Kbytes of low-density embedded Flash program including up to 2 Kbytes of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.

Error correction code is implemented on the EEPROM.

3.6 Low power modes

To minimize power consumption, the product features three low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode: CPU and peripheral clocks are stopped. The programmable wakeup time is controlled by the AWU unit.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. Wakeup is triggered by an external interrupt.

3.7 Voltage regulators

The STM8L101xx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

3.8 Clock control

The STM8L101xx embeds a robust clock controller. It is used to distribute the system clock to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

In addition, a 38 kHz low speed internal RC oscillator is used by the independent watchdog (IWDG) and Auto-wakeup unit (AWU).

3.9 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

3.15 USART

The USART interface (USART) allows full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

3.16 SPI

The serial peripheral interface (SPI) provides half/ full duplex synchronous serial communication with external devices. It can be configured as the master and in this case it provides the communication clock (SCK) to the external slave device. The interface can also operate in multi-master configuration.

3.17 I²C

The inter-integrated circuit (I2C) bus interface is designed to serve as an interface between the microcontroller and the serial I^2C bus. It provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It manages standard and fast speed modes.

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
-	-	-	26	26	30	PC5	I/O	**X**	X	X	HS	X	X	**Port C5**	-
-	-	-	27	27	31	PC6	I/O	**X**	X	X	HS	X	X	**Port C6**	-
20	20	3	28	28	32	PA0(5)/SWIM/ BEEP/IR_TIM (6)	I/O	X	**X**(5)	X	HS(6)	X	X	**Port A0**	SWIM input and output /Beep output/Timer Infrared output

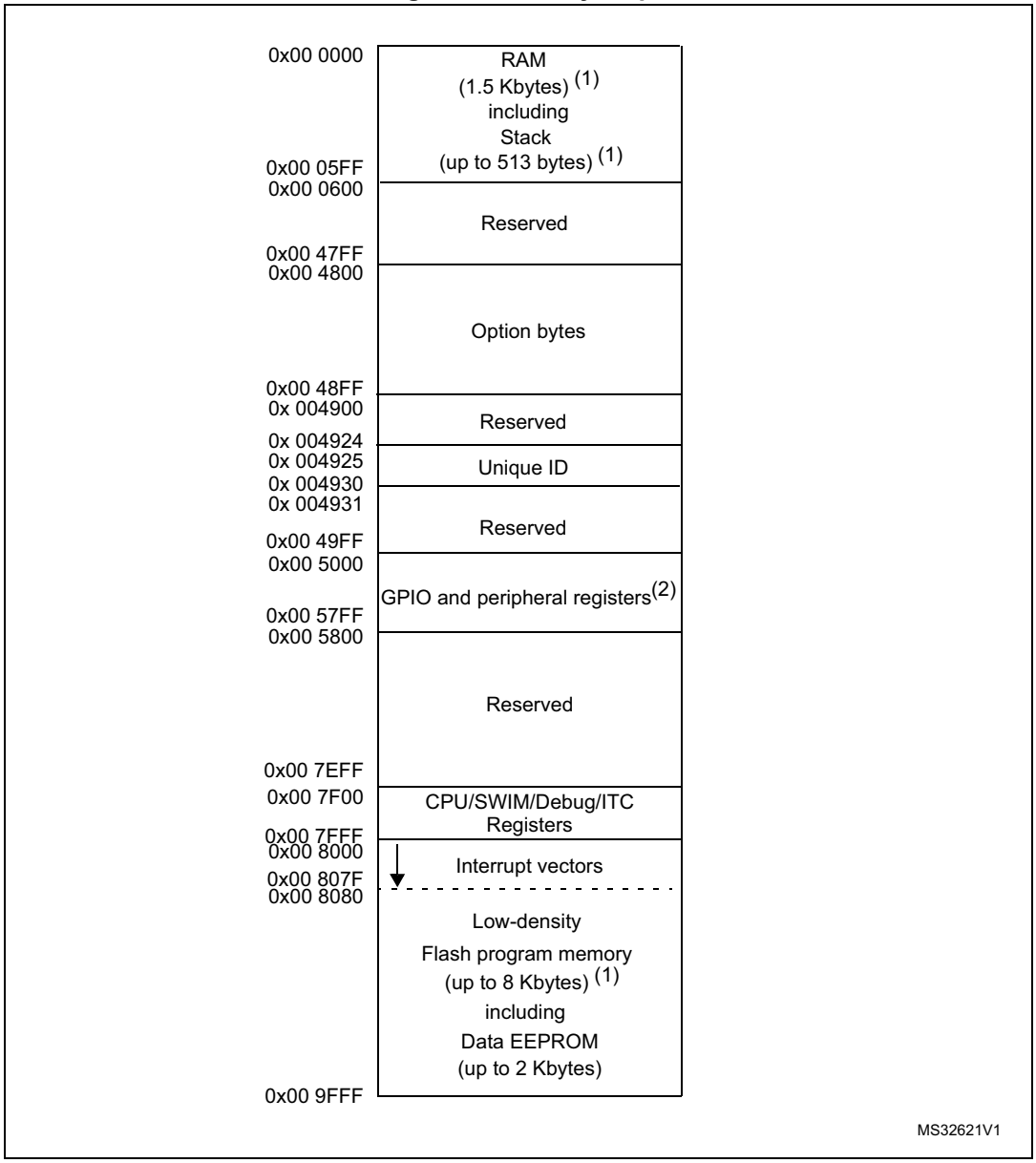
1. Please refer to the warning below.
2. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as a general purpose pin (PA1), it can be configured only as output push-pull, not neither as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L reference manual (RM0013).
3. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
4. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to V_{DD} are not implemented).
5. The PA0 pin is in input pull-up during the reset phase and after reset release.
6. High sink LED driver capability available on PA0.

Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.

Warning: For the STM8L101F1U6ATR, STM8L101F2U6ATR, STM8L101F3U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers (devices with COMP_REF pin), all ports available on 32-pin packages must be considered as active ports. To avoid spurious effects, the user has to configure them as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.

5 Memory and register map

Figure 8. Memory map



1. *Table 5* lists the boundary addresses for each memory size. The top of the stack is at the RAM end address.
2. Refer to *Table 7* for an overview of hardware register mapping, to *Table 6* for details on I/O port hardware registers, and to *Table 8* for information on CPU/SWIM/debug module controller registers.

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1.5 Kbytes	0x00 0000	0x00 05FF
Flash program memory	2 Kbytes	0x00 8000	0x00 87FF
	4 Kbytes	0x00 8000	0x00 8FFF
	8 Kbytes	0x00 8000	0x00 9FFF

Note: 2 Kbytes of Data EEPROM is only available on devices with 8 Kbytes flash program memory.

Table 6. I/O Port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xxx
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xxx
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xxx
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xxx
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00

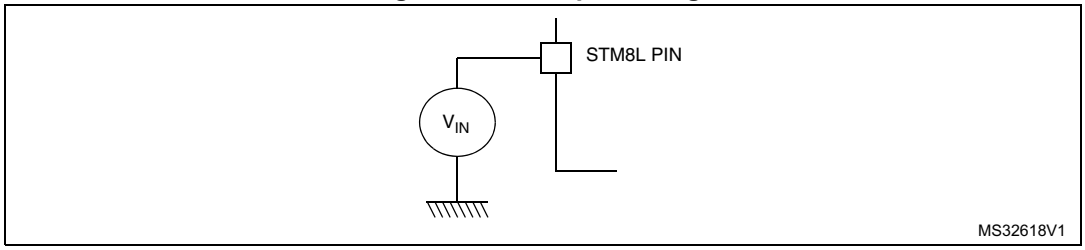
Table 7. General hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5050	Flash	FLASH_CR1	Flash control register 1	0x00
0x00 5051		FLASH_CR2	Flash control register 2	0x00
0x00 5052		FLASH _PUKR	Flash Program memory unprotection register	0x00
0x00 5053		FLASH _DUKR	Data EEPROM unprotection register	0x00
0x00 5054		FLASH _IAPSR	Flash in-application programming status register	0xX0
0x00 5055 to 0x00 509F	Reserved area (75 bytes)			
0x00 50A0	ITC-EXTI	EXTI_CR1	External interrupt control register 1	0x00
0x00 50A1		EXTI_CR2	External interrupt control register 2	0x00
0x00 50A2		EXTI_CR3	External interrupt control register 3	0x00
0x00 50A3		EXTI_SR1	External interrupt status register 1	0x00
0x00 50A4		EXTI_SR2	External interrupt status register 2	0x00
0x00 50A5		EXTI_CONF	External interrupt port select register	0x00
0x00 50A6	WFE	WFE_CR1	WFE control register 1	0x00
0x00 50A7		WFE_CR2	WFE control register 2	0x00
0x00 50A8 to 0x00 50AF	Reserved area (8 bytes)			
0x00 50B0	RST	RST_CR	Reset control register	0x00
0x00 50B1		RST_SR	Reset status register	0x01
0x00 50B2 to 0x00 50BF	Reserved area (14 bytes)			
0x00 50C0	CLK	CLK_CKDIVR	Clock divider register	0x03
0x00 50C1 to 0x00 50C2		Reserved area (2 bytes)		
0x00 50C3		CLK_PCKENR	Peripheral clock gating register	0x00
0x00 50C4		Reserved (1 byte)		
0x00 50C5		CLK_CCOR	Configurable clock control register	0x00
0x00 50C6 to 0x00 50DF	Reserved area (25 bytes)			

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on true open drain pins (PC0 and PC1)(1)	V_{SS}-0.3	V_{DD} + 4.0	
	Input voltage on any other pin (2)	V_{SS}-0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		-

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

9.3.2 Power-up / power-down operating conditions

Table 17. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	20	-	1300	µs/V
t_{TEMP}	Reset release delay	V_{DD} rising	-	1	-	ms
V_{POR}(1)(2)	Power on reset threshold	-	1.35	-	1.65(3)	V
V_{PDR}(1)(2)	Power down reset threshold	-	1.40	-	1.60	V

1. Data based on characterization results, not tested in production.
2. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.
3. Tested in production.

9.3.3 Supply current characteristics

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Current consumption of on-chip peripherals

Measurement made for f_{MASTER} = from 2 MHz to 16 MHz

Table 21. Peripheral current consumption

Symbol	Parameter	Typ. V_{DD} = 3.0 V	Unit
$I_{DD(TIM2)}$	TIM2 supply current (1)	9	µA/MHz
$I_{DD(TIM3)}$	TIM3 supply current (1)	9	
$I_{DD(TIM4)}$	TIM4 timer supply current (1)	4	
$I_{DD(USART)}$	USART supply current (2)	7	
$I_{DD(SPI)}$	SPI supply current (2)	4	
$I_{DD(I^2C1)}$	I2C supply current (2)	4	
$I_{DD(COMP)}$	Comparator supply current (2)	20	µA

1. Data based on a differential I_{DD} measurement between all peripherals off and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pin toggling. Not tested in production.
2. Data based on a differential I_{DD} measurement between the on-chip peripheral when kept under reset and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pin toggling. Not tested in production.

9.3.4 Clock and timing characteristics

Internal clock sources

Subject to general operating conditions for V_{DD} and T_A.

High speed internal RC oscillator (HSI)

Table 22. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)	V_{DD} = 3.0 V, T_A = 25 °C	-1	-	1	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 85 °C	-2.5(2)	-	2(2)	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 125 °C	-4.5(2)	-	2(2)	%
		V_{DD} = 3.0 V, 0 °C ≤T_A ≤ 55 °C	-1.5(2)	-	1.5(2)	%
		V_{DD} = 3.0 V, -10 °C ≤T_A ≤ 70 °C	-2(2)	-	2(2)	%
		1.65 V ≤ V_{DD} ≤ 3.6 V, -40 °C ≤ T_A ≤125 °C	-4.5(2)	-	3(2)	%
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	70	100(2)	µA

1. V_{DD} = 3.0 V, T_A = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.

Figure 16. Typical HSI frequency vs. V_{DD}

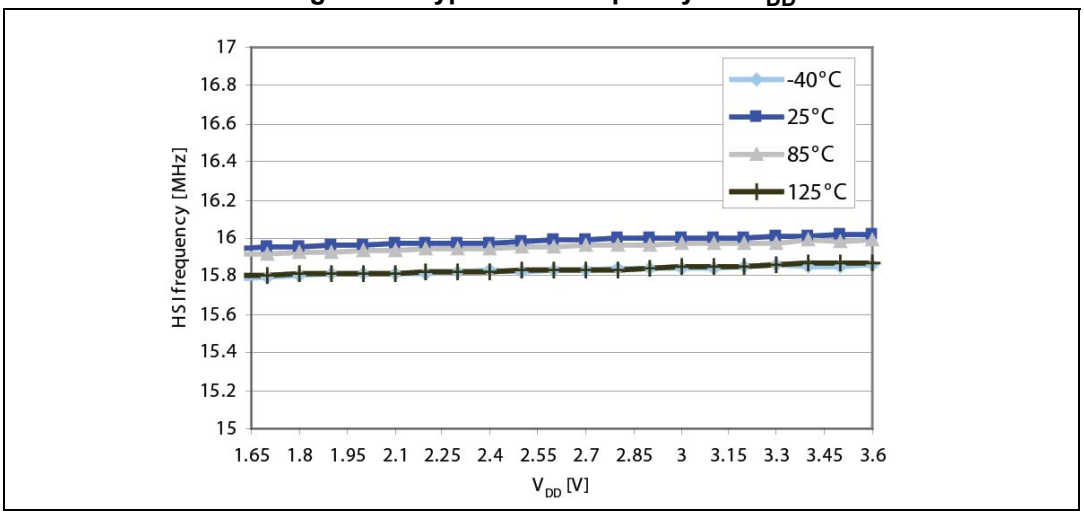


Figure 17. Typical HSI accuracy vs. temperature, V_{DD} = 3 V

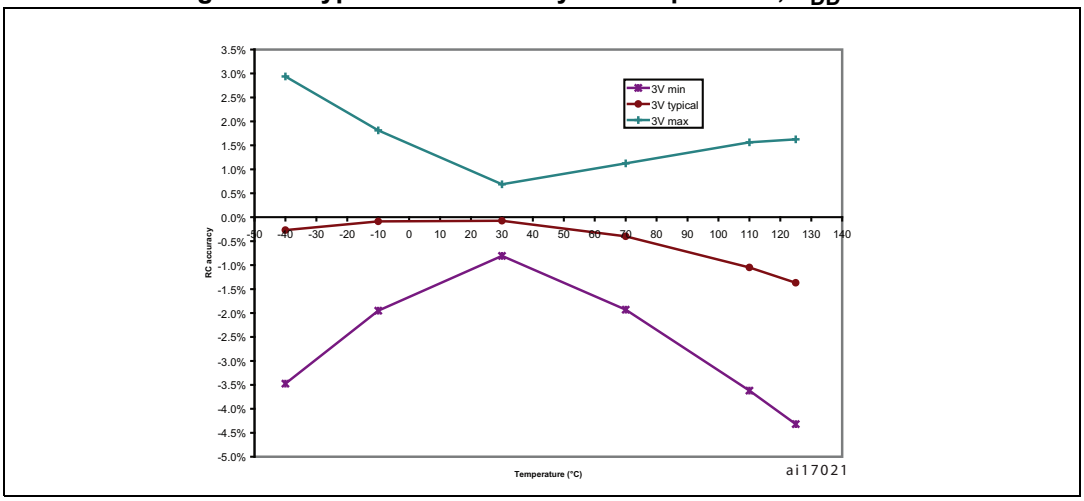


Figure 18. Typical HSI accuracy vs. temperature, V_{DD} = 1.65 V to 3.6 V

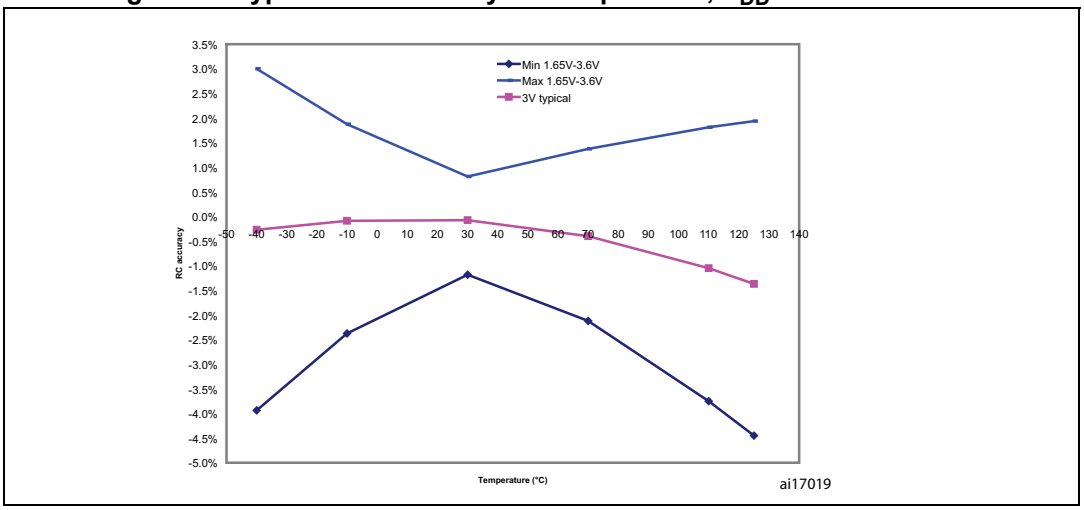


Figure 21. Typical V_{IL} and V_{IH} vs. V_{DD} (true open drain I/Os)

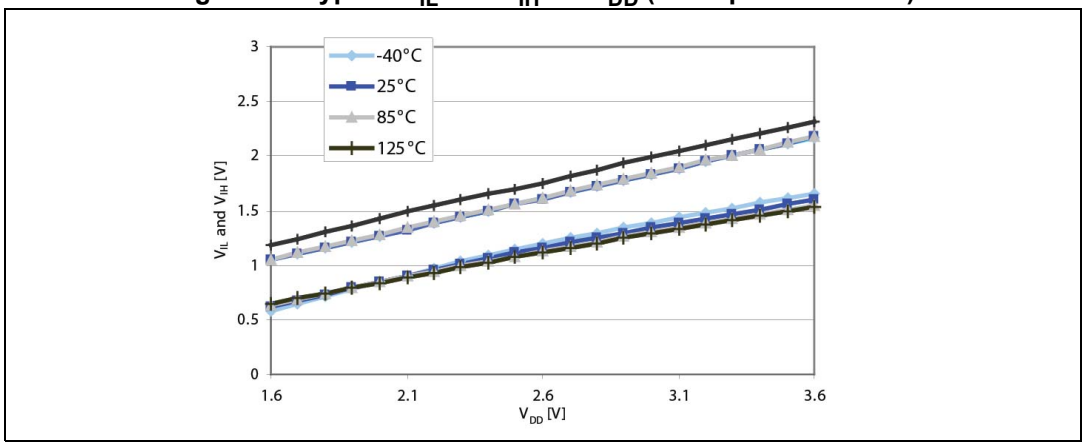


Figure 22. Typical pull-up resistance R_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$

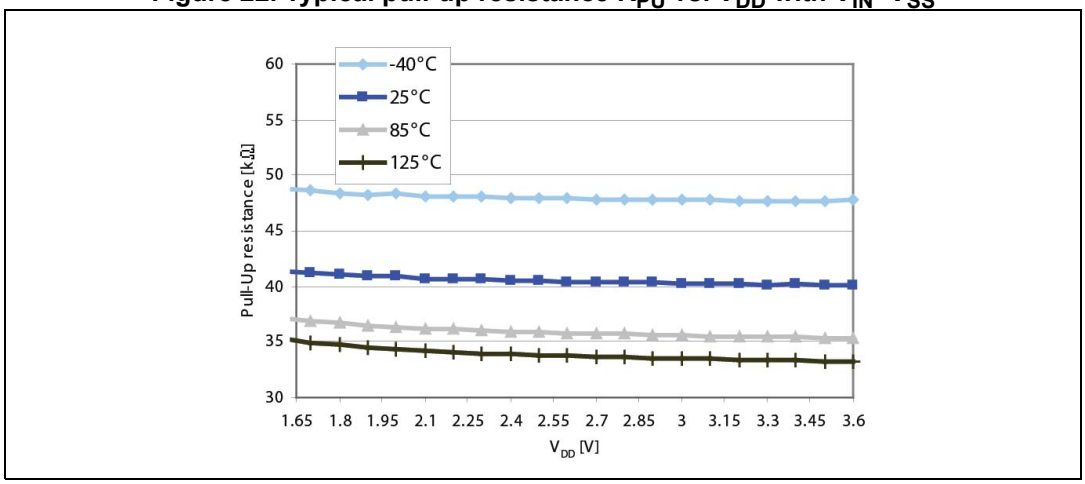
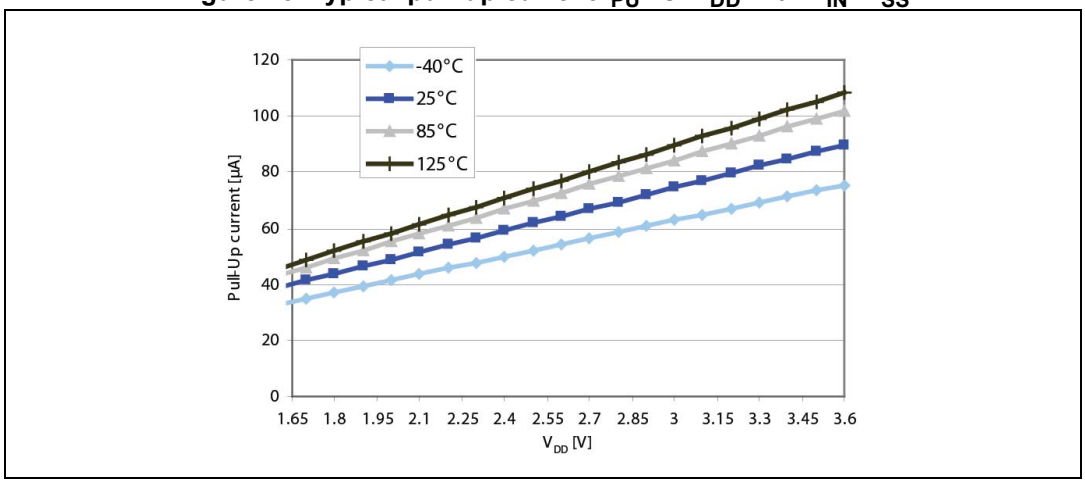


Figure 23. Typical pull-up current I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



NRST pin

The NRST pin input driver is CMOS. A permanent pull-up is present.
$R_{PU(NRST)}$ has the same value as R_{PU} (see *Table 26 on page 48*).

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 30. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ (1)	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage (1)	-	V_{SS}	-	0.8	V
$V_{IH(NRST)}$	NRST input high level voltage (1)	-	1.4	-	V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2 mA	-	-	V_{DD}-0.8	
$R_{PU(NRST)}$	NRST pull-up equivalent resistor (2)	-	30	45	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse (3)	-	-	-	50	ns
$t_{OP(NRST)}$	NRST output pulse width	-	20	-	-	ns
$V_{NF(NRST)}$	NRST input not filtered pulse (3)	-	300	-	-	ns

1. Data based on characterization results, not tested in production.
2. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (*Figure 30*). Corresponding I_{PU} current characteristics are described in *Figure 31*.
3. Data guaranteed by design, not tested in production.

Figure 30. Typical NRST pull-up resistance R_{PU} vs. V_{DD}

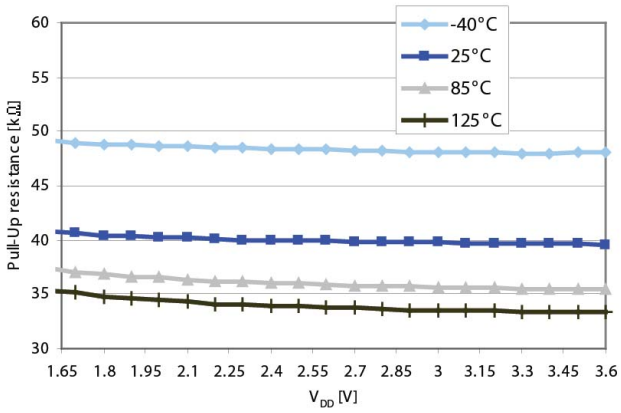
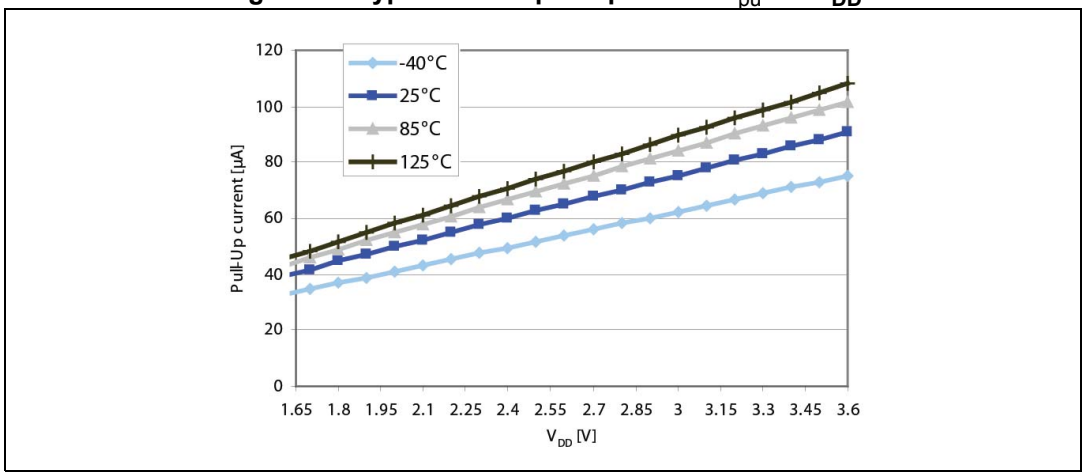
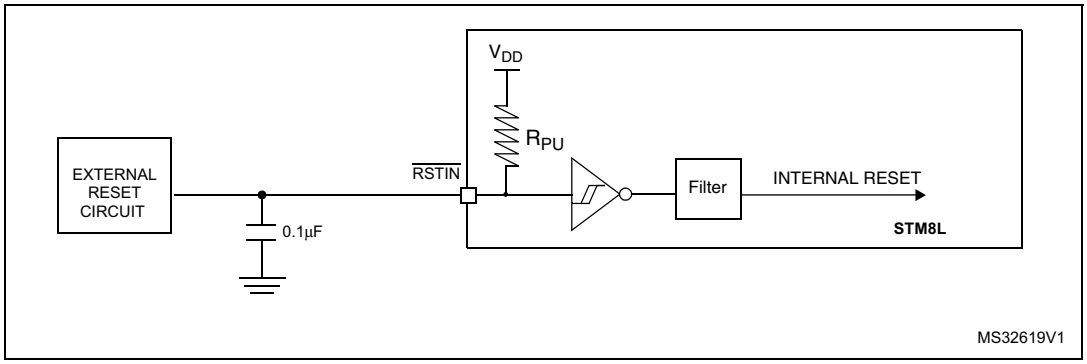


Figure 31. Typical NRST pull-up current I_{pu} vs. V_{DD}



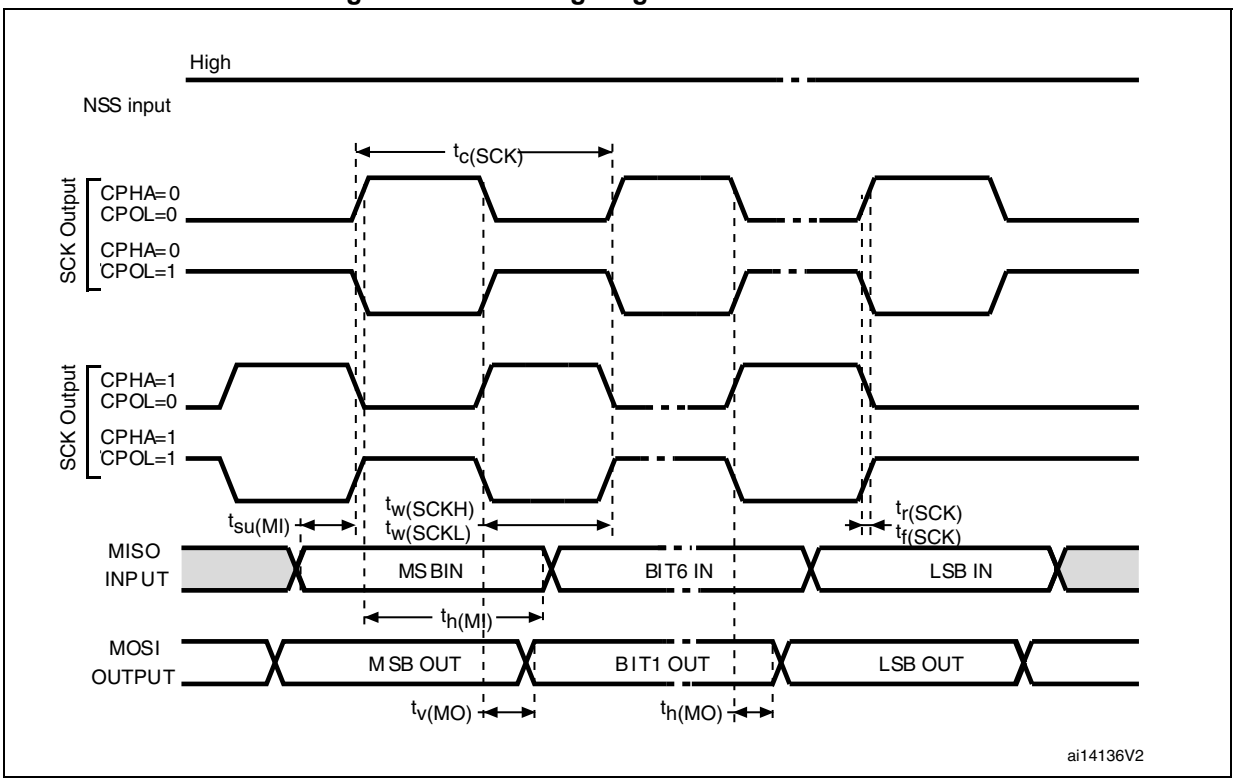
The reset network shown in *Figure 32* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 30*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

Figure 32. Recommended NRST pin configuration



1. Correct device reset during power on sequence is guaranteed when $t_{VDD[max]}$ is respected.
2. External reset circuit is recommended to ensure correct device reset during power down, when $V_{PDR} < V_{DD} < V_{DD[min]}$.

Figure 35. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Inter IC control interface (I2C)

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

The STM8L I^2C interface meets the requirements of the Standard I^2C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 32. I2C characteristics

Symbol	Parameter	Standard mode I2C		Fast mode I2C(1)		Unit
		Min(2)	Max (2)	Min (2)	Max (2)	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0 (3)	-	0 (4)	900 (3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. f_{SCK} must be at least 8 MHz to achieve max fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time of the START condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL).

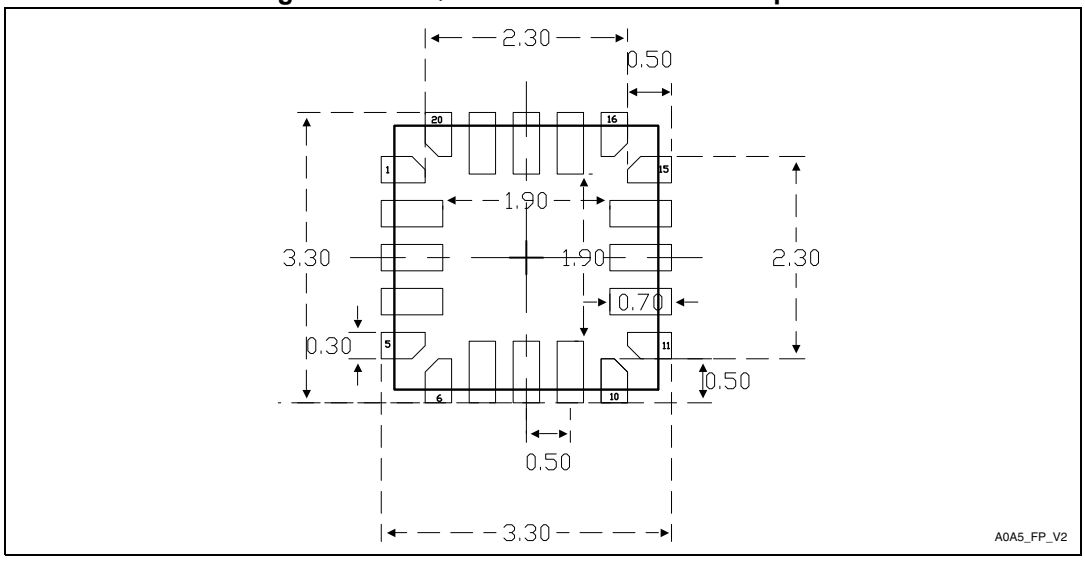
Note: For speeds around 200 kHz, achieved speed can have ±5% tolerance
For other speed ranges, achieved speed can have ±2% tolerance
The above variations depend on the accuracy of the external components used.

Table 42. UFQFPN20 - 20-lead ultra thin fine pitch quad flat package (3 x 3 mm) mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	-	3.000	-	-	0.1181	-
E	-	3.000	-	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
L5	-	0.150	-	-	0.0059	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd	-	0.050	-	-	0.0020	-

1. Values in inches are rounded to 4 decimal digits

Figure 47. UFQFPN20 recommended footprint



1. Dimensions are in millimeters.

12.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST Visual Develop (STVD) IDE and the ST Visual Programmer (STVP) software interface. STVD provides seamless integration of the Cosmic and Raisonance C compilers for STM8. A free version that outputs up to 32 Kbytes of code is available.

12.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at *www.st.com*. This package includes:

ST Visual Develop – Full-featured integrated development environment from ST, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST Visual Programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of the STM8 microcontroller Flash program memory, data EEPROM and option bytes. STVP also offers project mode for saving programming configurations and automating programming sequences.

12.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of user application directly from an easy-to-use graphical interface.

Available toolchains include:

- ***Cosmic C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code is available. For more information, see www.cosmic-software.com.
- ***Raisonance C compiler for STM8*** – One free version that outputs up to 32 Kbytes of code. For more information, see www.raisonance.com.
- ***STM8 assembler linker*** – Free assembly toolchain included in the STVD toolset, which allows the user to assemble and link their application source code.

12.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8 Flash microcontroller on the user's application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming the STM8.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.