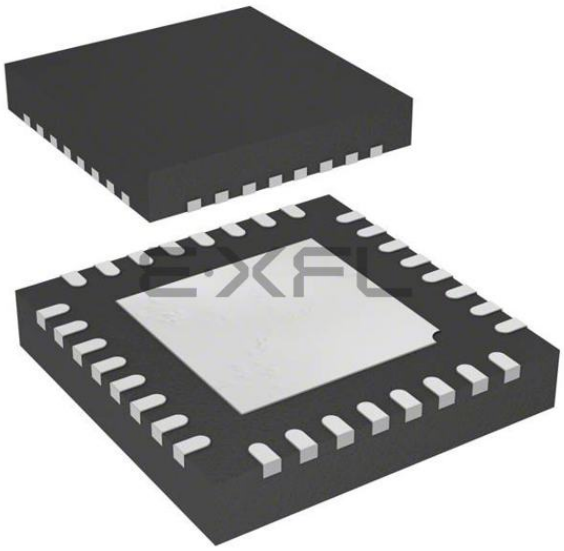

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	STM8
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Infrared, POR, PWM, WDT
Number of I/O	30
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm8l101k3u6tr

Contents

List of figures

3.1 Central processing unit STM8

The 8-bit STM8 core is designed for code efficiency and performance.

It features 21 internal registers, 20 addressing modes including indexed, indirect and relative addressing, and 80 instructions.

3.2 Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

3.3 Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, also CPU operation can be monitored in real-time by means of shadow registers.

3.4 Interrupt controller

The STM8L101xx features a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 26 interrupt vectors with hardware priority
- Up to 29 external interrupt sources on 10 vectors
- Trap and reset interrupts.

3.5 Memory

The STM8L101xx devices have the following main features:

- 1.5 Kbytes of RAM
- The EEPROM is divided into two memory arrays (see the STM8L reference manual for details on the memory mapping):
  - Up to 8 Kbytes of low-density embedded Flash program including up to 2 Kbytes of data EEPROM. Data EEPROM and Flash program areas can be write protected independently by using the memory access security mechanism (MASS).
  - 64 option bytes (one block) of which 5 bytes are already used for the device.

Error correction code is implemented on the EEPROM.

3.6 Low power modes

To minimize power consumption, the product features three low power modes:

- Wait mode: CPU clock stopped, selected peripherals at full clock speed.
- Active-halt mode: CPU and peripheral clocks are stopped. The programmable wakeup time is controlled by the AWU unit.
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. Wakeup is triggered by an external interrupt.

3.7 Voltage regulators

The STM8L101xx embeds an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes: main voltage regulator mode (MVR) and low power voltage regulator mode (LPVR). When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

3.8 Clock control

The STM8L101xx embeds a robust clock controller. It is used to distribute the system clock to the core and the peripherals and to manage clock gating for low power modes. This system clock is a 16-MHz High Speed Internal RC oscillator (HSI RC), followed by a programmable prescaler.

In addition, a 38 kHz low speed internal RC oscillator is used by the independent watchdog (IWDG) and Auto-wakeup unit (AWU).

3.9 Independent watchdog

The independent watchdog (IWDG) peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 38 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure.

Table 3. Legend/abbreviation for table 4

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS
	Output	HS = high sink/source (20 mA)
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull
Reset state	Bold X (pin state after reset release). Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state).	

Table 4. STM8L101xx pin description

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
1	1	4	1	1	1	NRST/PA1(2)	I/O	-	**X**	-	HS	-	X	**Reset**	PA1
2	2	5	2	2	2	PA2	I/O	**X**	X	X	HS	X	X	**Port A2**	-
3	-	6	3	3	3	PA3	I/O	**X**	X	X	HS	X	X	**Port A3**	-
-	-	-	4	4	4	PA4/TIM2_BKIN	I/O	**X**	X	X	HS	X	X	**Port A4**	Timer 2 - break input
-	-	-	5	-	5	PA5/TIM3_BKIN	I/O	**X**	X	X	HS	X	X	**Port A5**	Timer 3 - break input
-	3	-	-	5	6	PA6/COMP_REF	I/O	**X**	X	X	HS	X	X	**Port A6**	Comparator external reference
4	4	7	6	6	7	V_{SS}	S	-	-	-	-	-	-	Ground	
5	5	8	7	7	8	V_{DD}	S	-	-	-	-	-	-	Power supply	
6	6	9	8	8	9	PD0/TIM3_CH2/ COMP1_CH3	I/O	**X**	X	X	HS	X	X	**Port D0**	Timer 3 - channel 2 / Comparator 1 - channel 3
-	-	-	9	9	10	PD1/TIM3_ETR/ COMP1_CH4	I/O	**X**	X	X	HS	X	X	**Port D1**	Timer 3 - trigger / Comparator 1 - channel 4
-	-	-	10	10	11	PD2/ COMP2_CH3	I/O	**X**	X	X	HS	X	X	**Port D2**	Comparator 2 - channel 3
-	-	-	11	11	12	PD3/ COMP2_CH4	I/O	**X**	X	X	HS	X	X	**Port D3**	Comparator 2 - channel 4

Table 4. STM8L101xx pin description (continued)

Pin number						Pin name	Type	Input			Output			Main function (after reset)	Alternate function
standard UFQFPN20	UFQFPN20 with COMP_REF(1)	TSSOP20	standard UFQFPN28	UFQFPN28 with COMP_REF(1)	UFQFPN32 or LQFP32			floating	wpu	Ext. interrupt	High sink/source	OD	PP		
7	7	10	12	12	13	PB0/TIM2_CH1/ COMP1_CH1 (3)	I/O	**X**(3)	X(3)	X	HS	X	X	**Port B0**	Timer 2 - channel 1 / Comparator 1 - channel 1
8	8	11	13	13	14	PB1/TIM3_CH1/ COMP1_CH2	I/O	**X**	X	X	HS	X	X	**Port B1**	Timer 3 - channel 1 / Comparator 1 - channel 2
9	9	12	14	14	15	PB2/ TIM2_CH2/ COMP2_CH1/	I/O	**X**	X	X	HS	X	X	**Port B2**	Timer 2 - channel 2 / Comparator 2 - channel 1
10	10	13	15	15	16	PB3/TIM2_ETR/ COMP2_CH2	I/O	**X**	X	X	HS	X	X	**Port B3**	Timer 2 - trigger / Comparator 2 - channel 2
11	11	14	16	16	17	PB4/SPI_NSS(3)	I/O	**X**(3)	X(3)	X	HS	X	X	**Port B4**	SPI master/slave select
12	12	15	17	17	18	PB5/SPI_SCK	I/O	**X**	X	X	HS	X	X	**Port B5**	SPI clock
13	13	16	18	18	19	PB6/SPI_MOSI	I/O	**X**	X	X	HS	X	X	**Port B6**	SPI master out/ slave in
14	14	17	19	19	20	PB7/SPI_MISO	I/O	**X**	X	X	HS	X	X	**Port B7**	SPI master in/ slave out
-	-	-	20	20	21	PD4	I/O	**X**	X	X	HS	X	X	**Port D4**	-
-	-	-	-	-	22	PD5	I/O	**X**	X	X	HS	X	X	**Port D5**	-
-	-	-	-	-	23	PD6	I/O	**X**	X	X	HS	X	X	**Port D6**	-
-	-	-	-	-	24	PD7	I/O	**X**	X	X	HS	X	X	**Port D7**	-
15	15	18	21	21	25	PC0/I2C_SDA	I/O	**X**	-	X	-	T(4)		**Port C0**	I2C data
16	16	19	22	22	26	PC1/I2C_SCL	I/O	**X**	-	X	-	T(4)		**Port C1**	I2C clock
17	17	20	23	23	27	PC2/USART_RX	I/O	**X**	X	X	HS	X	X	**Port C2**	USART receive
18	18	1	24	24	28	PC3/USART_TX	I/O	**X**	X	X	HS	X	X	**Port C3**	USART transmit
19	19	2	25	25	29	PC4/USART_CK/ CCO	I/O	**X**	X	X	HS	X	X	**Port C4**	USART synchronous clock / Configurable clock output

Table 5. Flash and RAM boundary addresses

Memory area	Size	Start address	End address
RAM	1.5 Kbytes	0x00 0000	0x00 05FF
Flash program memory	2 Kbytes	0x00 8000	0x00 87FF
	4 Kbytes	0x00 8000	0x00 8FFF
	8 Kbytes	0x00 8000	0x00 9FFF

Note: 2 Kbytes of Data EEPROM is only available on devices with 8 Kbytes flash program memory.

Table 6. I/O Port hardware register map

Address	Block	Register label	Register name	Reset status
0x00 5000	Port A	PA_ODR	Port A data output latch register	0x00
0x00 5001		PA_IDR	Port A input pin value register	0xxx
0x00 5002		PA_DDR	Port A data direction register	0x00
0x00 5003		PA_CR1	Port A control register 1	0x00
0x00 5004		PA_CR2	Port A control register 2	0x00
0x00 5005	Port B	PB_ODR	Port B data output latch register	0x00
0x00 5006		PB_IDR	Port B input pin value register	0xxx
0x00 5007		PB_DDR	Port B data direction register	0x00
0x00 5008		PB_CR1	Port B control register 1	0x00
0x00 5009		PB_CR2	Port B control register 2	0x00
0x00 500A	Port C	PC_ODR	Port C data output latch register	0x00
0x00 500B		PC_IDR	Port C input pin value register	0xxx
0x00 500C		PC_DDR	Port C data direction register	0x00
0x00 500D		PC_CR1	Port C control register 1	0x00
0x00 500E		PC_CR2	Port C control register 2	0x00
0x00 500F	Port D	PD_ODR	Port D data output latch register	0x00
0x00 5010		PD_IDR	Port D input pin value register	0xxx
0x00 5011		PD_DDR	Port D data direction register	0x00
0x00 5012		PD_CR1	Port D control register 1	0x00
0x00 5013		PD_CR2	Port D control register 2	0x00

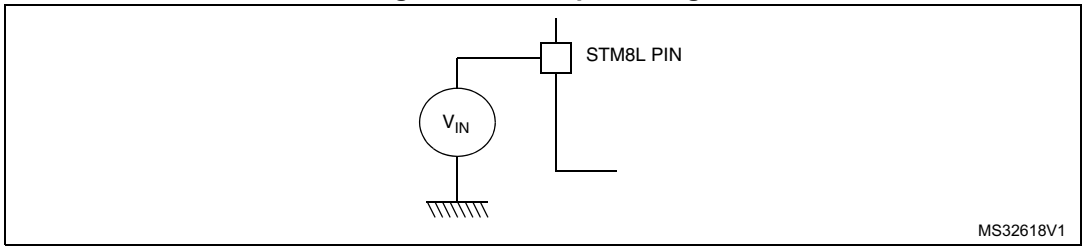
Table 7. General hardware register map (continued)

Address	Block	Register label	Register name	Reset status
0x00 50E0	IWDG	IWDG_KR	IWDG key register	0xXX
0x00 50E1		IWDG_PR	IWDG prescaler register	0x00
0x00 50E2		IWDG_RLR	IWDG reload register	0xFF
0x00 50E3 to 0x00 50EF	Reserved area (13 bytes)			
0x00 50F0	AWU	AWU_CSR	AWU control/status register	0x00
0x00 50F1		AWU_APR	AWU asynchronous prescaler buffer register	0x3F
0x00 50F2		AWU_TBR	AWU timebase selection register	0x00
0x00 50F3	BEEP	BEEP_CSR	BEEP control/status register	0x1F
0x00 50F4 to 0x00 51FF	Reserved area (268 bytes)			
0x00 5200	SPI	SPI_CR1	SPI control register 1	0x00
0x00 5201		SPI_CR2	SPI control register 2	0x00
0x00 5202		SPI_ICR	SPI interrupt control register	0x00
0x00 5203		SPI_SR	SPI status register	0x02
0x00 5204		SPI_DR	SPI data register	0x00
0x00 5205 to 0x00 520F	Reserved area (11 bytes)			
0x00 5210	I2C	I2C_CR1	I2C control register 1	0x00
0x00 5211		I2C_CR2	I2C control register 2	0x00
0x00 5212		I2C_FREQR	I2C frequency register	0x00
0x00 5213		I2C_OARL	I2C own address register low	0x00
0x00 5214		I2C_OARH	I2C own address register high	0x00
0x00 5215		Reserved area (1 byte)		
0x00 5216		I2C_DR	I2C data register	0x00
0x00 5217		I2C_SR1	I2C status register 1	0x00
0x00 5218		I2C_SR2	I2C status register 2	0x00
0x00 5219		I2C_SR3	I2C status register 3	0x00
0x00 521A		I2C_ITR	I2C interrupt control register	0x00
0x00 521B		I2C_CCRL	I2C Clock control register low	0x00
0x00 521C		I2C_CCRH	I2C Clock control register high	0x00
0x00 521D		I2C_TRISER	I2C TRISE register	0x02

9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 13: Voltage characteristics*, *Table 14: Current characteristics* and *Table 15: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. The device mission profile is compliant with the JEDEC JESD47 qualification standard; extended mission profiles are available on demand.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}- V_{SS}	External supply voltage	-0.3	4.0	V
V_{IN}	Input voltage on true open drain pins (PC0 and PC1)(1)	V_{SS}-0.3	V_{DD} + 4.0	
	Input voltage on any other pin (2)	V_{SS}-0.3	4.0	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 61*		-

1. Positive injection is not possible on these I/Os. V_{IN} maximum must always be respected. $I_{INJ(PIN)}$ must never be exceeded. A negative injection is induced by $V_{IN}<V_{SS}$.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

9.3 Operating conditions

Subject to general operating conditions for V_{DD} and T_A.

9.3.1 General operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MASTER} (1)	Master clock frequency	1.65 V ≤V_{DD} < 3.6 V	2	16	MHz
V_{DD}	Standard operating voltage	-	1.65	3.6	V
P_D (2)	Power dissipation at T_A= 85 °C for suffix 6 devices	LQFP32	-	288	mW
		UFQFPN32	-	288	
		UFQFPN28	-	250	
		TSSOP20	-	181	
		UFQFPN20	-	196	
	Power dissipation at T_A= 125 °C for suffix 3 devices	LQFP32	-	83	
		UFQFPN32	-	185	
		UFQFPN28	-	62	
		TSSOP20	-	45	
		UFQFPN20	-	49	
T_A	Temperature range	1.65 V ≤V_{DD} < 3.6 V (6 suffix version)	–40	85	°C
		1.65 V ≤V_{DD} < 3.6 V (3 suffix version)	–40	125	
T_J	Junction temperature range	-40 °C ≤T_A ≤85 °C (6 suffix version)	- 40	105	°C
		-40 °C ≤T_A ≤125 °C (3 suffix version)	–40	130	°C

1. f_{MASTER} = f_{CPU}
2. To calculate $P_{Dmax}(T_A)$ use the formula given in thermal characteristics $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with T_{Jmax} in this table and Θ_{JA} in table “Thermal characteristics”

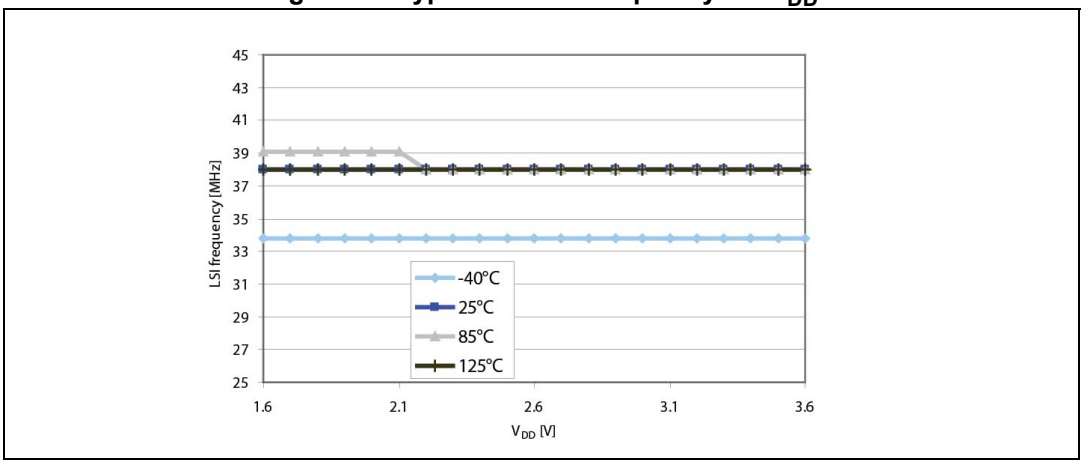
Low speed internal RC oscillator (LSI)

Table 23. LSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	-	26	38	56	kHz
$f_{drift(LSI)}$	LSI oscillator frequency drift(2)	0 °C ≤T_A ≤85 °C	-12	-	11	%

1. V_{DD} = 1.65 V to 3.6 V, T_A = -40 to 125 °C unless otherwise specified.
2. For each individual part, this value is the frequency drift from the initial measured frequency.

Figure 19. Typical LSI RC frequency vs. V_{DD}



9.3.5 Memory characteristics

T_A = -40 to 125 °C unless otherwise specified.

Table 24. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode (1)	Halt mode (or Reset)	1.4	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization, not tested in production.

Flash memory

Table 25. Flash program memory

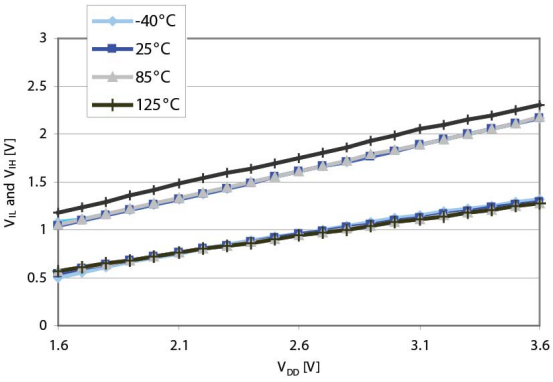
Symbol	Parameter	Conditions	Min	Typ	Max (1)	Unit
V_{DD}	Operating voltage (all modes, read/write/erase)	f_{MASTER} = 16 MHz	1.65	-	3.6	V
t_{prog}	Programming time for 1- or 64-byte (block) erase/write cycles (on programmed byte)	-	-	6	-	ms
	Programming time for 1- to 64-byte (block) write cycles (on erased byte)	-	-	3	-	ms

Table 26. I/O static characteristics (1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	50 (5)	nA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os	-	-	200(5)	
		$V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability	-	-	200(5)	
R_{PU}	Weak pull-up equivalent resistor(6)	$V_{IN} = V_{SS}$	30	45	60	kΩ
C_{IO}(7)	I/O pin capacitance	-	-	5	-	pF

1. V_{DD} = 3.0 V, T_A = -40 to 85 °C unless otherwise specified.
2. Data based on characterization results, not tested in production.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. R_{PU} pull-up equivalent resistor based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 22*).
7. Data guaranteed by Design, not tested in production.

Figure 20. Typical V_{IL} and V_{IH} vs. V_{DD} (High sink I/Os)



9.3.9 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Prequalification trials:

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring. Refer to application note *Software techniques for improving microcontrollers EMC performance* (AN1015).

Table 34. EMS data

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	LQFP32, V_{DD} = 3.3 V	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	LQFP32, V_{DD} = 3.3 V, f_{HSI}	3B
		LQFP32, V_{DD} = 3.3 V, $f_{HSI}/2$	4A

Table 38. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	60	°C/W
	Thermal resistance junction-ambient UFQFPN 32 - 5 x 5 mm	25	°C/W
	Thermal resistance junction-ambient UFQFPN 28 - 4 x 4 mm	80	°C/W
	Thermal resistance junction-ambient UFQFPN 20 - 3 x 3 mm - 0.6 mm	102	°C/W
	Thermal resistance junction-ambient TSSOP 20	110	°C/W

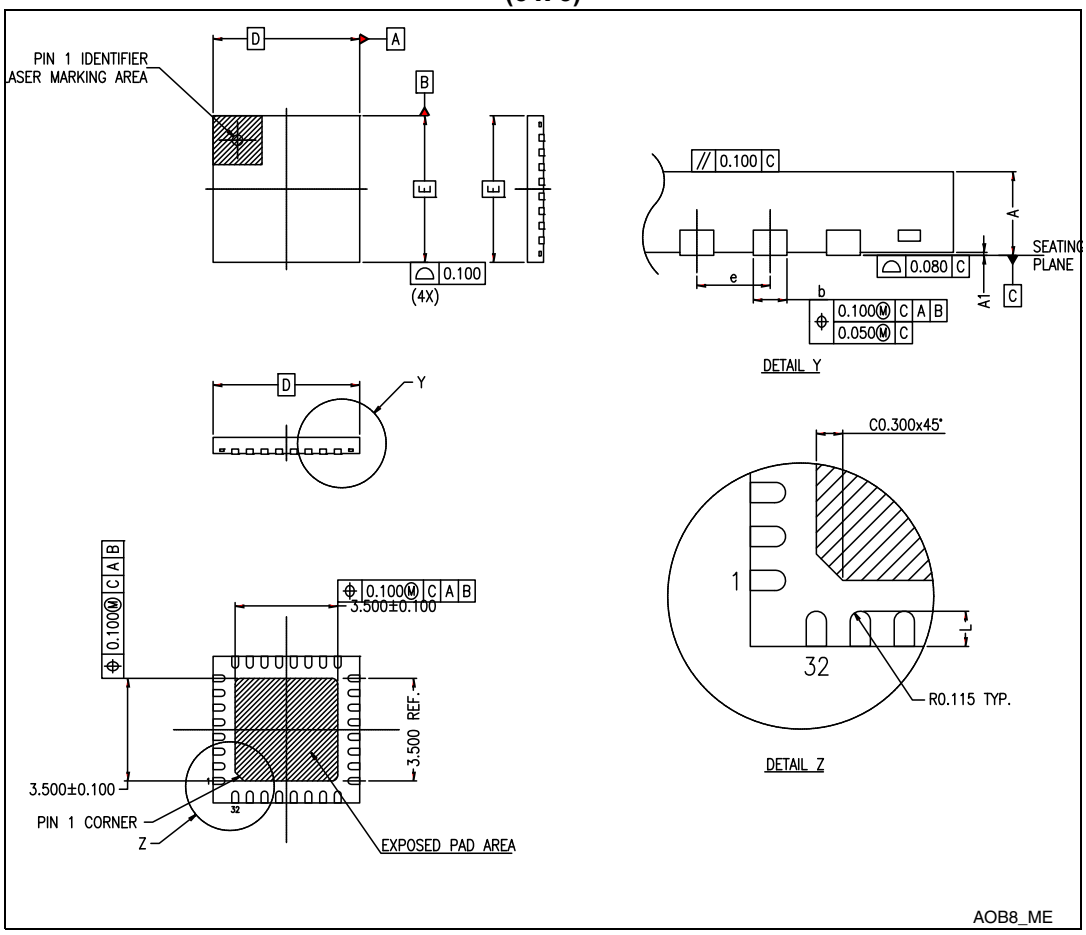
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.1 UFQFPN32 package information

Figure 37. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)



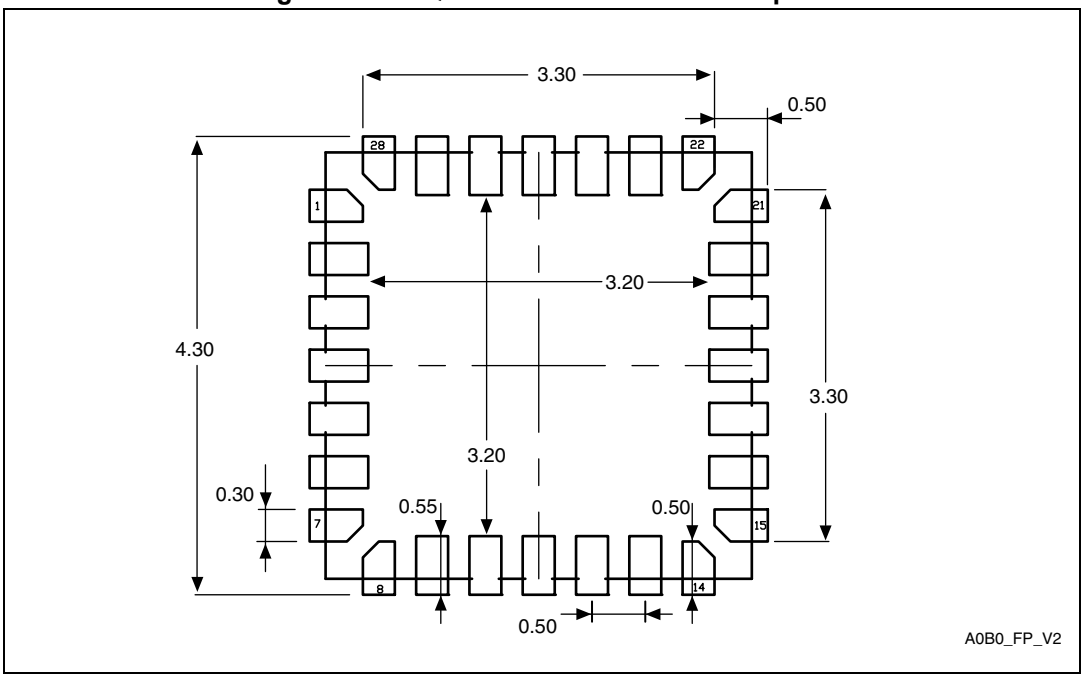
1. Drawing is not to scale.
2. All leads/pads should be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 41. UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package (4 x 4), package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0	0.020	0.050	0	0.0008	0.002
A3	-	0.152	-	-	0.0060	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
D	-	4.000	-	-	0.1575	-
E	-	4.000	-	-	0.1575	-
e	-	0.500	-	-	0.0197	-
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
L2	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	0.080	-	-	0.0031	-
-	Number of pins					
N	28					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

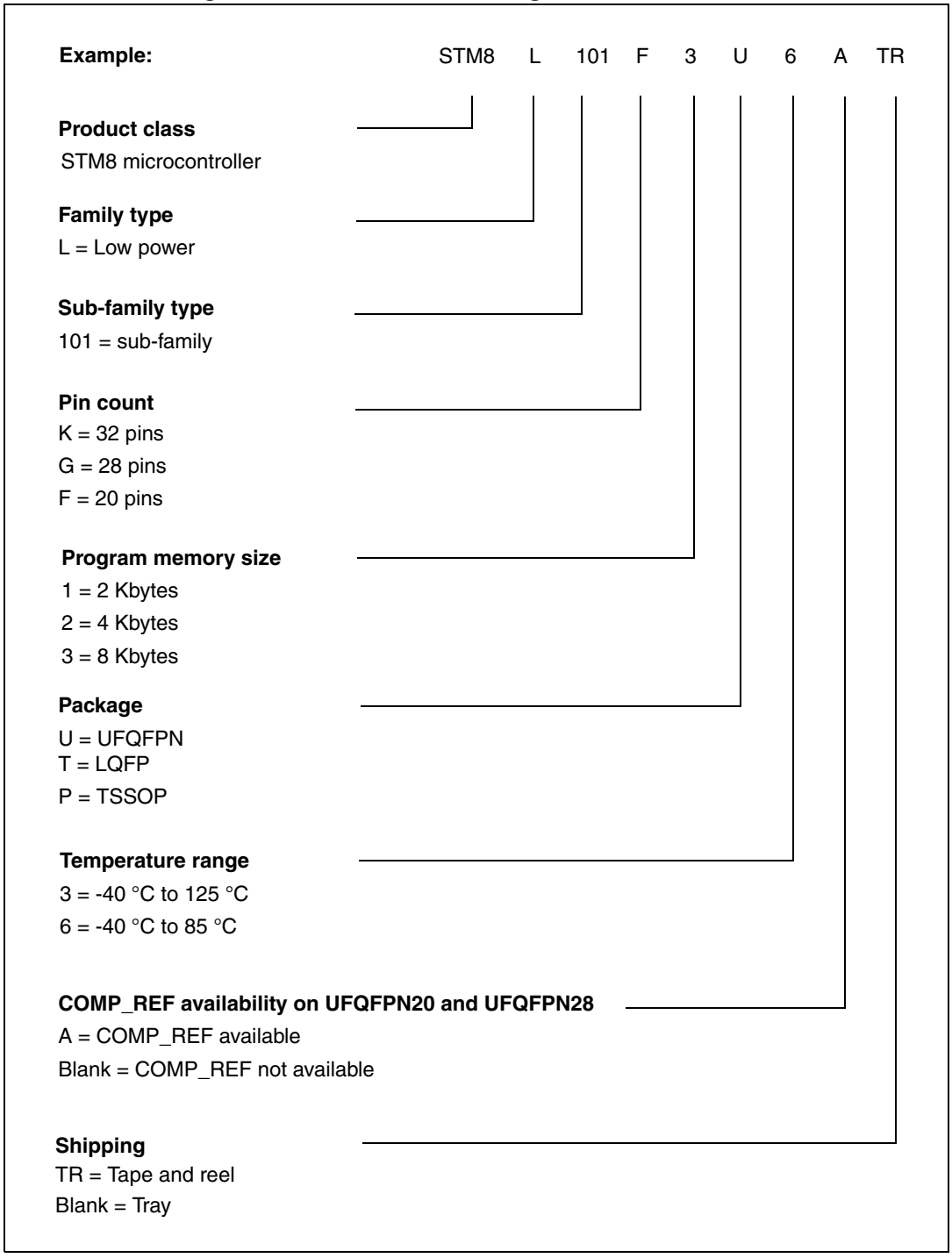
Figure 44. UFQFPN28 recommended footprint



1. Dimensions are expressed in millimeters.

11 Device ordering information

Figure 52. STM8L101xx ordering information scheme



1. For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

13 Revision history

Table 44. Document revision history

Date	Revision	Changes
19-Dec-2008	1	Initial release.
22-Apr-2009	2	Added TSSOP28 package Modified packages on first page COMPx_OUT pins removed Added *Figure 6: 28-pin TSSOP package pinout on page 17* Modified *Section 9: Electrical parameters on page 37*. Updated UBC[7:0] description in *Section 7: Option bytes*. Updated low power current consumption on cover page. Updated *Table 13: Voltage characteristics*, *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V*, *Table 26: I/O static characteristics*, *Table 30: NRST pin characteristics*, and *Section 9.3.9: EMC characteristics*. Updated PA1/NRST, PC0 and PC1 in *Table 4: STM8L101xx pin description*. Added ECC feature. Changed internal RC frequency to 38 kHz. Updated electrical characteristics in *Table 16*, *Table 18*, *Table 19*, *Table 20*, *Table 22*, *Table 23*, and *Table 26*.
24-Apr-2009	3	Corrected title on cover page. Changed VFQFPN32 to WFQFPN32 and updated *Table 39: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data*. Updated *Table 13*, *Table 26*, and *Table 33*.
14-May-2009	4	Replaced WFQFPN20 3 x 3 mm 0.8 mm package by UFQFPN20 3 x 3 mm 0.6 mm package (first page, *Table 16: General operating conditions on page 40*, *Table 38: Thermal characteristics on page 63*, *Section 10.2: Package mechanical data on page 67*) Added one UFQFPN20 version with COMP_REF Modified *Figure 40: LQFP32 recommended footprint(1) on page 69* Added I_{PROG} values in *Table 25: Flash program memory on page 47* Updated *Table 31: SPI characteristics on page 55*
15-May-2009	5	Added STM8L101F3U6ATR part number in *Section 4: Pin description on page 15* and in *Figure 47: STM8L101xx ordering information scheme on page 74*

Table 44. Document revision history (continued)

Date	Revision	Changes
07-Sep-2009	7	Added STM8L101F2U6ATR, STM8L101G2U6ATR and STM8L101G3U6ATR part numbers Modified *Section 2: Description on page 9*. Modified *Table 2: STM8L101xx device feature summary on page 9* (Flash) Modified *Figure 1: STM8L101xx device block diagram on page 10* Modified *Section 3.5: Memory on page 12* Added note below *Figure 2: Standard 20-pin UFQFPN package pinout on page 15* and *Figure 5: Standard 28-pin UFQFPN package pinout on page 17* Added *Figure 6: 28-pin UFQFPN package pinout for STM8L101G3U6ATR and STM8L101G2U6ATR part numbers on page 18* Modified reset values for Px_IDR registers in *Table 6: I/O Port hardware register map on page 24* Added *Section 6: Interrupt vector mapping on page 32* Modified OPT numbers in *Section 7: Option bytes* Modified OPT2 in *Table 10: Option bytes* Added *Section 8: Unique ID on page 36* TIM_IR pin replaced with IR_TIM pin Modified *Table 20: Total current consumption and timing in Halt and Active-halt mode at VDD = 1.65 V to 3.6 V on page 44* Modified *Figure 15: Typ. IDD(Halt) vs. VDD, fCPU = 2 MHz and 16 MHz on page 44* and *Figure 19: Typical LSI RC frequency vs. VDD on page 47* Modified *Table 27: Output driving current (High sink ports) on page 51* Updated *Table 29: Output driving current (PA0 with high sink LED driver capability) on page 51* Modified *: Functional EMS (electromagnetic susceptibility) on page 60* Modified conditions in *Table 35: EMI data on page 61* Added note to *Figure 37: UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5) on page 67* Modified *Figure 41: UFQFPN28 - 28-lead ultra thin fine pitch quad flat no-lead package outline (4 x 4)(1) on page 70* Added *Figure 44: UFQFPN20 recommended footprint (1) on page 71* Added *Figure 46: TSSOP20 recommended footprint (1) on page 72* CMP replaced with COMP