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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

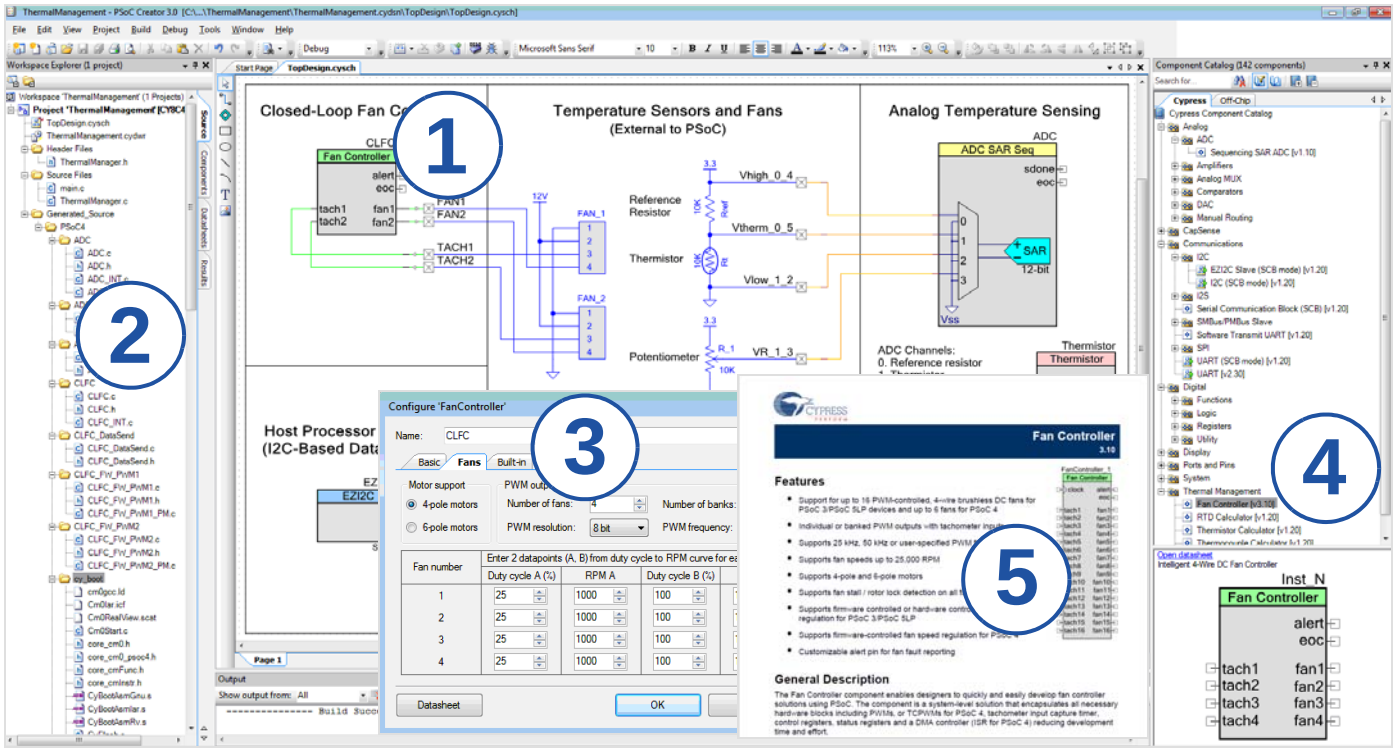
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 24MHz |
| Connectivity | I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART |
| Peripherals | Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT |
| Number of I/O | 54 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4127axi-s455 |

## PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

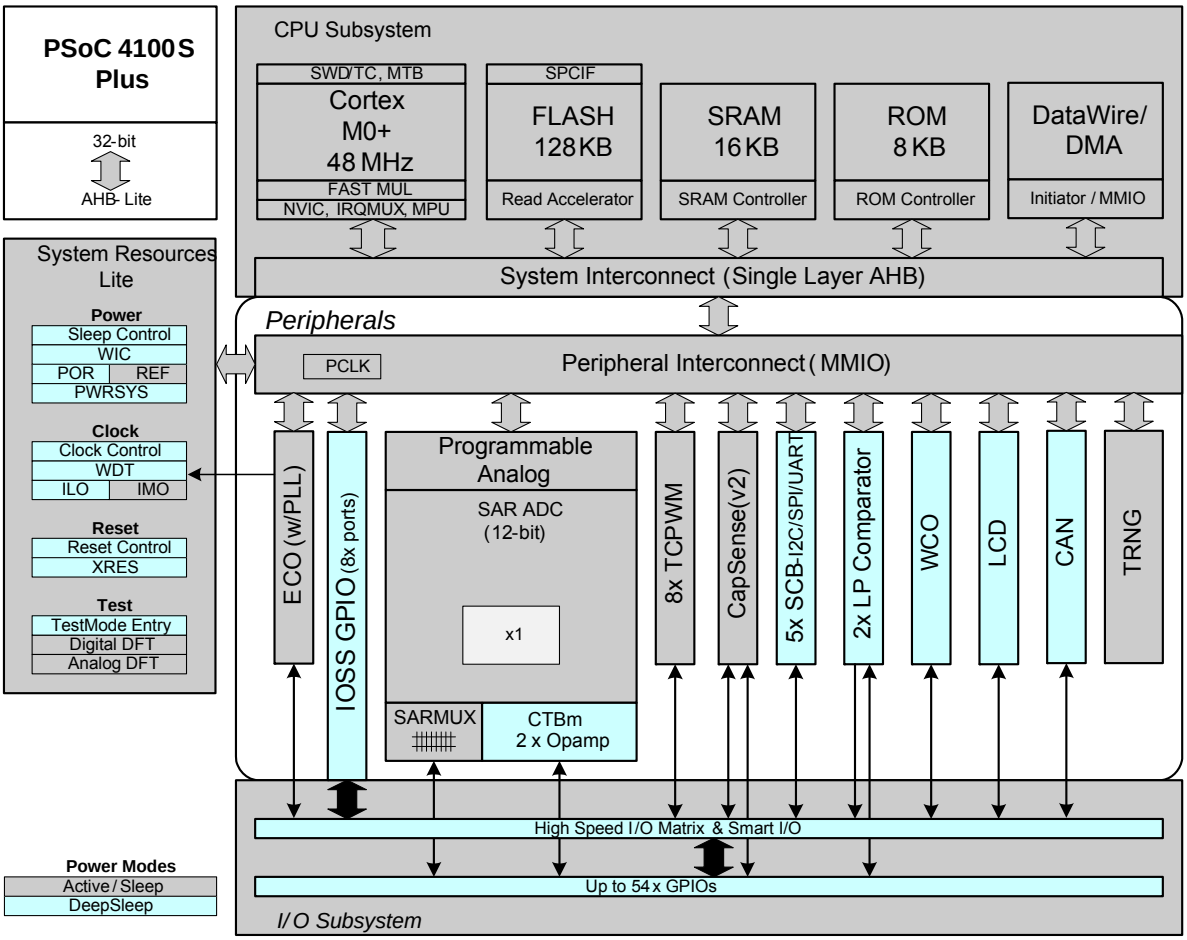
1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



## Contents

**Figure 2. Block Diagram**




PSoC 4100S Plus devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S Plus devices. The SWD interface is fully compatible with industry-standard third-party tools. PSoC 4100S Plus provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S Plus, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S Plus allows the customer to make.

*Watch Crystal Oscillator (WCO)*

The PSoC 4100S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

*External Crystal Oscillators (ECO)*

The PSoC 4100S Plus also implements a 4 to 33 MHz crystal oscillator.

*Watchdog Timer and Counters*

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable. The Watchdog counters can be used to implement a Real-Time clock using the 32-kHz WCO.

*Reset*

PSoC 4100S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

## Analog Blocks

*12-bit SAR ADC*

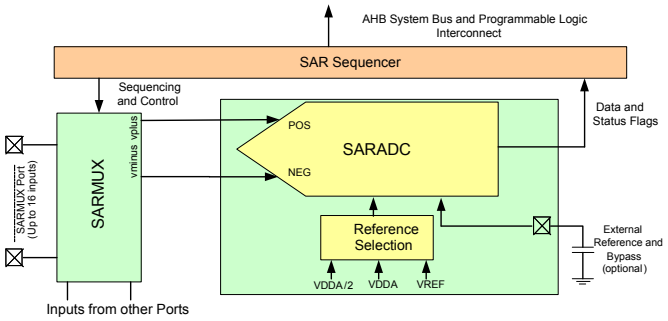
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

**Figure 4. SAR ADC**




*Two Opamps (Continuous-Time Block; CTB)*

PSoC 4100S Plus has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

*Low-power Comparators (LPC)*

PSoC 4100S Plus has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

*Current DACs*

PSoC 4100S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

*Analog Multiplexed Buses*

PSoC 4100S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

## Programmable Digital Blocks

*Smart I/O Block*

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

## Fixed Function Digital Blocks

*Timer/Counter/PWM (TCPWM) Block*

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. Each block also incorporates a Quadrature decoder. There are eight TCPWM blocks in PSoC 4100S Plus.

*Serial Communication Block (SCB)*

PSoC 4100S Plus has five serial communication blocks, which can be programmed to have SPI, $I^2C$, or UART functionality.

**$I^2C$ Mode**: The hardware $I^2C$ block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of PSoC 4100S Plus and effectively reduces $I^2C$ communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The $I^2C$ peripheral is compatible with the $I^2C$ Standard-mode and Fast-mode devices as defined in the NXP $I^2C$-bus specification and user manual (UM10204). The $I^2C$ bus I/O is implemented with GPIO in open-drain modes.

PSoC 4100S Plus is not completely compliant with the $I^2C$ spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the $I^2C$ system.

**UART Mode**: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

**SPI Mode**: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

*CAN*

There is a CAN 2.0B block with support for TT-CAN.

## GPIO

PSoC 4100S Plus has up to 54 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

## Pinouts

The following table provides the pin list for PSoC 4100S Plus for the 44-pin TQFP and 64-pin TQFP Normal and Fine Pitch packages.

| 64-TQFP | | 44-TQFP | |
|---|---|---|---|
| **Pin** | **Name** | **Pin** | **Name** |
| 39 | P0.0 | 24 | P0.0 |
| 40 | P0.1 | 25 | P0.1 |
| 41 | P0.2 | 26 | P0.2 |
| 42 | P0.3 | 27 | P0.3 |
| 43 | P0.4 | 28 | P0.4 |
| 44 | P0.5 | 29 | P0.5 |
| 45 | P0.6 | 30 | P0.6 |
| 46 | P0.7 | 31 | P0.7 |
| 47 | XRES | 32 | XRES |
| 48 | VCCD | 33 | VCCD |
| 49 | VSSD | | |
| 50 | VDDD | 34 | VDDD |
| 51 | P5.0 | | |
| 52 | P5.1 | | |
| 53 | P5.2 | | |
| 54 | P5.3 | | |
| 55 | P5.5 | | |
| 56 | VDDA | 35 | VDDA |
| 57 | VSSA | 36 | VSSA |
| 58 | P1.0 | 37 | P1.0 |
| 59 | P1.1 | 38 | P1.1 |
| 60 | P1.2 | 39 | P1.2 |
| 61 | P1.3 | 40 | P1.3 |
| 62 | P1.4 | 41 | P1.4 |
| 63 | P1.5 | 42 | P1.5 |
| 64 | P1.6 | 43 | P1.6 |
| 1 | P1.7 | 44 | P1.7 |
| | | 1 | VSSD |
| 2 | P2.0 | 2 | P2.0 |
| 3 | P2.1 | 3 | P2.1 |
| 4 | P2.2 | 4 | P2.2 |
| 5 | P2.3 | 5 | P2.3 |
| 6 | P2.4 | 6 | P2.4 |
| 7 | P2.5 | 7 | P2.5 |
| 8 | P2.6 | 8 | P2.6 |
| 9 | P2.7 | 9 | P2.7 |
| 10 | VSSD | 10 | P6.0 |
| 11 | No Connect (NC) | | |
| 12 | P6.0 | | |
| 13 | P6.1 | | |

### Alternate Pin Functions

Each Port pin has can be assigned to one of multiple functions; it can, for example, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

| Port/Pin | Analog | Smart I/O | ACT #0 | ACT #1 | ACT #3 | DS #2 | DS #3 |
|---|---|---|---|---|---|---|---|
| P0.0 | lpcomp.in_p[0] | | | tcpwm.tr_in[0] | scb[2].uart_cts:0 | scb[2].i2c_scl:0 | scb[0].spi_select1:0 |
| P0.1 | lpcomp.in_n[0] | | | tcpwm.tr_in[1] | scb[2].uart_rts:0 | scb[2].i2c_sda:0 | scb[0].spi_select2:0 |
| P0.2 | lpcomp.in_p[1] | | | | | | scb[0].spi_select3:0 |
| P0.3 | lpcomp.in_n[1] | | | | | | scb[2].spi_select0:1 |
| P0.4 | wco.wco_in | | | scb[1].uart_rx:0 | scb[2].uart_rx:0 | scb[1].i2c_scl:0 | scb[1].spi_mosi:1 |
| P0.5 | wco.wco_out | | | scb[1].uart_tx:0 | scb[2].uart_tx:0 | scb[1].i2c_sda:0 | scb[1].spi_miso:1 |
| P0.6 | exco.eco_in | | srss.ext_clk:0 | scb[1].uart_cts:0 | scb[2].uart_tx:1 | | scb[1].spi_clk:1 |
| P0.7 | exco.eco_out | | tcpwm.line[0]:3 | scb[1].uart_rts:0 | | | scb[1].spi_select0:1 |
| P5.0 | | | tcpwm.line[4]:2 | | scb[2].uart_rx:1 | scb[2].i2c_scl:1 | scb[2].spi_mosi:0 |
| P5.1 | | | tcpwm.line_compl[4]:2 | | scb[2].uart_tx:2 | scb[2].i2c_sda:1 | scb[2].spi_miso:0 |
| P5.2 | | | tcpwm.line[5]:2 | | scb[2].uart_cts:1 | lpcomp.comp[0]:2 | scb[2].spi_clk:0 |
| P5.3 | | | tcpwm.line_compl[5]:2 | | scb[2].uart_rts:1 | lpcomp.comp[1]:0 | scb[2].spi_select0:0 |
| P5.4 | | | tcpwm.line[6]:2 | | | | scb[2].spi_select1:0 |
| P5.5 | | | tcpwm.line_compl[6]:2 | | | | scb[2].spi_select2:0 |
| P1.0 | ctb0_oa0+ | SmartIo[2].io[0] | tcpwm.line[2]:1 | scb[0].uart_rx:1 | | scb[0].i2c_scl:0 | scb[0].spi_mosi:1 |
| P1.1 | ctb0_oa0- | SmartIo[2].io[1] | tcpwm.line_compl[2]:1 | scb[0].uart_tx:1 | | scb[0].i2c_sda:0 | scb[0].spi_miso:1 |
| P1.2 | ctb0_oa0_out | SmartIo[2].io[2] | tcpwm.line[3]:1 | scb[0].uart_cts:1 | tcpwm.tr_in[2] | scb[2].i2c_scl:2 | scb[0].spi_clk:1 |
| P1.3 | ctb0_oa1_out | SmartIo[2].io[3] | tcpwm.line_compl[3]:1 | scb[0].uart_rts:1 | tcpwm.tr_in[3] | scb[2].i2c_sda:2 | scb[0].spi_select0:1 |
| P1.4 | ctb0_oa1- | SmartIo[2].io[4] | tcpwm.line[6]:1 | | | scb[3].i2c_scl:0 | scb[0].spi_select1:1 |
| P1.5 | ctb0_oa1+ | SmartIo[2].io[5] | tcpwm.line_compl[6]:1 | | | scb[3].i2c_sda:0 | scb[0].spi_select2:1 |
| P1.6 | ctb0_oa0+ | SmartIo[2].io[6] | tcpwm.line[7]:1 | | | | scb[0].spi_select3:1 |
| P1.7 | ctb0_oa1+<br>sar_ext_vref0<br>sar_ext_vref1 | SmartIo[2].io[7] | tcpwm.line_compl[7]:1 | | | | scb[2].spi_clk:1 |
| P2.0 | sarmux[0] | SmartIo[0].io[0] | tcpwm.line[4]:0 | csd.comp | tcpwm.tr_in[4] | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | sarmux[1] | SmartIo[0].io[1] | tcpwm.line_compl[4]:0 | | tcpwm.tr_in[5] | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | sarmux[2] | SmartIo[0].io[2] | tcpwm.line[5]:1 | | | | scb[1].spi_clk:2 |
| P2.3 | sarmux[3] | SmartIo[0].io[3] | tcpwm.line_compl[5]:1 | | | | scb[1].spi_select0:2 |

## Analog Peripherals

*CTBm Opamp*

**Table 8. CTBm Opamp Specifications**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| | $I_{DD}$ | Opamp block current, External load | | | | | |
| SID269 | $I_{DD\_HI}$ | power=hi | – | 1100 | 1850 | µA | – |
| SID270 | $I_{DD\_MED}$ | power=med | – | 550 | 950 | | – |
| SID271 | $I_{DD\_LOW}$ | power=lo | – | 150 | 350 | | – |
| | $G_{BW}$ | Load = 20 pF, 0.1 mA<br>$V_{DDA}$ = 2.7 V | | | | | |
| SID272 | $G_{BW\_HI}$ | power=hi | 6 | – | – | MHz | Input and output are 0.2 V to $V_{DDA}$-0.2 V |
| SID273 | $G_{BW\_MED}$ | power=med | 3 | – | – | | Input and output are 0.2 V to $V_{DDA}$-0.2 V |
| SID274 | $G_{BW\_LO}$ | power=lo | – | 1 | – | | Input and output are 0.2 V to $V_{DDA}$-0.2 V |
| | $I_{OUT\_MAX}$ | $V_{DDA}$ = 2.7 V, 500 mV from rail | | | | | |
| SID275 | $I_{OUT\_MAX\_HI}$ | power=hi | 10 | – | – | mA | Output is 0.5 V to $V_{DDA}$ -0.5 V |
| SID276 | $I_{OUT\_MAX\_MID}$ | power=mid | 10 | – | – | | Output is 0.5 V to $V_{DDA}$ -0.5 V |
| SID277 | $I_{OUT\_MAX\_LO}$ | power=lo | – | 5 | – | | Output is 0.5 V to $V_{DDA}$ -0.5 V |
| | $I_{OUT}$ | $V_{DDA}$ = 1.71 V, 500 mV from rail | | | | | |
| SID278 | $I_{OUT\_MAX\_HI}$ | power=hi | 4 | – | – | mA | Output is 0.5 V to $V_{DDA}$ -0.5 V |
| SID279 | $I_{OUT\_MAX\_MID}$ | power=mid | 4 | – | – | | Output is 0.5 V to $V_{DDA}$-0.5 V |
| SID280 | $I_{OUT\_MAX\_LO}$ | power=lo | – | 2 | – | | Output is 0.5 V to $V_{DDA}$-0.5 V |
| | $I_{DD\_Int}$ | Opamp block current Internal Load | | | | | |
| SID269_I | $I_{DD\_HI\_Int}$ | power=hi | – | 1500 | 1700 | µA | – |
| SID270_I | $I_{DD\_MED\_Int}$ | power=med | – | 700 | 900 | | – |
| SID271_I | $I_{DD\_LOW\_Int}$ | power=lo | – | – | – | | – |
| | $G_{BW}$ | $V_{DDA}$ = 2.7 V | – | – | – | | – |
| SID272_I | $G_{BW\_HI\_Int}$ | power=hi | 8 | – | – | MHz | Output is 0.25 V to $V_{DDA}$-0.25 V |
| | | General opamp specs for both internal and external modes | | | | | |
| SID281 | $V_{IN}$ | Charge-pump on, $V_{DDA}$ = 2.7 V | –0.05 | – | $V_{DDA}$-0.2 | V | – |
| SID282 | $V_{CM}$ | Charge-pump on, $V_{DDA}$ = 2.7 V | –0.05 | – | $V_{DDA}$-0.2 | | – |
| | $V_{OUT}$ | $V_{DDA}$ = 2.7 V | | | | | |

**Table 8. CTBm Opamp Specifications** *(continued)*

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details/ Conditions |
|---|---|---|---|---|---|---|---|
| SID283 | $V_{OUT\_1}$ | power=hi, Iload=10 mA | 0.5 | – | $V_{DDA}$ -0.5 | V | – |
| SID284 | $V_{OUT\_2}$ | power=hi, Iload=1 mA | 0.2 | – | $V_{DDA}$ -0.2 | | – |
| SID285 | $V_{OUT\_3}$ | power=med, Iload=1 mA | 0.2 | – | $V_{DDA}$ -0.2 | | – |
| SID286 | $V_{OUT\_4}$ | power=lo, Iload=0.1 mA | 0.2 | – | $V_{DDA}$ -0.2 | | – |
| SID288 | $V_{OS\_TR}$ | Offset voltage, trimmed | –1.0 | ±0.5 | 1.0 | mV | High mode, input 0 V to $V_{DDA}$-0.2 V |
| SID288A | $V_{OS\_TR}$ | Offset voltage, trimmed | – | ±1 | – | | Medium mode, input 0 V to $V_{DDA}$-0.2 V |
| SID288B | $V_{OS\_TR}$ | Offset voltage, trimmed | – | ±2 | – | | Low mode, input 0 V to $V_{DDA}$-0.2 V |
| SID290 | $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | –10 | ±3 | 10 | µV/°C | High mode |
| SID290A | $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | – | ±10 | – | µV/°C | Medium mode |
| SID290B | $V_{OS\_DR\_TR}$ | Offset voltage drift, trimmed | – | ±10 | – | | Low mode |
| SID291 | CMRR | DC | 70 | 80 | – | dB | Input is 0 V to $V_{DDA}$-0.2 V, Output is 0.2 V to $V_{DDA}$-0.2 V |
| SID292 | PSRR | At 1 kHz, 10-mV ripple | 70 | 85 | – | | $V_{DDD}$ = 3.6 V, high-power mode, input is 0.2 V to $V_{DDA}$-0.2 V |
| | Noise | | | | | | |
| SID294 | VN2 | Input-referred, 1 kHz, power = Hi | – | 72 | – | nV/rtHz | Input and output are at 0.2 V to $V_{DDA}$-0.2 V |
| SID295 | VN3 | Input-referred, 10 kHz, power = Hi | – | 28 | – | | Input and output are at 0.2 V to $V_{DDA}$-0.2 V |
| SID296 | VN4 | Input-referred, 100 kHz, power = Hi | – | 15 | – | | Input and output are at 0.2 V to $V_{DDA}$-0.2 V |
| SID297 | $C_{LOAD}$ | Stable up to max. load. Performance specs at 50 pF. | – | – | 125 | pF | – |
| SID298 | SLEW_RATE | Cload = 50 pF, Power = High, $V_{DDA}$ = 2.7 V | 6 | – | – | V/µs | – |
| SID299 | T_OP_WAKE | From disable to enable, no external RC dominating | – | – | 25 | µs | – |
| SID299A | OL_GAIN | Open Loop Gain | – | 90 | – | dB | |
| | COMP_MODE | Comparator mode; 50 mV drive, $T_{rise}$=$T_{fall}$ (approx.) | | | | | |

*SPI*

**Table 18. SPI DC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID163 | ISPI1 | Block current consumption at 1 Mbps | – | – | 360 | µA | – |
| SID164 | ISPI2 | Block current consumption at 4 Mbps | – | – | 560 | | – |
| SID165 | ISPI3 | Block current consumption at 8 Mbps | – | – | 600 | | – |

**Table 19. SPI AC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID166 | FSPI | SPI Operating frequency (Master; 6X Oversampling) | – | – | 8 | MHz | |
| **Fixed SPI Master Mode AC Specifications** | | | | | | | |
| SID167 | TDMO | MOSI Valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | TDSI | MISO Valid before SClock capturing edge | 20 | – | – | | Full clock, late MISO sampling |
| SID169 | THMO | Previous MOSI data hold time | 0 | – | – | | Referred to Slave capturing edge |
| **Fixed SPI Slave Mode AC Specifications** | | | | | | | |
| SID170 | TDMI | MOSI Valid before Sclock Capturing edge | 40 | – | – | ns | – |
| SID171 | TDSO | MISO Valid after Sclock driving edge | – | – | 42 + 3*Tcpu | | $T_{CPU} = 1/F_{CPU}$ |
| SID171A | TDSO_EXT | MISO Valid after Sclock driving edge in Ext. Clk mode | – | – | 48 | | – |
| SID172 | THSO | Previous MISO data hold time | 0 | – | – | | – |
| SID172A | TSSELSSCK | SSEL Valid to first SCK Valid edge | – | – | 100 | ns | – |

*UART*

**Table 20. UART DC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID160 | $I_{UART1}$ | Block current consumption at 100 Kbps | – | – | 55 | µA | – |
| SID161 | $I_{UART2}$ | Block current consumption at 1000 Kbps | – | – | 312 | µA | – |

**Table 21. UART AC Specifications**[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID162 | $F_{UART}$ | Bit rate | – | – | 1 | Mbps | – |

**Note**
8. Guaranteed by characterization.

*SWD Interface*

**Table 28. SWD Interface Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID213 | F_SWDCLK1 | 3.3 V ≤ $V_{DD}$ ≤ 5.5 V | – | – | 14 | MHz | SWDCLK ≤ 1/3 CPU clock frequency |
| SID214 | F_SWDCLK2 | 1.71 V ≤ $V_{DD}$ ≤ 3.3 V | – | – | 7 | | SWDCLK ≤ 1/3 CPU clock frequency |
| SID215[12] | T_SWDI_SETUP | T = 1/f SWDCLK | 0.25*T | – | – | ns | – |
| SID216[12] | T_SWDI_HOLD | T = 1/f SWDCLK | 0.25*T | – | – | | – |
| SID217[12] | T_SWDO_VALID | T = 1/f SWDCLK | – | – | 0.5*T | | – |
| SID217A[12] | T_SWDO_HOLD | T = 1/f SWDCLK | 1 | – | – | | – |

*Internal Main Oscillator*

**Table 29. IMO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID218 | $I_{IMO1}$ | IMO operating current at 48 MHz | – | – | 250 | µA | – |
| SID219 | $I_{IMO2}$ | IMO operating current at 24 MHz | – | – | 180 | µA | – |

**Table 30. IMO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID223 | $F_{IMOTOL1}$ | Frequency variation at 24, 32, and 48 MHz (trimmed) | – | – | ±2 | % | |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 7 | µs | – |
| SID228 | $T_{JITRMSIMO2}$ | RMS jitter at 24 MHz | – | 145 | – | ps | – |

*Internal Low-Speed Oscillator*

**Table 31. ILO DC Specifications**

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID231 | $I_{ILO1}$ | ILO operating current | – | 0.3 | 1.05 | µA | – |

**Table 32. ILO AC Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID234[12] | $T_{STARTILO1}$ | ILO startup time | – | – | 2 | ms | – |
| SID236[12] | $T_{ILODUTY}$ | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | $F_{ILOTRIM1}$ | ILO frequency range | 20 | 40 | 80 | kHz | – |

**Note**
12. Guaranteed by design.

*Smart I/O*

**Table 38. Smart I/O Pass-through Time (Delay in Bypass Mode)**

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|---|---|---|---|---|---|---|---|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in bypass mode | – | – | 1.6 | ns | |

*CAN*

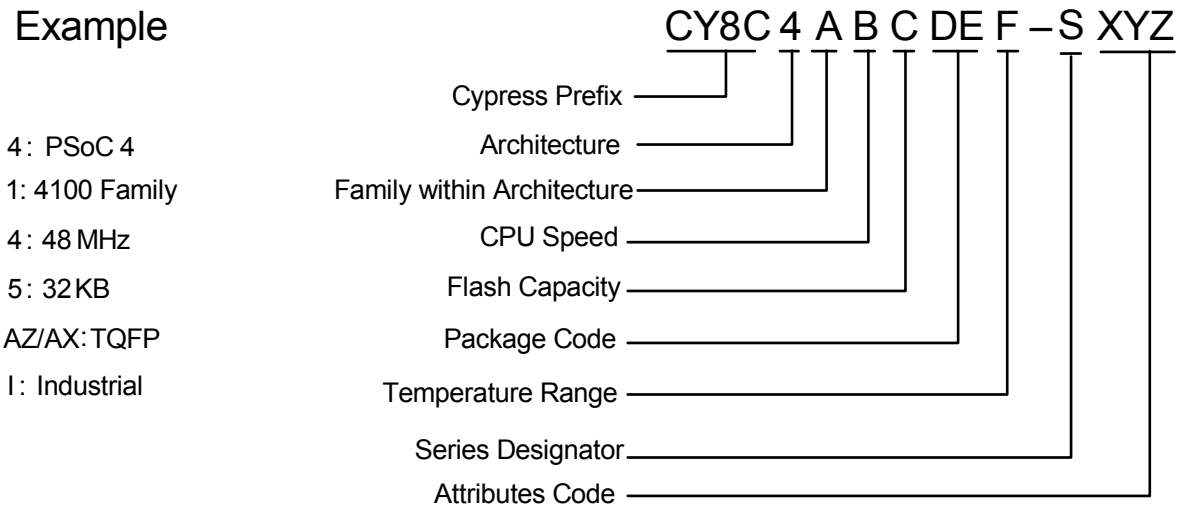
**Table 39. CAN Specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|---|---|---|---|---|---|---|
| SID420 | IDD_CAN | Block current consumption | – | – | 200 | µA | |
| SID421 | CAN_bits | CAN Bit rate | – | – | 1 | Mbps | Min 8-MHZ clock |

The nomenclature used in the preceding table is based on the following part numbering convention:

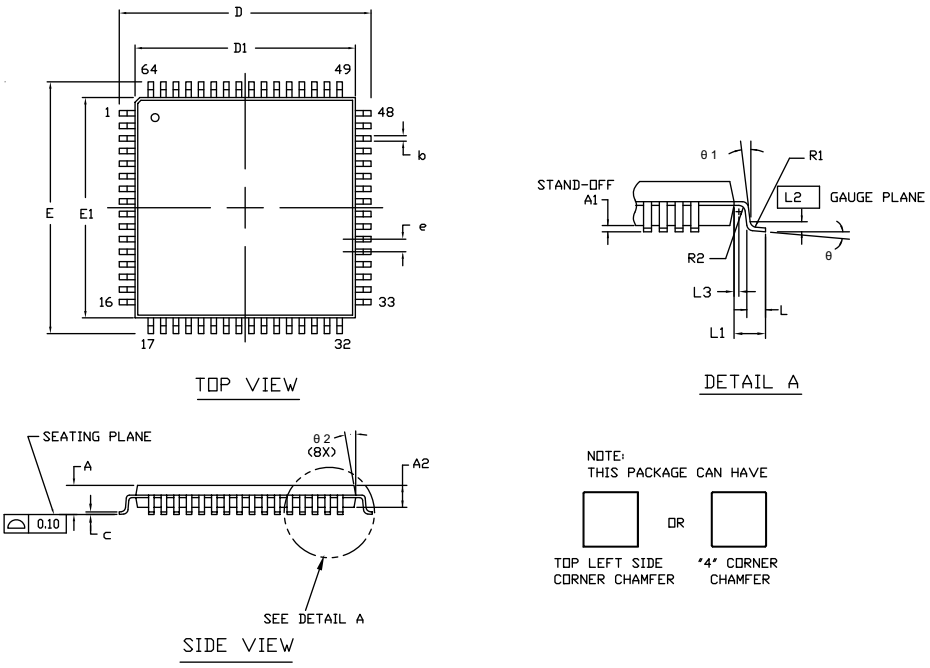
| Field | Description | Values | Meaning |
|---|---|---|---|
| CY8C | Cypress Prefix | | |
| 4 | Architecture | 4 | PSoC 4 |
| A | Family | 1 | 4100 Family |
| B | CPU Speed | 2 | 24 MHz |
| | | 4 | 48 MHz |
| C | Flash Capacity | 4 | 16 KB |
| | | 5 | 32 KB |
| | | 6 | 64 KB |
| | | 7 | 128 KB |
| DE | Package Code | AX | TQFP (0.8-mm pitch) |
| | | AZ | TQFP (0.5-mm pitch) |
| | | LQ | QFN |
| | | PV | SSOP |
| | | FN | CSP |
| F | Temperature Range | I | Industrial |
| S | Series Designator | S | PSoC 4 S-Series |
| | | M | PSoC 4 M-Series |
| | | L | PSoC 4 L-Series |
| | | BL | PSoC 4 BLE-Series |
| XYZ | Attributes Code | 000-999 | Code of feature set in the specific family |

The following is an example of a part number:



## Package Diagrams

**Figure 7. 64-pin TQFP Package (0.8-mm Pitch) Outline**




| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| D | 15.75 | 16.00 | 16.25 |
| D1 | 13.95 | 14.00 | 14.05 |
| E | 15.75 | 16.00 | 16.25 |
| E1 | 13.95 | 14.00 | 14.05 |
| R1 | 0.08 | — | 0.20 |
| R2 | 0.08 | — | 0.20 |
| θ | 0° | — | 7° |
| θ1 | 0° | — | — |
| θ2 | 11° | 12° | 13° |
| c | — | — | 0.20 |
| b | 0.30 | 0.35 | 0.40 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| L2 | 0.25 BSC | | |
| L3 | 0.20 | — | — |
| e | 0.80 TYP | | |

NOTE:
1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85046 *H

**Figure 8. 64-pin TQFP Package (0.5-mm Pitch) Outline**

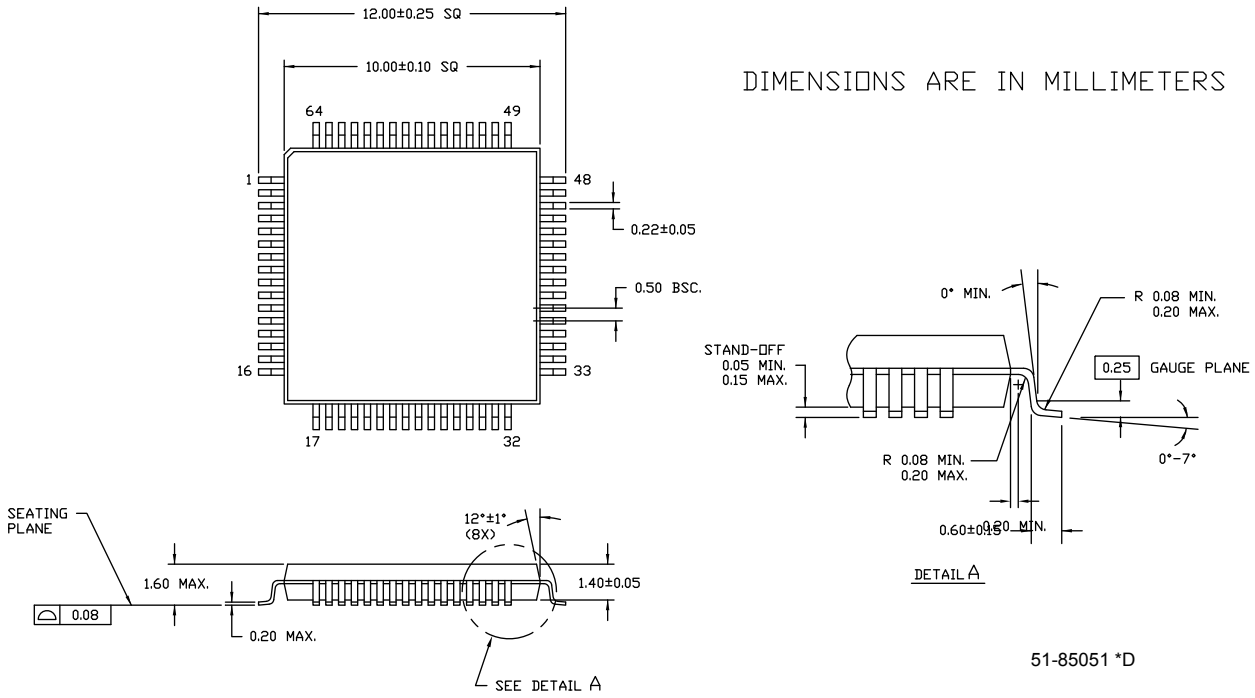
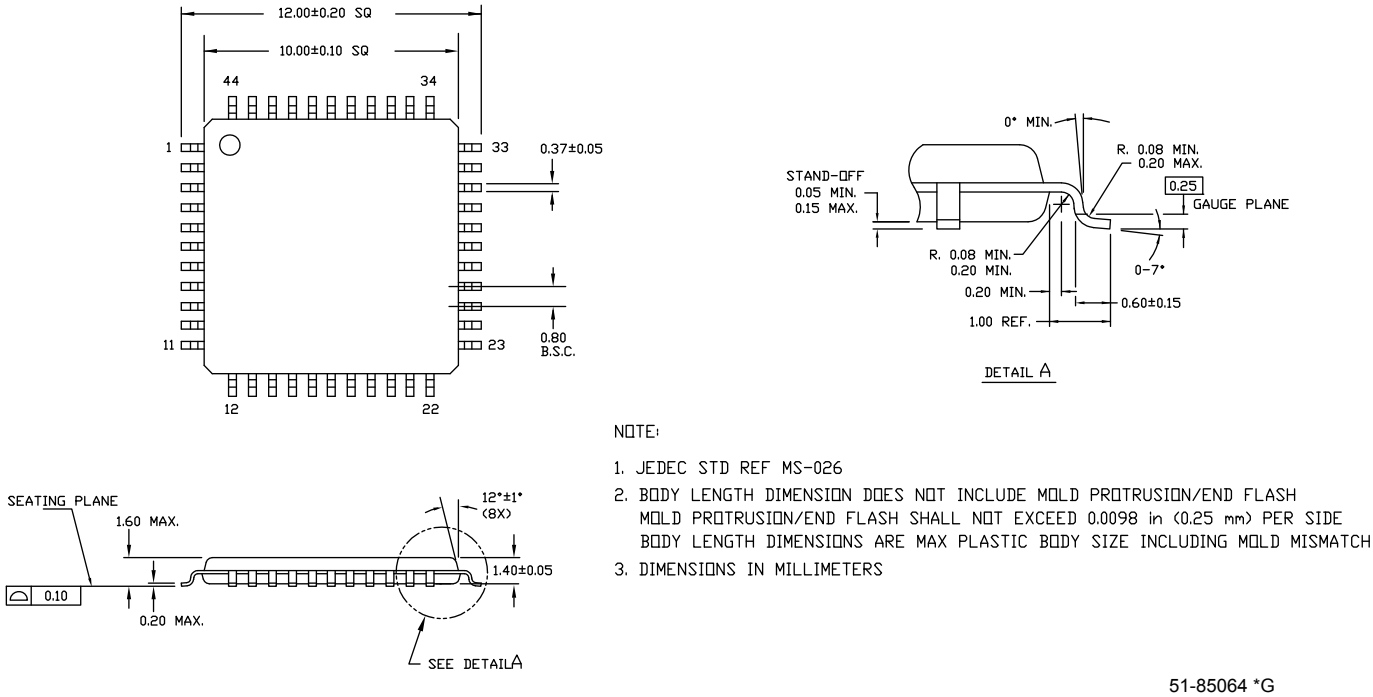



**Figure 9. 44-Pin TQFP Package Outline**




NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

## Acronyms

**Table 44. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | execution program status register |
| ESD | electrostatic discharge |

**Table 44. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| $I^2C$, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |

**Table 44. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration data sheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC® | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | $I^2C$ serial clock |
| SDA | $I^2C$ serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |

**Table 44. Acronyms Used in this Document** *(continued)*

| Acronym | Description |
|---|---|
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

## Document Conventions

### Units of Measure

**Table 45. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | megasamples per second |
| µA | microampere |
| µF | microfarad |
| µH | microhenry |
| µs | microsecond |
| µV | microvolt |
| µW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

## Revision History

| Description Title: PSoC® 4: PSoC 4100S Plus Datasheet Programmable System-on-Chip (PSoC)<br>Document Number: 002-19966 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *E | 5995731 | WKA | 12/15/2017 | New release |
| *F | 6069640 | JIAO | 02/13/2018 | Updated Pinouts and DC Specifications. |
| *G | 6169676 | WKA | 05/09/2018 | Updated Clock Diagram to show Watchdog details and clock divider information.<br>Removed preliminary statement in Pinouts. |

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