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What is "Embedded - Microcontrollers"?

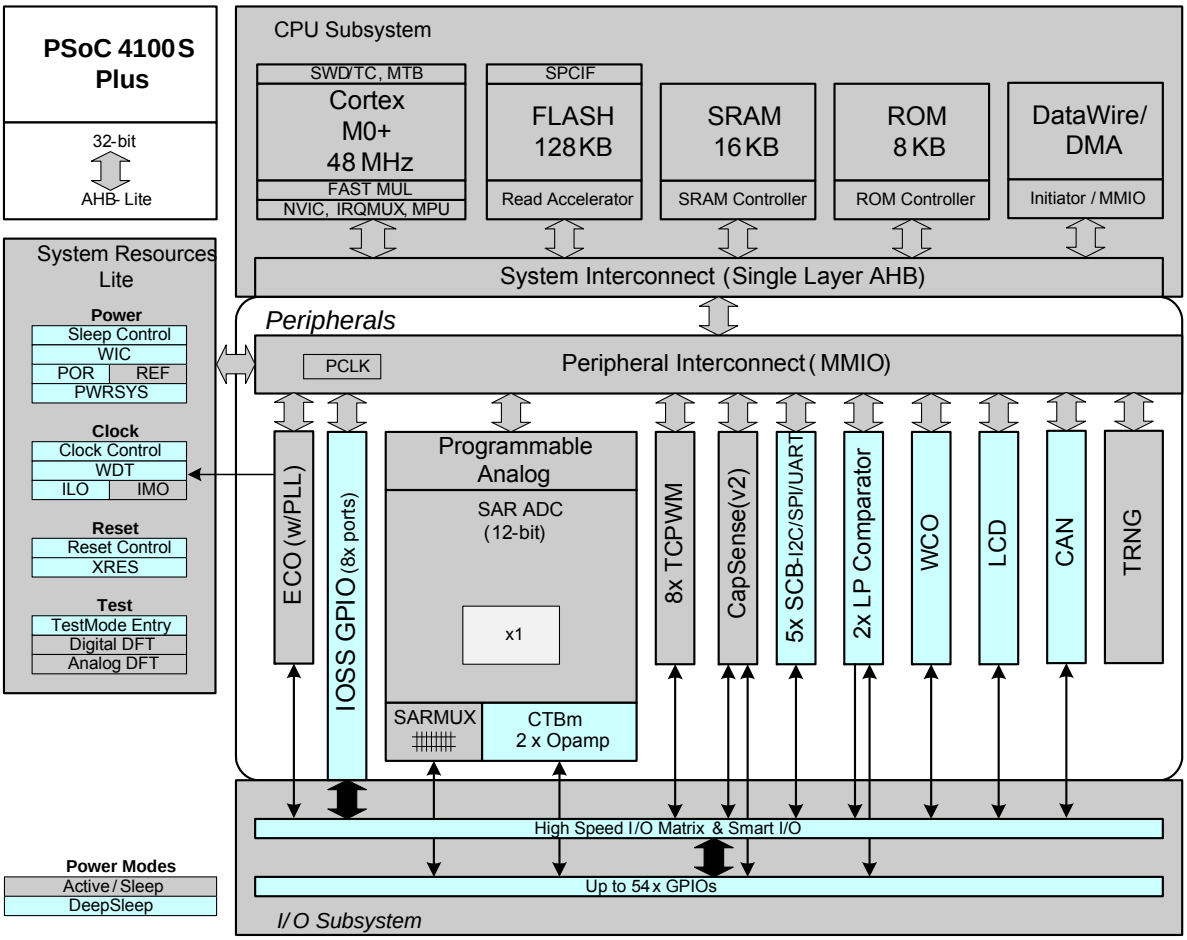
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4147axi-s455

Contents

Figure 2. Block Diagram



PSoC 4100S Plus devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S Plus devices. The SWD interface is fully compatible with industry-standard third-party tools. PSoC 4100S Plus provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S Plus, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S Plus allows the customer to make.

Watch Crystal Oscillator (WCO)

The PSoC 4100S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

External Crystal Oscillators (ECO)

The PSoC 4100S Plus also implements a 4 to 33 MHz crystal oscillator.

Watchdog Timer and Counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable. The Watchdog counters can be used to implement a Real-Time clock using the 32-kHz WCO.

Reset

PSoC 4100S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

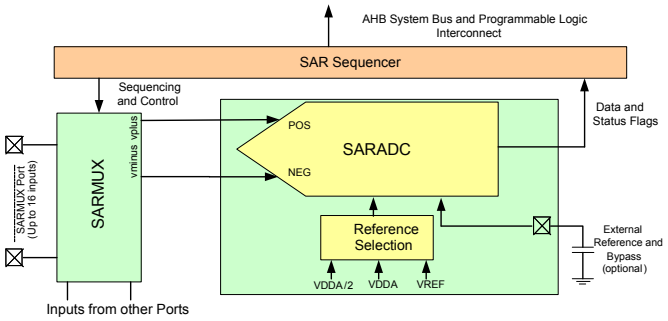
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

PSoC 4100S Plus has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

PSoC 4100S Plus has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

PSoC 4100S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

PSoC 4100S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Programmable Digital Blocks

Smart I/O Block

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital Blocks

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. Each block also incorporates a Quadrature decoder. There are eight TCPWM blocks in PSoC 4100S Plus.

Serial Communication Block (SCB)

PSoC 4100S Plus has five serial communication blocks, which can be programmed to have SPI, I^2C, or UART functionality.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of PSoC 4100S Plus and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

PSoC 4100S Plus is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

CAN

There is a CAN 2.0B block with support for TT-CAN.

GPIO

PSoC 4100S Plus has up to 54 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4100S Plus through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

PSoC 4100S Plus has an LCD controller, which can drive up to 4 commons and up to 50 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; one 32-bit register per port).

64-TQFP		44-TQFP	
Pin	**Name**	**Pin**	**Name**
14	P6.2		
15	P6.4		
16	P6.5		
17	VSSD		
17	VSSD		
18	P3.0	11	P3.0
19	P3.1	12	P3.1
20	P3.2	13	P3.2
21	P3.3	14	P3.3
22	P3.4	15	P3.4
23	P3.5	16	P3.5
24	P3.6	17	P3.6
25	P3.7	18	P3.7
26	VDDD	19	VDDD
27	P4.0	20	P4.0
28	P4.1	21	P4.1
29	P4.2	22	P4.2
30	P4.3	23	P4.3
31	P4.4		
32	P4.5		
33	P4.6		
34	P4.7		
35	P5.6		
36	P5.7		
37	P7.0		
38	P7.1		

Descriptions of the Power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

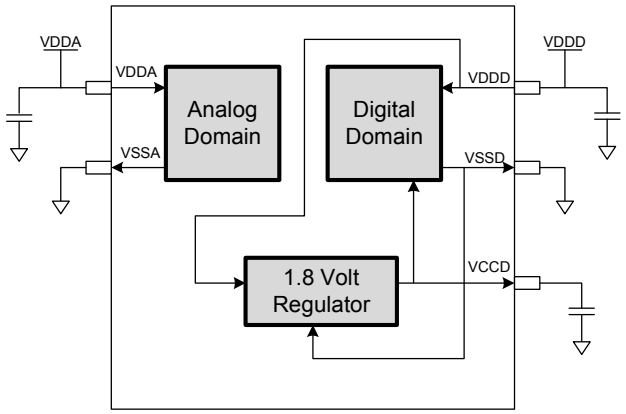
GPIOs by package:

	64 TQFP	44 TQFP
Number	54	37

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S Plus. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 5. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, PSoC 4100S Plus is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4100S Plus supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

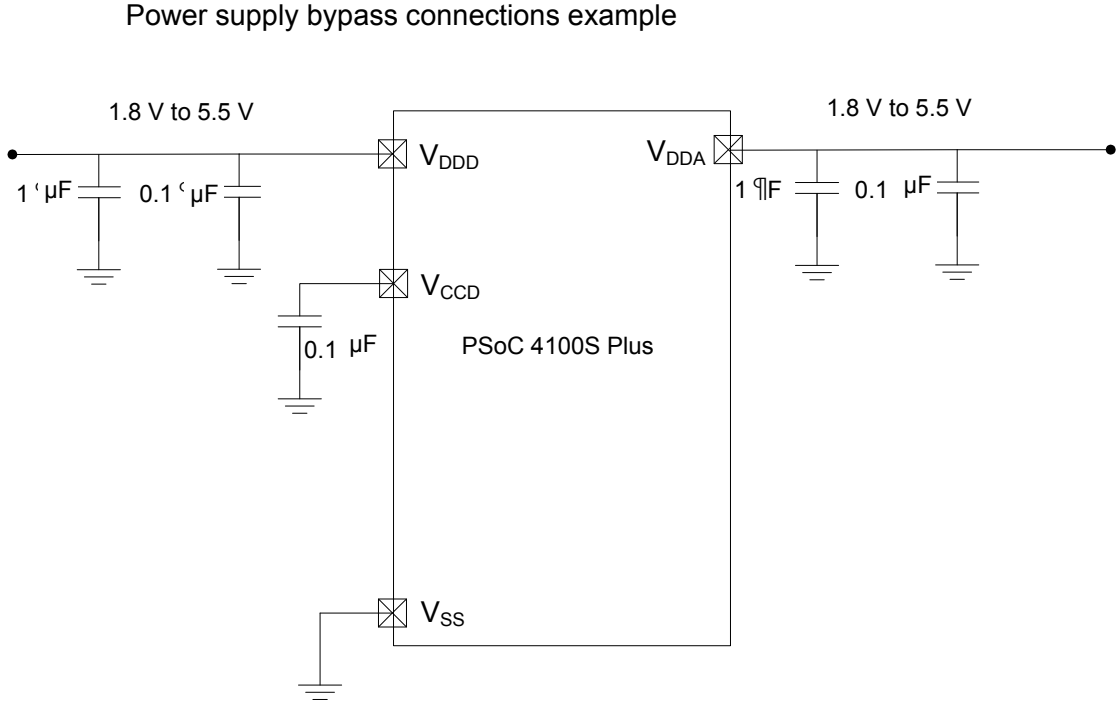
Mode 2: 1.8 V ±5% External Supply

In this mode, PSoC 4100S Plus is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 6. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active



Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95		–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5		–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DDD} = V_{DDA})	1.71	–	1.89		Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		X5R ceramic or better
Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25 °C.							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.4	mA	Max is at 85 °C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	4.6		Max is at 85 °C and 5.5 V
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	7.1		Max is at 85 °C and 5.5 V

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 2. DC Specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	I_{DD17}	I^2C wakeup WDT, and Comparators on	–	1.1	1.8	mA	6 MHZ. Max is at 85 °C and 5.5 V
SID25	I_{DD20}	I^2C wakeup, WDT, and Comparators on	–	1.5	2.1		12 MHZ. Max is at 85 °C and 5.5 V
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	I_{DD23}	I^2C wakeup, WDT, and Comparators on	–	1.1	1.8	mA	6 MHZ. Max is at 85 °C and 1.89 V
SID28A	I_{DD23A}	I^2C wakeup, WDT, and Comparators on	–	1.5	2.1	mA	12 MHZ. Max is at 85 °C and 1.89 V
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID30	I_{DD25}	I^2C wakeup and WDT on; T = –40 °C to 60 °C	–	2.5	40	µA	T = –40 °C to 60 °C
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	125	µA	Max is at 3.6 V and 85 °C
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID33	I_{DD28}	I^2C wakeup and WDT on; T = –40 °C to 60 °C	–	2.5	40	µA	T = –40 °C to 60 °C
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	125	µA	Max is at 5.5 V and 85 °C
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID36	I_{DD31}	I^2C wakeup and WDT on; T = –40 °C to 60 °C	–	2.5	60	µA	T = –40 °C to 60 °C
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	180	µA	Max is at 1.89 V and 85 °C
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49[2]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	
SID50[2]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		

Note
2. Guaranteed by characterization.

Analog Peripherals

CTBm Opamp

Table 8. CTBm Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I_{DD}	Opamp block current, External load					
SID269	I_{DD_HI}	power=hi	–	1100	1850	µA	–
SID270	I_{DD_MED}	power=med	–	550	950		–
SID271	I_{DD_LOW}	power=lo	–	150	350		–
	G_{BW}	Load = 20 pF, 0.1 mA V_{DDA} = 2.7 V					
SID272	G_{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V_{DDA}-0.2 V
SID273	G_{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V_{DDA}-0.2 V
SID274	G_{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V_{DDA}-0.2 V
	I_{OUT_MAX}	V_{DDA} = 2.7 V, 500 mV from rail					
SID275	$I_{OUT\_MAX\_HI}$	power=hi	10	–	–	mA	Output is 0.5 V to V_{DDA} -0.5 V
SID276	$I_{OUT\_MAX\_MID}$	power=mid	10	–	–		Output is 0.5 V to V_{DDA} -0.5 V
SID277	$I_{OUT\_MAX\_LO}$	power=lo	–	5	–		Output is 0.5 V to V_{DDA} -0.5 V
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail					
SID278	$I_{OUT\_MAX\_HI}$	power=hi	4	–	–	mA	Output is 0.5 V to V_{DDA} -0.5 V
SID279	$I_{OUT\_MAX\_MID}$	power=mid	4	–	–		Output is 0.5 V to V_{DDA}-0.5 V
SID280	$I_{OUT\_MAX\_LO}$	power=lo	–	2	–		Output is 0.5 V to V_{DDA}-0.5 V
	I_{DD_Int}	Opamp block current Internal Load					
SID269_I	$I_{DD\_HI\_Int}$	power=hi	–	1500	1700	µA	–
SID270_I	$I_{DD\_MED\_Int}$	power=med	–	700	900		–
SID271_I	$I_{DD\_LOW\_Int}$	power=lo	–	–	–		–
	G_{BW}	V_{DDA} = 2.7 V	–	–	–		–
SID272_I	$G_{BW\_HI\_Int}$	power=hi	8	–	–	MHz	Output is 0.25 V to V_{DDA}-0.25 V
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA}-0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD}-0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD}-1.15		V_{DDD} ≥ 2.2 V at –40 °C
SID88	C_{MRR}	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7V
SID88A	C_{MRR}	Common mode rejection ratio	42	–	–		V_{DDD} ≤ 2.7V
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	
SID248	I_{CMP2}	Block current, low power mode	–	–	100		
SID259	I_{CMP3}	Block current in ultra low-power mode	–	–	6		V_{DDD} ≥ 2.2 V at –40 °C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	

Table 10. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	V_{DDD} ≥ 2.2 V at –40 °C

Note
6. Guaranteed by characterization.

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSENSACC	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SAR ADC DC Specifications							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msps	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A_samp/2	kHz	
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1.7	–	2	LSB	V_{REF} = 1 to V_{DD}
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 to V_{DD}
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 to V_{DD}
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1	_	2.2	LSB	V_{REF} = 1 to V_{DD}
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6, 1 Msps	–1	_	2	LSB	V_{REF} = 1.71 to V_{DD}
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1	_	2.2	LSB	V_{REF} = 1 to V_{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
SID261	FSARINTREF	SAR operating speed without external reference bypass	_	_	100	ksps	12-bit resolution

CSD and IDAC

Table 13. CSD and IDAC Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75V (with ripple), 25 °C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External Voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} –0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ
SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	µA	LSB = 37.5-nA typ

SPI

Table 18. SPI DC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 19. SPI AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	
Fixed SPI Master Mode AC Specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave Mode AC Specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + 3*Tcpu		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

UART

Table 20. UART DC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 21. UART AC Specifications[8]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Note
8. Guaranteed by characterization.

LCD Direct Drive

Table 22. LCD Direct Drive DC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	–	2	–	mA	32 × 4 segments at 50 Hz 25 °C
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	–	2	–		32 × 4 segments at 50 Hz 25 °C

Table 23. LCD Direct Drive AC Specifications[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note
9. Guaranteed by characterization.

Watch Crystal Oscillator (WCO)

Table 33. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	µW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	

External Clock

Table 34. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306[13]	ExtClkDuty	Duty cycle; measured at $V_{DD/2}$	45	–	55	%	–

External Crystal Oscillator and PLL

Table 35. External Crystal Oscillator (ECO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID316[13]	IECO1	External clock input frequency	–	–	1.5	mA	–
SID317[13]	FECO	Crystal frequency range	4	–	33	MHz	–

Table 36. PLL Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	–	530	610	uA	
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	–	300	405	uA	
SID412	Fpllin	PLL input frequency	1	–	48	MHz	
SID413	Fpllint	PLL intermediate frequency; prescaler out	1	–	3	MHz	
SID414	Fpllvco	VCO output frequency before post-divide	22.5	–	104	MHz	
SID415	Divvco	VCO Output post-divider range; PLL output frequency is Fpplvco/Divvco	1	–	8		
SID416	Plllocktime	Lock time at startup	–	–	250	µs	
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	–	–	150	ps	Guaranteed by design
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	–	–	200	ps	Guaranteed by design

System Clock

Table 37. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262[13]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

Note
13. Guaranteed by characterization.

Ordering Information

The marketing part numbers for the PSoC 4100S Plus devices are listed in the following table.

Category	MPN	Features															Packages		
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Op-amp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	SAR ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	ECO	CAN Controller	Smart I/Os	GPIO	44-TQFP (0.8-mm pitch)	64-TQFP (0.5-mm pitch)	64-TQFP (0.8-mm pitch)
4126	CY8C4126AXI-S443	24	64	8	2	0	1	1	806 ksps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4126AZI-S445	24	64	8	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4126AXI-S445	24	64	8	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4126AZI-S455	24	64	8	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4126AXI-S455	24	64	8	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
4146	CY8C4146AXI-S443	48	64	8	2	0	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4146AZI-S445	48	64	8	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4146AXI-S445	48	64	8	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4146AXI-S453	48	64	8	2	1	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4146AZI-S455	48	64	8	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4146AXI-S455	48	64	8	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
4127	CY8C4127AXI-S443	24	128	16	2	0	1	1	806 ksps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4127AZI-S445	24	128	16	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4127AXI-S445	24	128	16	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4127AXI-S453	24	128	16	2	1	1	1	806 ksps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4127AZI-S455	24	128	16	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4127AXI-S455	24	128	16	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
4147	CY8C4147AXI-S443	48	128	16	2	0	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4147AZI-S445	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4147AXI-S445	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4147AXI-S453	48	128	16	2	1	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4147AZI-S455	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4147AXI-S455	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4147AZI-S465	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	1	24	54	–	✔	–
	CY8C4147AXI-S465	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	1	24	54	–	–	✔
	CY8C4147AZI-S475	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	1	24	54	–	✔	–
	CY8C4147AXI-S475	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	1	24	54	–	–	✔

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8-mm pitch)
		AZ	TQFP (0.5-mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Series Designator	S	PSoC 4 S-Series
		M	PSoC 4 M-Series
		L	PSoC 4 L-Series
		BL	PSoC 4 BLE-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

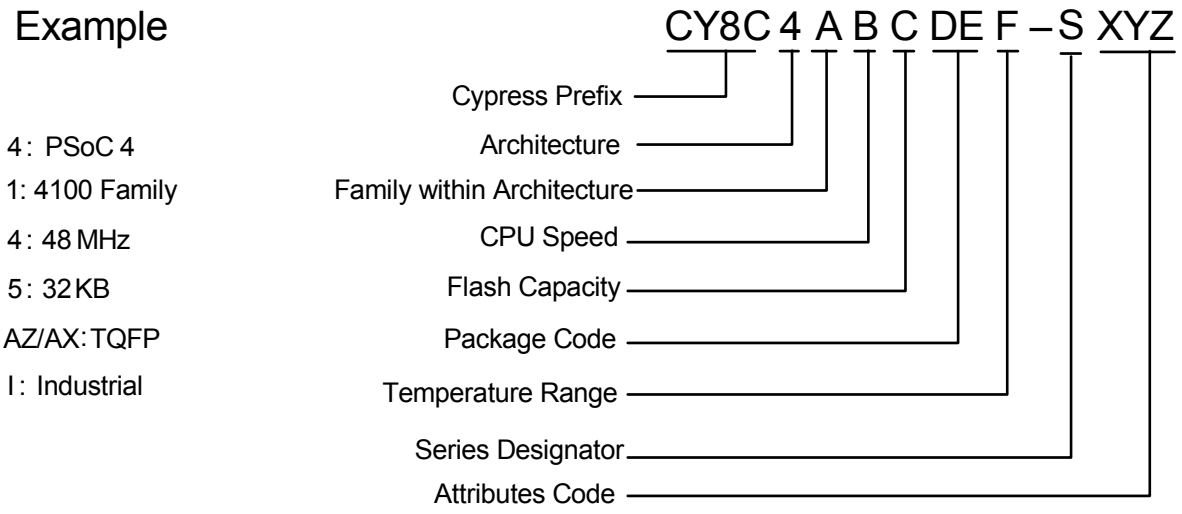


Figure 8. 64-pin TQFP Package (0.5-mm Pitch) Outline

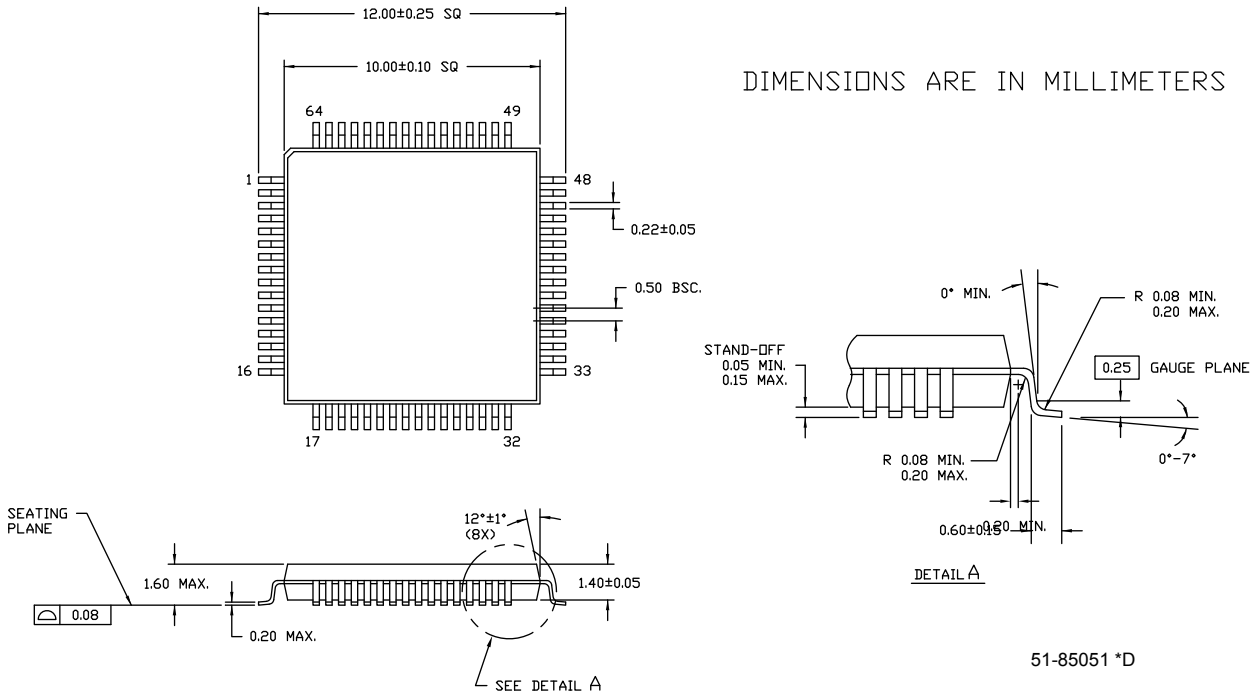
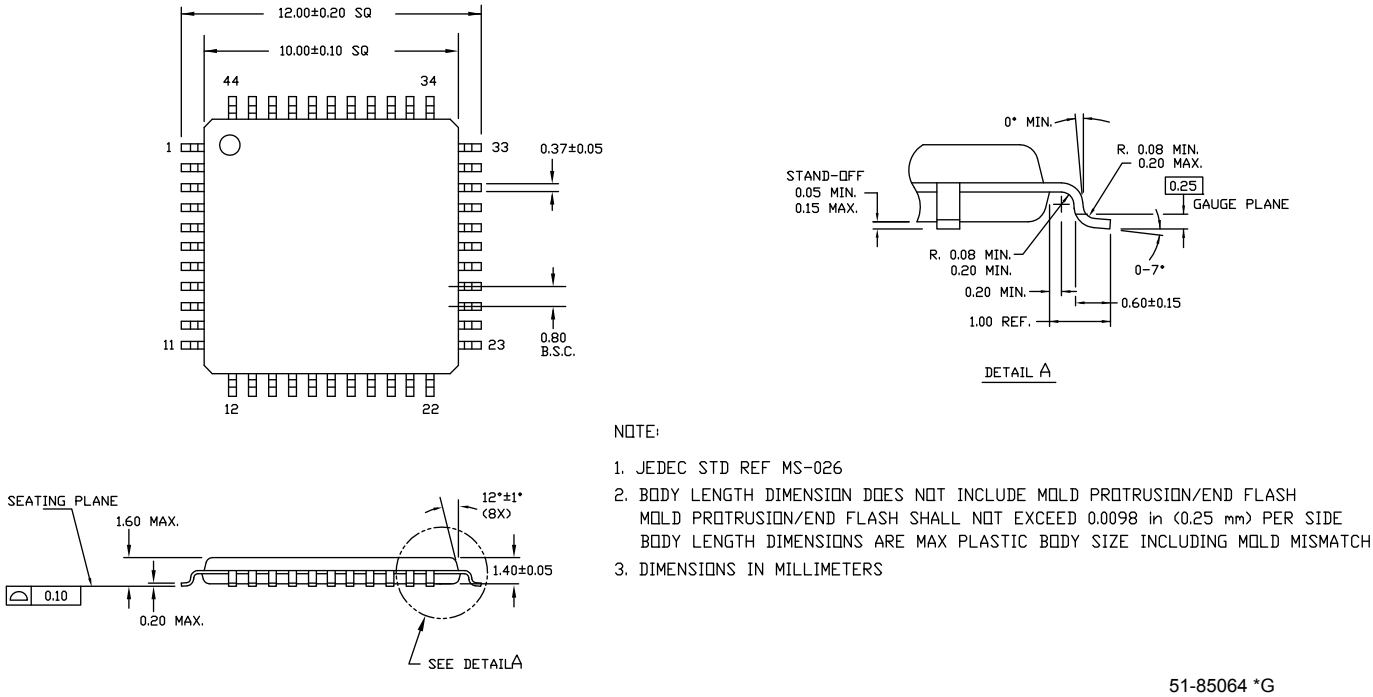


Figure 9. 44-Pin TQFP Package Outline



NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Acronyms

Table 44. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD