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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

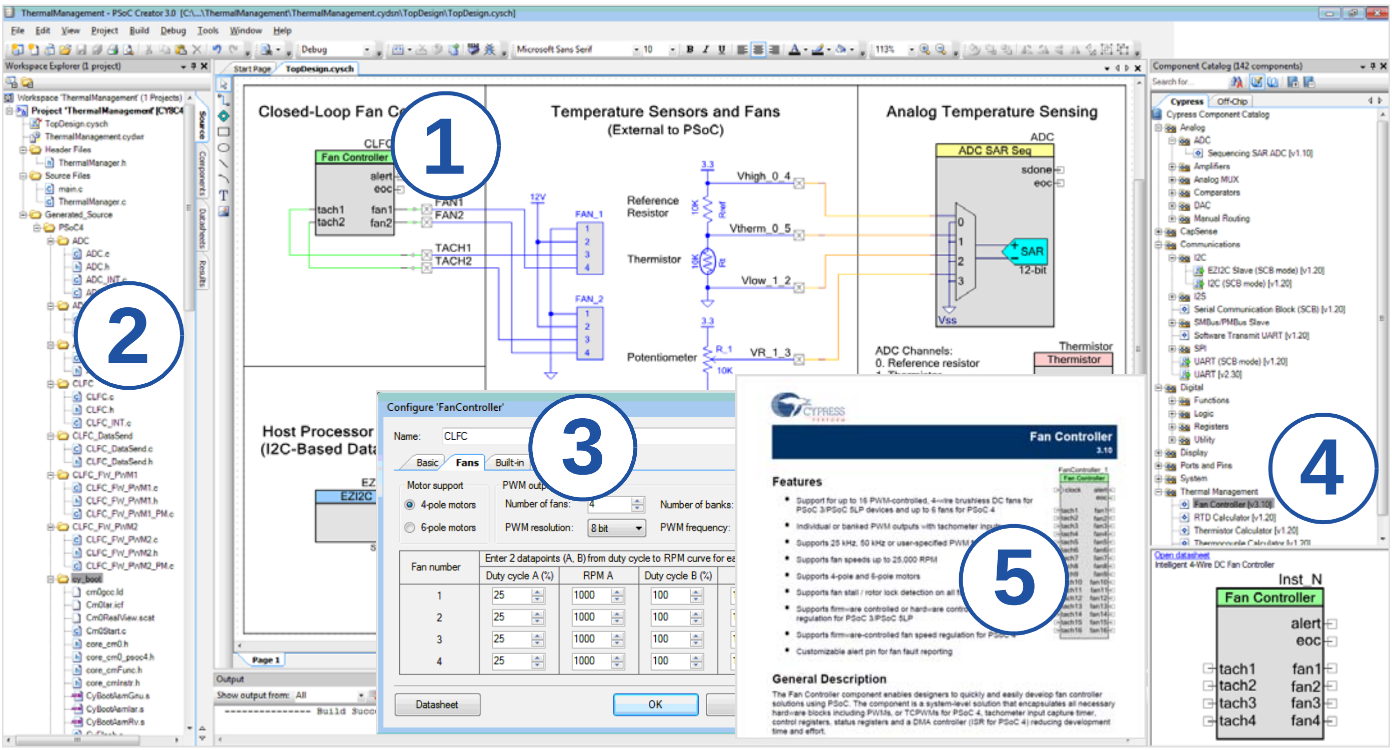
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4147axi-s465

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



Contents

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S Plus is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU subsystem includes an 8-channel DMA engine and also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S Plus has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S Plus device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

16 KB of SRAM are provided with zero wait-state access at 48 MHz.

SROM

An 8-KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section Power. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). PSoC 4100S Plus operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSoC 4100S Plus provides Active, Sleep, and Deep Sleep low-power modes.

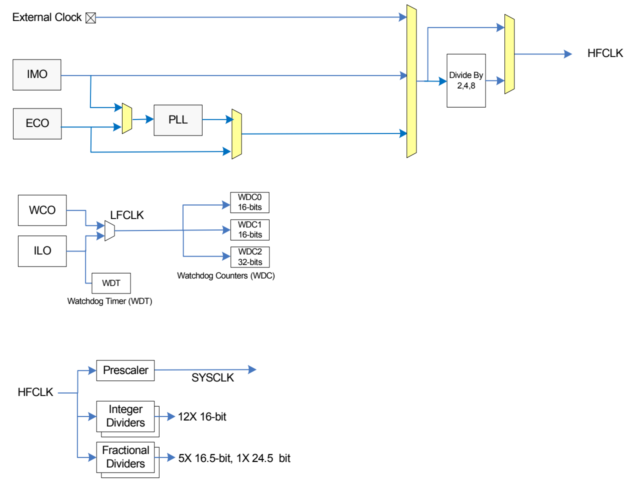
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

Clock System

The PSoC 4100S Plus clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S Plus consists of the IMO, ILO, a 32-kHz Watch Crystal Oscillator (WCO), MHz ECO and PLL, and provision for an external clock. The WCO block allows locking the IMO to the 32-kHz oscillator.

Figure 3. PSoC 4100S Plus MCU Clocking Architecture



The HFCLK signal can be divided down as shown to generate synchronous clocks for the Analog and Digital peripherals. There are 18 clock dividers for the PSoC 4100S Plus (six with fractional divide capability, twelve with integer divide only). The twelve 16-bit integer divide capability allows a lot of flexibility in generating fine-grained frequency. In addition, there are five 16-bit fractional dividers and one 24-bit fractional divider.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S Plus. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2% over the entire voltage and temperature range.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watch Crystal Oscillator (WCO)

The PSoC 4100S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

External Crystal Oscillators (ECO)

The PSoC 4100S Plus also implements a 4 to 33 MHz crystal oscillator.

Watchdog Timer and Counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable. The Watchdog counters can be used to implement a Real-Time clock using the 32-kHz WCO.

Reset

PSoC 4100S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

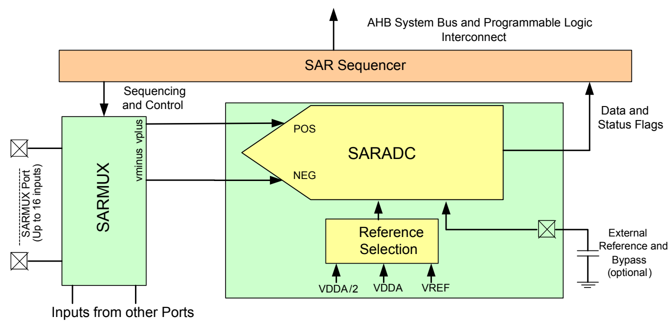
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

PSoC 4100S Plus has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

PSoC 4100S Plus has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

PSoC 4100S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

PSoC 4100S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Pinouts

The following table provides the pin list for PSoC 4100S Plus for the 44-pin TQFP and 64-pin TQFP Normal and Fine Pitch packages.

64-TQFP		44-TQFP	
Pin	Name	Pin	Name
39	P0.0	24	P0.0
40	P0.1	25	P0.1
41	P0.2	26	P0.2
42	P0.3	27	P0.3
43	P0.4	28	P0.4
44	P0.5	29	P0.5
45	P0.6	30	P0.6
46	P0.7	31	P0.7
47	XRES	32	XRES
48	VCCD	33	VCCD
49	VSSD		
50	VDDD	34	VDDD
51	P5.0		
52	P5.1		
53	P5.2		
54	P5.3		
55	P5.5		
56	VDDA	35	VDDA
57	VSSA	36	VSSA
58	P1.0	37	P1.0
59	P1.1	38	P1.1
60	P1.2	39	P1.2
61	P1.3	40	P1.3
62	P1.4	41	P1.4
63	P1.5	42	P1.5
64	P1.6	43	P1.6
1	P1.7	44	P1.7
		1	VSSD
2	P2.0	2	P2.0
3	P2.1	3	P2.1
4	P2.2	4	P2.2
5	P2.3	5	P2.3
6	P2.4	6	P2.4
7	P2.5	7	P2.5
8	P2.6	8	P2.6
9	P2.7	9	P2.7
10	VSSD	10	P6.0
11	No Connect (NC)		
12	P6.0		
13	P6.1		

64-TQFP		44-TQFP	
Pin	**Name**	**Pin**	**Name**
14	P6.2		
15	P6.4		
16	P6.5		
17	VSSD		
17	VSSD		
18	P3.0	11	P3.0
19	P3.1	12	P3.1
20	P3.2	13	P3.2
21	P3.3	14	P3.3
22	P3.4	15	P3.4
23	P3.5	16	P3.5
24	P3.6	17	P3.6
25	P3.7	18	P3.7
26	VDDD	19	VDDD
27	P4.0	20	P4.0
28	P4.1	21	P4.1
29	P4.2	22	P4.2
30	P4.3	23	P4.3
31	P4.4		
32	P4.5		
33	P4.6		
34	P4.7		
35	P5.6		
36	P5.7		
37	P7.0		
38	P7.1		

Descriptions of the Power pins are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip

GPIOs by package:

	64 TQFP	44 TQFP
Number	54	37

Alternate Pin Functions

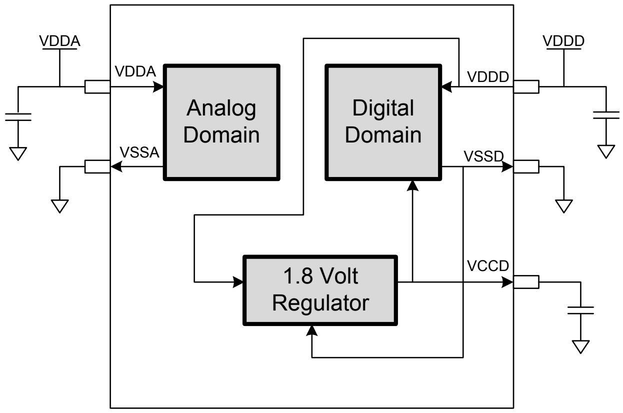
Each Port pin has can be assigned to one of multiple functions; it can, for example, be an analog I/O, a digital peripheral function, an LCD pin, or a CapSense pin. The pin assignments are shown in the following table.

Port/Pin	Analog	Smart I/O	ACT #0	ACT #1	ACT #3	DS #2	DS #3
P0.0	lpcomp.in_p[0]			tcpwm.tr_in[0]	scb[2].uart_cts:0	scb[2].i2c_scl:0	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]			tcpwm.tr_in[1]	scb[2].uart_rts:0	scb[2].i2c_sda:0	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]						scb[2].spi_select0:1
P0.4	wco.wco_in			scb[1].uart_rx:0	scb[2].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco.wco_out			scb[1].uart_tx:0	scb[2].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6	exco.eco_in		srss.ext_clk:0	scb[1].uart_cts:0	scb[2].uart_tx:1		scb[1].spi_clk:1
P0.7	exco.eco_out		tcpwm.line[0]:3	scb[1].uart_rts:0			scb[1].spi_select0:1
P5.0			tcpwm.line[4]:2		scb[2].uart_rx:1	scb[2].i2c_scl:1	scb[2].spi_mosi:0
P5.1			tcpwm.line_compl[4]:2		scb[2].uart_tx:2	scb[2].i2c_sda:1	scb[2].spi_miso:0
P5.2			tcpwm.line[5]:2		scb[2].uart_cts:1	lpcomp.comp[0]:2	scb[2].spi_clk:0
P5.3			tcpwm.line_compl[5]:2		scb[2].uart_rts:1	lpcomp.comp[1]:0	scb[2].spi_select0:0
P5.4			tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5			tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P1.0	ctb0_oa0+	SmartIo[2].io[0]	tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0_oa0-	SmartIo[2].io[1]	tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0_oa0_out	SmartIo[2].io[2]	tcpwm.line[3]:1	scb[0].uart_cts:1	tcpwm.tr_in[2]	scb[2].i2c_scl:2	scb[0].spi_clk:1
P1.3	ctb0_oa1_out	SmartIo[2].io[3]	tcpwm.line_compl[3]:1	scb[0].uart_rts:1	tcpwm.tr_in[3]	scb[2].i2c_sda:2	scb[0].spi_select0:1
P1.4	ctb0_oa1-	SmartIo[2].io[4]	tcpwm.line[6]:1			scb[3].i2c_scl:0	scb[0].spi_select1:1
P1.5	ctb0_oa1+	SmartIo[2].io[5]	tcpwm.line_compl[6]:1			scb[3].i2c_sda:0	scb[0].spi_select2:1
P1.6	ctb0_oa0+	SmartIo[2].io[6]	tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1	SmartIo[2].io[7]	tcpwm.line_compl[7]:1				scb[2].spi_clk:1
P2.0	sarmux[0]	SmartIo[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	SmartIo[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux[2]	SmartIo[0].io[2]	tcpwm.line[5]:1				scb[1].spi_clk:2
P2.3	sarmux[3]	SmartIo[0].io[3]	tcpwm.line_compl[5]:1				scb[1].spi_select0:2

Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC 4100S Plus. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

Figure 5. Power Supply Connections



There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

Mode 1: 1.8 V to 5.5 V External Supply

In this mode, PSoC 4100S Plus is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4100S Plus supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

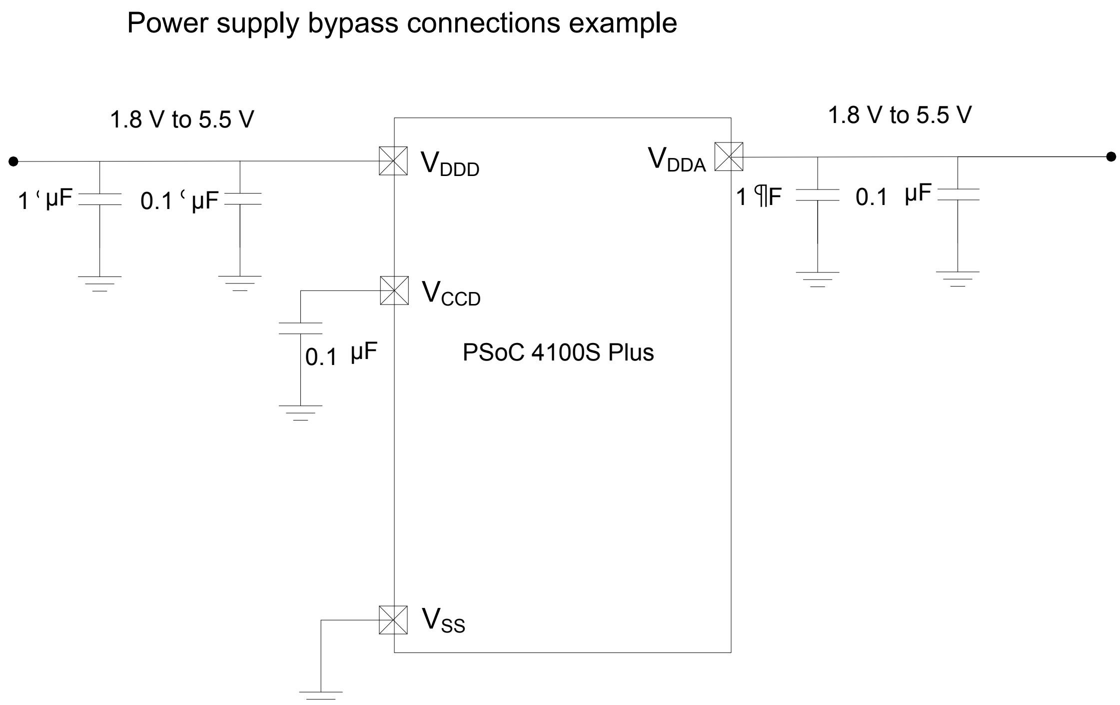
Mode 2: 1.8 V ±5% External Supply

In this mode, PSoC 4100S Plus is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

Figure 6. External Supply Range from 1.8 V to 5.5 V with Internal Regulator Active



Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95	V	–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD}+0.5	V	–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO\_injection}$	GPIO injection current, Max for V_{IH} > V_{DDD}, and Min for V_{IL} < V_{SS}	–0.5	–	0.5	mA	Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DDD} = V_{DDA})	1.71	–	1.89	V	Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at VDD = 3.3 V and 25 °C.							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.4	mA	Max is at 85 °C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	4.6	mA	Max is at 85 °C and 5.5 V
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	7.1	mA	Max is at 85 °C and 5.5 V

Note
1. Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID283	V_{OUT_1}	power=hi, Iload=10 mA	0.5	–	V_{DDA} -0.5	V	–
SID284	V_{OUT_2}	power=hi, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID285	V_{OUT_3}	power=med, Iload=1 mA	0.2	–	V_{DDA} -0.2		–
SID286	V_{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V_{DDA} -0.2		–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V_{DDA}-0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V_{DDA}-0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V_{DDA}-0.2 V
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA}-0.2 V, Output is 0.2 V to V_{DDA}-0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA}-0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	72	–	nV/rtHz	Input and output are at 0.2 V to V_{DDA}-0.2 V
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	28	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	15	–		Input and output are at 0.2 V to V_{DDA}-0.2 V
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, T_{rise}=T_{fall} (approx.)					

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to V_{DDA}-0.2 V
SID301	TPD2	Response time; power=med	–	500	–	ns	Input is 0.2 V to V_{DDA}-0.2 V
SID302	TPD3	Response time; power=lo	–	2500	–	ns	Input is 0.2 V to V_{DDA}-0.2 V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	700	–	µA	25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	200	–	µA	25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	$G_{BW\_HI\_M1}$	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_8	$G_{BW\_MED\_M1}$	Mode 1, Medium current	–	2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_9	$G_{BW\_LOW\_M1}$	Mode 1, Low current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_10	$G_{BW\_HI\_M2}$	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_11	$G_{BW\_MED\_M2}$	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_12	$G_{BW\_Low\_M2}$	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-0.2 V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_15	$V_{OS\_LOW\_M2}$	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-0.2 V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-0.2 V

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–		Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–		
SID_DS_23	$I_{OU\_MED\_M2}$	Mode 2, Medium current	–	1	–		
SID_DS_24	$I_{OU\_LOW\_M2}$	Mode 2, Low current	–	0.5	–		

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD}-0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD}-1.15		V_{DDD} ≥ 2.2 V at –40 °C
SID88	C_{MRR}	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7V
SID88A	C_{MRR}	Common mode rejection ratio	42	–	–		V_{DDD} ≤ 2.7V
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	
SID248	I_{CMP2}	Block current, low power mode	–	–	100		
SID259	I_{CMP3}	Block current in ultra low-power mode	–	–	6		V_{DDD} ≥ 2.2 V at –40 °C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	

Table 10. Comparator AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	V_{DDD} ≥ 2.2 V at –40 °C

Note
6. Guaranteed by characterization.

Table 13. CSD and IDAC Specifications *(continued)*

SPEC ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	5	µs	Full-scale transition. No external load
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	5	µs	Full-scale transition. No external load
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap

10-bit CapSense ADC

Table 14. 10-bit CapSense ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	
SIDA98	A_GAINERR	Gain error	–	–	±3	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	±18	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA100	A_ISAR	Current consumption	–	–	0.25	mA	
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.

Table 14. 10-bit CapSense ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V_{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 15. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[7]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

I^2C

Table 16. Fixed I^2C DC Specifications[7]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	1	–		

Table 17. Fixed I^2C AC Specifications[7]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Msps	–

Note
7. Guaranteed by characterization.

Memory

Table 24. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 25. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	$T_{ROWERASE}$[10]	Row erase time	–	–	16		–
SID176	$T_{ROWPROGRAM}$[10]	Row program time after erase	–	–	4		–
SID178	$T_{BULKERASE}$[10]	Bulk erase time (64 KB)	–	–	35		–
SID180[11]	$T_{DEVPROG}$[10]	Total device program time	–	–	7	Seconds	–
SID181[11]	F_{END}	Flash endurance	100 K	–	–	Cycles	–
SID182[11]	F_{RET}	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A[11]	–	Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 26. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185[11]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[11]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

Table 27. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190[11]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[11]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.
11. Guaranteed by characterization.

SWD Interface

Table 28. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215[12]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216[12]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID217[12]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	–
SID217A[12]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

Internal Main Oscillator

Table 29. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 30. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 31. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 32. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234[12]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[12]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

Note

12. Guaranteed by design.

Ordering Information

The marketing part numbers for the PSoC 4100S Plus devices are listed in the following table.

Category	MPN	Features															Packages		
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Op-amp (CTBm)	CSD	10-bit CSD ADC	12-bit SAR ADC	SAR ADC Sample Rate	LP Comparators	TCPWM Blocks	SCB Blocks	ECO	CAN Controller	Smart I/Os	GPIO	44-TQFP (0.8-mm pitch)	64-TQFP (0.5-mm pitch)	64-TQFP (0.8-mm pitch)
4126	CY8C4126AXI-S443	24	64	8	2	0	1	1	806 ksps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4126AZI-S445	24	64	8	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4126AXI-S445	24	64	8	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4126AZI-S455	24	64	8	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4126AXI-S455	24	64	8	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
4146	CY8C4146AXI-S443	48	64	8	2	0	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4146AZI-S445	48	64	8	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4146AXI-S445	48	64	8	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4146AXI-S453	48	64	8	2	1	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4146AZI-S455	48	64	8	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4146AXI-S455	48	64	8	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
4127	CY8C4127AXI-S443	24	128	16	2	0	1	1	806 ksps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4127AZI-S445	24	128	16	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4127AXI-S445	24	128	16	2	0	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4127AXI-S453	24	128	16	2	1	1	1	806 ksps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4127AZI-S455	24	128	16	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4127AXI-S455	24	128	16	2	1	1	1	806 ksps	2	8	5	✔	0	24	54	–	–	✔
4147	CY8C4147AXI-S443	48	128	16	2	0	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4147AZI-S445	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4147AXI-S445	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4147AXI-S453	48	128	16	2	1	1	1	1 Msps	2	8	4	✔	0	24	36	✔	–	–
	CY8C4147AZI-S455	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	✔	–
	CY8C4147AXI-S455	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	0	24	54	–	–	✔
	CY8C4147AZI-S465	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	1	24	54	–	✔	–
	CY8C4147AXI-S465	48	128	16	2	0	1	1	1 Msps	2	8	5	✔	1	24	54	–	–	✔
	CY8C4147AZI-S475	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	1	24	54	–	✔	–
	CY8C4147AXI-S475	48	128	16	2	1	1	1	1 Msps	2	8	5	✔	1	24	54	–	–	✔

Acronyms

Table 44. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

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