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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4147azi-s445

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

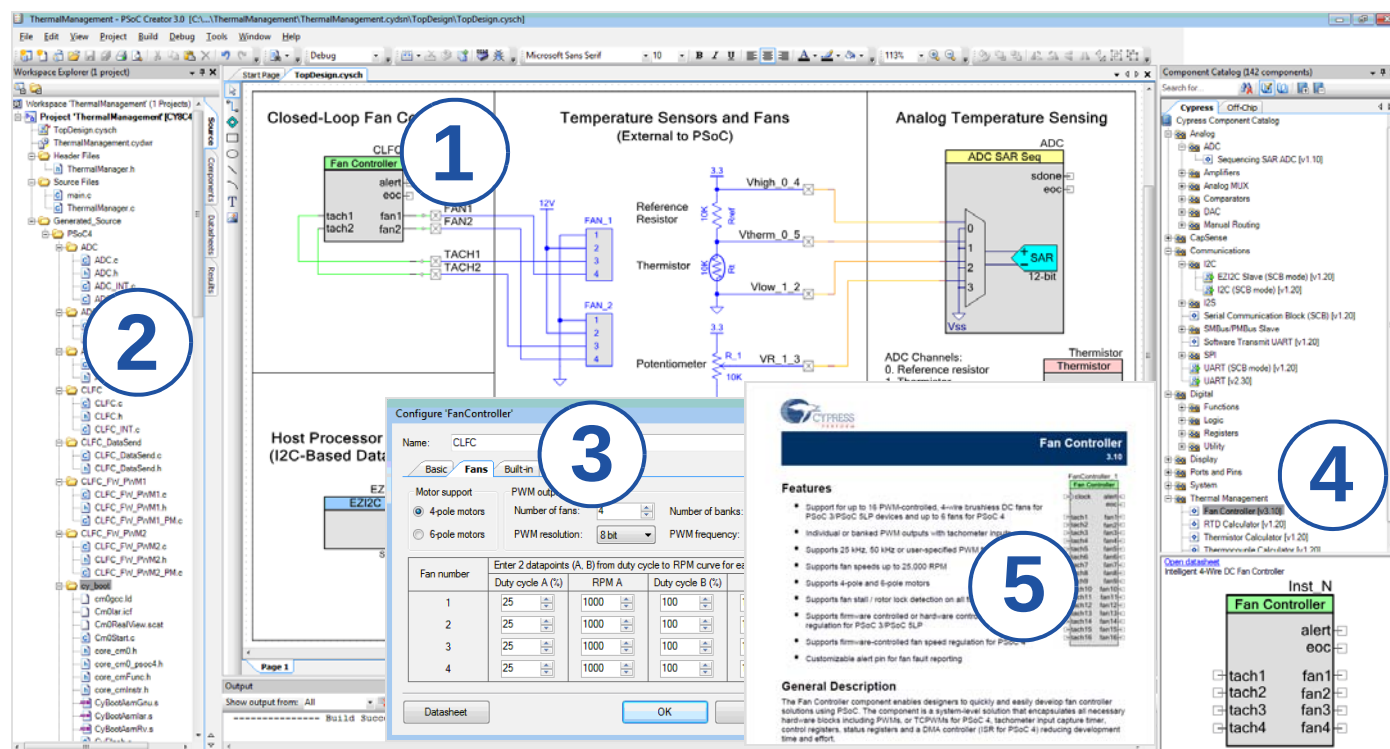
- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): Arm Cortex Code Optimization
 - [AN85951](#): PSoC® 4 and PSoC Analog Coprocessor CapSense® Design Guide
- Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
 - [CY8CKIT-041-41XX](#) PSoC 4100S CapSense Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
 - [CY8CKIT-149](#) PSoC® 4100S Plus Prototyping Kit enables you to evaluate and develop with Cypress' fourth-generation, low-power CapSense solution using the PSoC 4100S Plus devices.
- The [MiniProg3](#) device provides an interface for flash programming and debug.
- [Software User Guide](#):
 - A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.
- Component Datasheets:
 - The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.
- Online:
 - In addition to print documentation, the [Cypress PSoC forums](#) connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator



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Watch Crystal Oscillator (WCO)

The PSoC 4100S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

External Crystal Oscillators (ECO)

The PSoC 4100S Plus also implements a 4 to 33 MHz crystal oscillator.

Watchdog Timer and Counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable. The Watchdog counters can be used to implement a Real-Time clock using the 32-kHz WCO.

Reset

PSoC 4100S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

Analog Blocks

12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

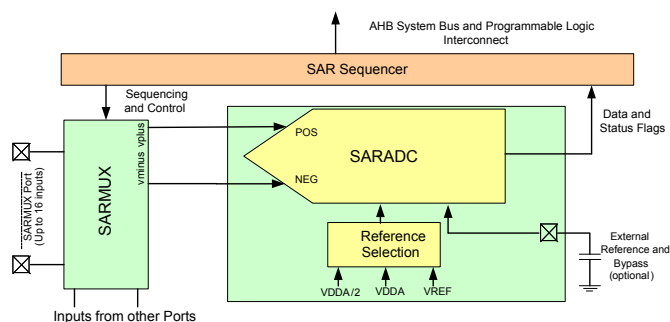
The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range

values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

Figure 4. SAR ADC



Two Opamps (Continuous-Time Block; CTB)

PSoC 4100S Plus has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, Voltage Buffers, Filters, Trans-Impedance Amplifiers, and other functions can be realized, in some cases with external passives, saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering.

Low-power Comparators (LPC)

PSoC 4100S Plus has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

Current DACs

PSoC 4100S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

Analog Multiplexed Buses

PSoC 4100S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4100S Plus through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

PSoC 4100S Plus has an LCD controller, which can drive up to 4 commons and up to 50 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; one 32-bit register per port).

Pinouts

The following table provides the pin list for PSoC 4100S Plus for the 44-pin TQFP and 64-pin TQFP Normal and Fine Pitch packages.

64-TQFP		44-TQFP	
Pin	Name	Pin	Name
39	P0.0	24	P0.0
40	P0.1	25	P0.1
41	P0.2	26	P0.2
42	P0.3	27	P0.3
43	P0.4	28	P0.4
44	P0.5	29	P0.5
45	P0.6	30	P0.6
46	P0.7	31	P0.7
47	XRES	32	XRES
48	VCCD	33	VCCD
49	VSSD		
50	VDDD	34	VDDD
51	P5.0		
52	P5.1		
53	P5.2		
54	P5.3		
55	P5.5		
56	VDDA	35	VDDA
57	VSSA	36	VSSA
58	P1.0	37	P1.0
59	P1.1	38	P1.1
60	P1.2	39	P1.2
61	P1.3	40	P1.3
62	P1.4	41	P1.4
63	P1.5	42	P1.5
64	P1.6	43	P1.6
1	P1.7	44	P1.7
		1	VSSD
2	P2.0	2	P2.0
3	P2.1	3	P2.1
4	P2.2	4	P2.2
5	P2.3	5	P2.3
6	P2.4	6	P2.4
7	P2.5	7	P2.5
8	P2.6	8	P2.6
9	P2.7	9	P2.7
10	VSSD	10	P6.0
11	No Connect (NC)		
12	P6.0		
13	P6.1		

Port/Pin	Analog	Smart I/O	ACT #0	ACT #1	ACT #3	DS #2	DS #3
P2.4	sarmux[4]	Smartlo[0].io[4]	tcpwm.line[0]:1	scb[3].uart_rx:1			scb[1].spi_select1:1
P2.5	sarmux[5]	Smartlo[0].io[5]	tcpwm.line_compl[0]:1	scb[3].uart_tx:1			scb[1].spi_select2:1
P2.6	sarmux[6]	Smartlo[0].io[6]	tcpwm.line[1]:1	scb[3].uart_cts:1			scb[1].spi_select3:1
P2.7	sarmux[7]	Smartlo[0].io[7]	tcpwm.line_compl[1]:1	scb[3].uart_rts:1		lpcomp.comp[0]:0	scb[2].spi_mosi:1
P6.0			tcpwm.line[4]:1	scb[3].uart_rx:0	can.can_tx_enb_n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:0
P6.1			tcpwm.line_compl[4]:1	scb[3].uart_tx:0	can.can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:0
P6.2			tcpwm.line[5]:0	scb[3].uart_cts:0	can.can_tx:0		scb[3].spi_clk:0
P6.3			tcpwm.line_compl[5]:0	scb[3].uart_rts:0			scb[3].spi_select0:0
P6.4			tcpwm.line[6]:0			scb[4].i2c_scl	scb[3].spi_select1:0
P6.5			tcpwm.line_compl[6]:0			scb[4].i2c_sda	scb[3].spi_select2:0
P3.0		Smartlo[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		Smartlo[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		Smartlo[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		Smartlo[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		Smartlo[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		Smartlo[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		Smartlo[1].io[6]	tcpwm.line[3]:0			scb[4].spi_select3	scb[1].spi_select3:0
P3.7		Smartlo[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso:1
P4.0	csd.vref_ext			scb[0].uart_rx:0	can.can_rx:1	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshield			scb[0].uart_tx:0	can.can_tx:1	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmod			scb[0].uart_cts:0	can.can_tx_enb_n:1	lpcomp.comp[0]:1	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:2	scb[0].spi_select0:0
P4.4				scb[4].uart_rx		scb[4].spi_mosi	scb[0].spi_select1:2
P4.5				scb[4].uart_tx		scb[4].spi_miso	scb[0].spi_select2:2
P4.6				scb[4].uart_cts		scb[4].spi_clk	scb[0].spi_select3:2
P4.7				scb[4].uart_rts		scb[4].spi_select0	
P5.6			tcpwm.line[7]:0			scb[4].spi_select1	scb[2].spi_select3:0
P5.7			tcpwm.line_compl[7]:0			scb[4].spi_select2	
P7.0			tcpwm.line[0]:2	scb[3].uart_rx:2		scb[3].i2c_scl:2	scb[3].spi_mosi:1
P7.1			tcpwm.line_compl[0]:2	scb[3].uart_tx:2		scb[3].i2c_sda:2	scb[3].spi_miso:1
P7.2			tcpwm.line[1]:2	scb[3].uart_cts:2			scb[3].spi_clk:1

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	–	–		–
SID242	V_{IL}	LVTTL input, $V_{DD} < 2.7$ V	–	–	$0.3 \times V_{DD}$		–
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, $V_{DD} \geq 2.7$ V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	$V_{DD} - 0.6$	–	–		$I_{OH} = 4$ mA at 3 V V_{DD}
SID60	V_{OH}	Output voltage high level	$V_{DD} - 0.5$	–	–		$I_{OH} = 1$ mA at 1.8 V V_{DD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 4$ mA at 1.8 V V_{DD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 10$ mA at 3 V V_{DD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		$I_{OL} = 3$ mA at 3 V V_{DD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DD} = 3.0$ V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67 ^[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DD} \geq 2.7$ V
SID68 ^[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–		$V_{DD} < 4.5$ V
SID68A ^[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5$ V
SID69 ^[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	–
SID69A ^[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 5. GPIO AC Specifications
 (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Load = 25 pF

Notes

3. V_{IH} must not exceed $V_{DD} + 0.2$ V.
4. Guaranteed by characterization.

Analog Peripherals
CTBm Opamp
Table 8. CTBm Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
	I _{DD}	Opamp block current, External load					
SID269	I _{DD_HI}	power=hi	–	1100	1850	μA	–
SID270	I _{DD_MED}	power=med	–	550	950		–
SID271	I _{DD_LOW}	power=lo	–	150	350		–
	G _{BW}	Load = 20 pF, 0.1 mA V _{D_{DDA}} = 2.7 V					
SID272	G _{BW_HI}	power=hi	6	–	–	MHz	Input and output are 0.2 V to V _{D_{DDA}} -0.2 V
SID273	G _{BW_MED}	power=med	3	–	–		Input and output are 0.2 V to V _{D_{DDA}} -0.2 V
SID274	G _{BW_LO}	power=lo	–	1	–		Input and output are 0.2 V to V _{D_{DDA}} -0.2 V
	I _{OUT_MAX}	V _{D_{DDA}} = 2.7 V, 500 mV from rail					
SID275	I _{OUT_MAX_HI}	power=hi	10	–	–	mA	Output is 0.5 V to V _{D_{DDA}} -0.5 V
SID276	I _{OUT_MAX_MID}	power=mid	10	–	–		Output is 0.5 V to V _{D_{DDA}} -0.5 V
SID277	I _{OUT_MAX_LO}	power=lo	–	5	–		Output is 0.5 V to V _{D_{DDA}} -0.5 V
	I _{OUT}	V _{D_{DDA}} = 1.71 V, 500 mV from rail					
SID278	I _{OUT_MAX_HI}	power=hi	4	–	–	mA	Output is 0.5 V to V _{D_{DDA}} -0.5 V
SID279	I _{OUT_MAX_MID}	power=mid	4	–	–		Output is 0.5 V to V _{D_{DDA}} -0.5 V
SID280	I _{OUT_MAX_LO}	power=lo	–	2	–		Output is 0.5 V to V _{D_{DDA}} -0.5 V
	I _{DD_Int}	Opamp block current Internal Load					
SID269_I	I _{DD_HI_Int}	power=hi	–	1500	1700	μA	–
SID270_I	I _{DD_MED_Int}	power=med	–	700	900		–
SID271_I	I _{DD_LOW_Int}	power=lo	–	–	–		–
	G _{BW}	V _{D_{DDA}} = 2.7 V	–	–	–	–	
SID272_I	G _{BW_HI_Int}	power=hi	8	–	–	MHz	Output is 0.25 V to V _{D_{DDA}} -0.25 V
		General opamp specs for both internal and external modes					
SID281	V _{IN}	Charge-pump on, V _{D_{DDA}} = 2.7 V	–0.05	–	V _{D_{DDA}} -0.2	V	–
SID282	V _{CM}	Charge-pump on, V _{D_{DDA}} = 2.7 V	–0.05	–	V _{D_{DDA}} -0.2		–
	V _{OUT}	V _{D_{DDA}} = 2.7 V					

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID283	V _{OUT_1}	power=hi, Iload=10 mA	0.5	–	V _{DDA} -0.5	V	–
SID284	V _{OUT_2}	power=hi, Iload=1 mA	0.2	–	V _{DDA} -0.2		–
SID285	V _{OUT_3}	power=med, Iload=1 mA	0.2	–	V _{DDA} -0.2		–
SID286	V _{OUT_4}	power=lo, Iload=0.1 mA	0.2	–	V _{DDA} -0.2		–
SID288	V _{OS_TR}	Offset voltage, trimmed	–1.0	±0.5	1.0	mV	High mode, input 0 V to V _{DDA} -0.2 V
SID288A	V _{OS_TR}	Offset voltage, trimmed	–	±1	–		Medium mode, input 0 V to V _{DDA} -0.2 V
SID288B	V _{OS_TR}	Offset voltage, trimmed	–	±2	–		Low mode, input 0 V to V _{DDA} -0.2 V
SID290	V _{OS_DR_TR}	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID290A	V _{OS_DR_TR}	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	V _{OS_DR_TR}	Offset voltage drift, trimmed	–	±10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V _{DDA} -0.2 V, Output is 0.2 V to V _{DDA} -0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V _{DDD} = 3.6 V, high-power mode, input is 0.2 V to V _{DDA} -0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	72	–	nV/rHz	Input and output are at 0.2 V to V _{DDA} -0.2 V
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	28	–		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	15	–		Input and output are at 0.2 V to V _{DDA} -0.2 V
SID297	C _{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V _{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T _{OP_WAKE}	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	COMP_MODE	Comparator mode; 50 mV drive, T _{rise} =T _{fall} (approx.)					

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to $V_{DDA}-0.2$ V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I _{DD_HI_M1}	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	I _{DD_MED_M1}	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	I _{DD_LOW_M1}	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	I _{DD_HI_M2}	Mode 2, High current	–	120	–		25 °C
SID_DS_5	I _{DD_MED_M2}	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	I _{DD_LOW_M2}	Mode 2, Low current	–	15	–		25 °C
SID_DS_7	G _{BW_HI_M1}	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_8	G _{BW_MED_M1}	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_9	G _{BW_LOW_M1}	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_10	G _{BW_HI_M2}	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_11	G _{BW_MED_M2}	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_12	G _{BW_Low_M2}	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_13	V _{OS_HI_M1}	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_14	V _{OS_MED_M1}	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_15	V _{OS_LOW_M2}	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_16	V _{OS_HI_M2}	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to $V_{DDA}-0.2$ V
SID_DS_17	V _{OS_MED_M2}	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_18	V _{OS_LOW_M2}	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID93	TSENSACC	Temperature sensor accuracy	-5	±1	5	°C	-40 to +85 °C

SAR ADC

Table 12. SAR ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SAR ADC DC Specifications							
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16		
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	
SID102	A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	
SID104	A_INCAP	Input capacitance	–	–	10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	–	–	TBD	V	
SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP	Sample rate	–	–	1	Msp/s	
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F _{IN} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–	–	A _{samp} /2	kHz	
SID111	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 1 Msp/s	-1.7	–	2	LSB	V _{REF} = 1 to V _{DD}
SID111A	A_INL	Integral non linearity. V _{DD} = 1.71 to 3.6, 1 Msp/s	-1.5	–	1.7	LSB	V _{REF} = 1.71 to V _{DD}
SID111B	A_INL	Integral non linearity. V _{DD} = 1.71 to 5.5, 500 ksp/s	-1.5	–	1.7	LSB	V _{REF} = 1 to V _{DD}
SID112	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 1 Msp/s	-1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID112A	A_DNL	Differential non linearity. V _{DD} = 1.71 to 3.6, 1 Msp/s	-1	–	2	LSB	V _{REF} = 1.71 to V _{DD}
SID112B	A_DNL	Differential non linearity. V _{DD} = 1.71 to 5.5, 500 ksp/s	-1	–	2.2	LSB	V _{REF} = 1 to V _{DD}
SID113	A_THD	Total harmonic distortion	–	–	-65	dB	F _{in} = 10 kHz
SID261	FSARINTREF	SAR operating speed without external reference bypass	–	–	100	ksp/s	12-bit resolution

LCD Direct Drive

Table 22. LCD Direct Drive DC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	μA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current V_{bias} = 5 V	–	2	–	mA	32 × 4 segments at 50 Hz 25 °C
SID158	I_{LCDOP2}	LCD system operating current V_{bias} = 3.3 V	–	2	–		32 × 4 segments at 50 Hz 25 °C

Table 23. LCD Direct Drive AC Specifications^[9]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note

9. Guaranteed by characterization.

Memory

Table 24. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 25. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	T _{ROWERASE} ^[10]	Row erase time	–	–	16		–
SID176	T _{ROWPROGRAM} ^[10]	Row program time after erase	–	–	4		–
SID178	T _{BULKERASE} ^[10]	Bulk erase time (64 KB)	–	–	35		–
SID180 ^[11]	T _{DEVPROG} ^[10]	Total device program time	–	–	7	Seconds	–
SID181 ^[11]	F _{END}	Flash endurance	100 K	–	–	Cycles	–
SID182 ^[11]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A ^[11]	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 26. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[11]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[11]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

Table 27. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[11]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[11]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

11. Guaranteed by characterization.

Watch Crystal Oscillator (WCO)

Table 33. WCO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	μW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal Load Capacitance	6	–	12.5	pF	
SID404	C0	Crystal Shunt Capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating Current (high power mode)	–	–	8	uA	

External Clock

Table 34. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305 ^[13]	ExtClkFreq	External clock input frequency	0	–	48	MHz	–
SID306 ^[13]	ExtClkDuty	Duty cycle; measured at V _{DD} /2	45	–	55	%	–

External Crystal Oscillator and PLL

Table 35. External Crystal Oscillator (ECO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID316 ^[13]	IECO1	External clock input frequency	–	–	1.5	mA	–
SID317 ^[13]	FECO	Crystal frequency range	4	–	33	MHz	–

Table 36. PLL Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	–	530	610	uA	
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	–	300	405	uA	
SID412	Fp1lin	PLL input frequency	1	–	48	MHz	
SID413	Fp1int	PLL intermediate frequency; prescaler out	1	–	3	MHz	
SID414	Fp1vco	VCO output frequency before post-divide	22.5	–	104	MHz	
SID415	Divvco	VCO Output post-divider range; PLL output frequency is Fp1vco/Divvco	1	–	8		
SID416	Pllocktime	Lock time at startup	–	–	250	μs	
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	–	–	150	ps	Guaranteed by design
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	–	–	200	ps	Guaranteed by design

System Clock

Table 37. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID262 ^[13]	T _{CLKSWITCH}	System clock source switching time	3	–	4	Periods	–

Note

13. Guaranteed by characterization.

Smart I/O

Table 38. Smart I/O Pass-through Time (Delay in Bypass Mode)

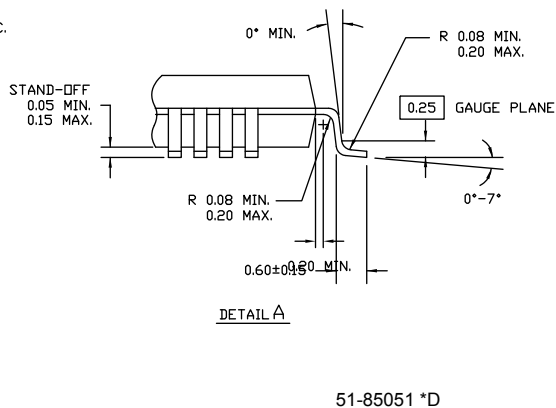
Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

CAN

Table 39. CAN Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID420	IDD_CAN	Block current consumption	–	–	200	μA	
SID421	CAN_bits	CAN Bit rate	–	–	1	Mbps	Min 8-MHZ clock

DIMENSIONS ARE IN MILLIMETERS



Technical drawing of Detail A, showing a cross-section of a mechanical part. The drawing includes the following dimensions and tolerances:

- STAND-OFF: 0.05 MIN. to 0.15 MAX.
- Top horizontal edge: 0° MIN.
- Top right fillet: R. 0.08 MIN. to 0.20 MAX.
- Top right flat section: 0.25
- Right vertical edge: GAUGE PLANE
- Right side fillet: 0-7°
- Right side flat section: 0.60 ± 0.15
- Bottom right horizontal edge: 1.00 REF.
- Bottom left fillet: R. 0.08 MIN. to 0.20 MIN.
- Bottom left flat section: 0.20 MIN.

DETAIL A

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



Acronyms

Table 44. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I ² C serial clock
SDA	I ² C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 45. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μV	microvolt
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt