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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x10b Slope, 16x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4147azi-s455

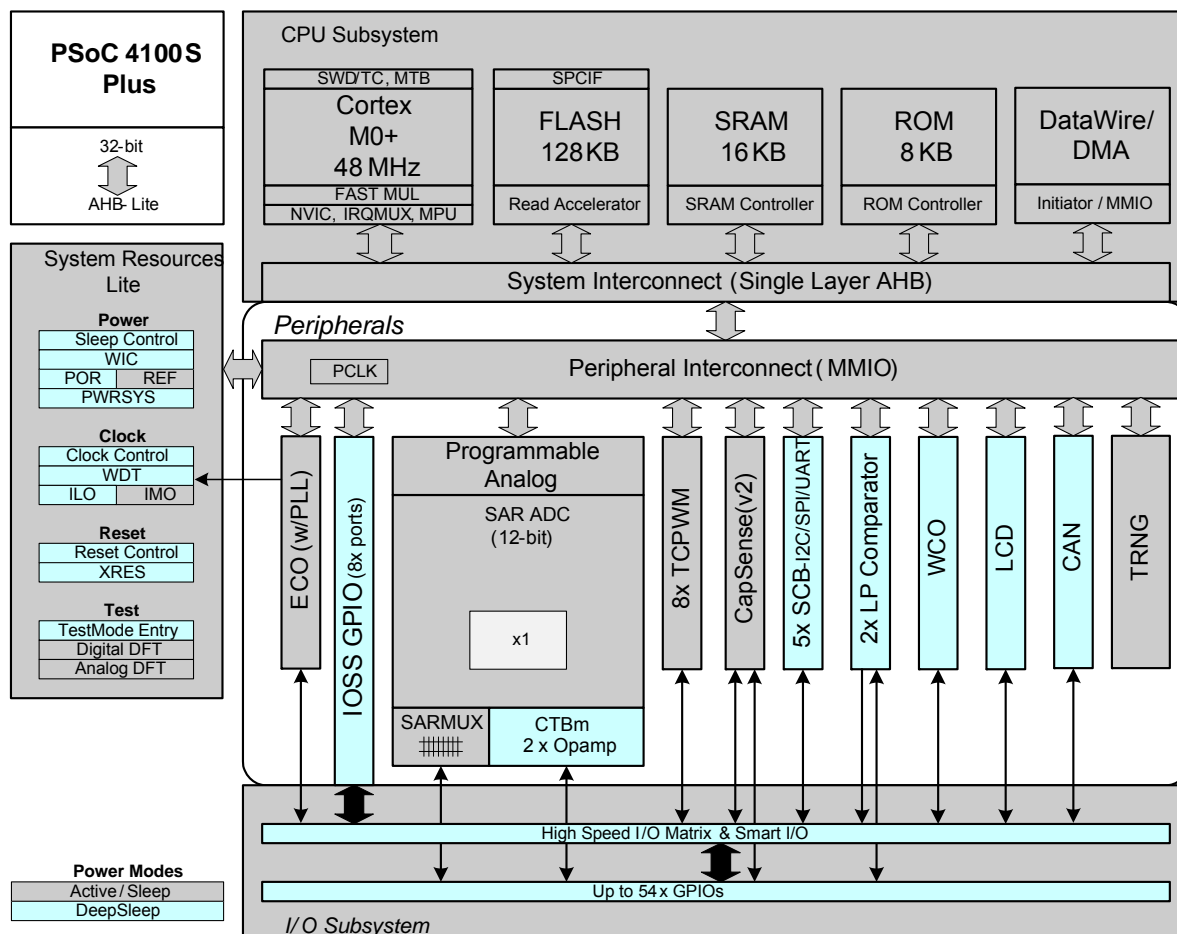
More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 4:

- Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
 - [AN79953](#): Getting Started With PSoC 4
 - [AN88619](#): PSoC 4 Hardware Design Considerations
 - [AN86439](#): Using PSoC 4 GPIO Pins
 - [AN57821](#): Mixed Signal Circuit Board Layout
 - [AN81623](#): Digital Design Best Practices
 - [AN73854](#): Introduction To Bootloaders
 - [AN89610](#): Arm Cortex Code Optimization
 - [AN85951](#): PSoC® 4 and PSoC Analog Coprocessor CapSense® Design Guide
- Technical Reference Manual (TRM) is in two documents:
 - [Architecture TRM](#) details each PSoC 4 functional block.
 - [Registers TRM](#) describes each of the PSoC 4 registers.
- Development Kits:
 - [CY8CKIT-041-41XX](#) PSoC 4100S CapSense Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
 - [CY8CKIT-149](#) PSoC® 4100S Plus Prototyping Kit enables you to evaluate and develop with Cypress' fourth-generation, low-power CapSense solution using the PSoC 4100S Plus devices.
- The [MiniProg3](#) device provides an interface for flash programming and debug.
- [Software User Guide](#):
 - A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.
- Component Datasheets:
 - The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.
- Online:
 - In addition to print documentation, the [Cypress PSoC forums](#) connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

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Figure 2. Block Diagram


PSoC 4100S Plus devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm Serial-Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE provides fully integrated programming and debug support for the PSoC 4100S Plus devices. The SWD interface is fully compatible with industry-standard third-party tools. PSoC 4100S Plus provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC 4100S Plus, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC 4100S Plus allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0+ CPU in the PSoC 4100S Plus is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU subsystem includes an 8-channel DMA engine and also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC 4100S Plus has four breakpoint (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4100S Plus device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

SRAM

16 KB of SRAM are provided with zero wait-state access at 48 MHz.

SRAM

An 8-KB supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

The power system is described in detail in the section [Power](#). It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). PSoC 4100S Plus operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSoC 4100S Plus provides Active, Sleep, and Deep Sleep low-power modes.

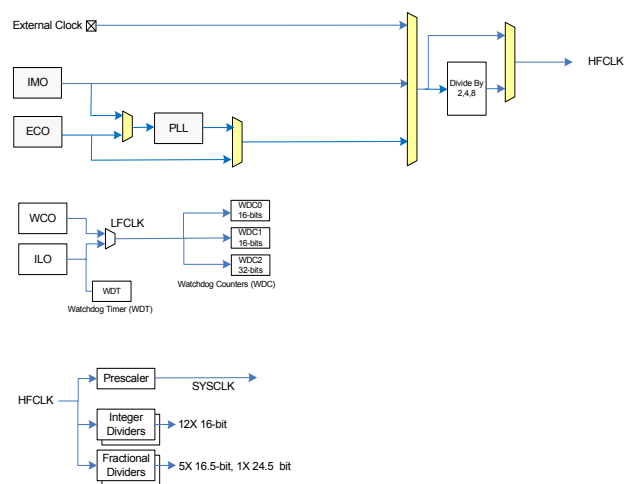
All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s. The opamps can remain operational in Deep Sleep mode.

Clock System

The PSoC 4100S Plus clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC 4100S Plus consists of the IMO, ILO, a 32-kHz Watch Crystal Oscillator (WCO), MHz ECO and PLL, and provision for an external clock. The WCO block allows locking the IMO to the 32-kHz oscillator.

Figure 3. PSoC 4100S Plus MCU Clocking Architecture



The HFCLK signal can be divided down as shown to generate synchronous clocks for the Analog and Digital peripherals. There are 18 clock dividers for the PSoC 4100S Plus (six with fractional divide capability, twelve with integer divide only). The twelve 16-bit integer divide capability allows a lot of flexibility in generating fine-grained frequency. In addition, there are five 16-bit fractional dividers and one 24-bit fractional divider.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100S Plus. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Cypress-provided calibration settings is \pm 2% over the entire voltage and temperature range.

ILO Clock Source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Programmable Digital Blocks

Smart I/O Block

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

Fixed Function Digital Blocks

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. Each block also incorporates a Quadrature decoder. There are eight TCPWM blocks in PSoC 4100S Plus.

Serial Communication Block (SCB)

PSoC 4100S Plus has five serial communication blocks, which can be programmed to have SPI, I²C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 400 kbps (Fast Mode) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of PSoC 4100S Plus and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

PSoC 4100S Plus is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

CAN

There is a CAN 2.0B block with support for TT-CAN.

GPIO

PSoC 4100S Plus has up to 54 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-up
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

Special Function Peripherals

CapSense

CapSense is supported in the PSoC 4100S Plus through a CapSense Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CapSense function can thus be provided on any available pin or group of pins in a system under software control. A PSoC Creator component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block has two IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

The CapSense block also provides a 10-bit Slope ADC function which can be used in conjunction with the CapSense function.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

LCD Segment Drive

PSoC 4100S Plus has an LCD controller, which can drive up to 4 commons and up to 50 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; one 32-bit register per port).

Pinouts

The following table provides the pin list for PSoC 4100S Plus for the 44-pin TQFP and 64-pin TQFP Normal and Fine Pitch packages.

64-TQFP		44-TQFP	
Pin	Name	Pin	Name
39	P0.0	24	P0.0
40	P0.1	25	P0.1
41	P0.2	26	P0.2
42	P0.3	27	P0.3
43	P0.4	28	P0.4
44	P0.5	29	P0.5
45	P0.6	30	P0.6
46	P0.7	31	P0.7
47	XRES	32	XRES
48	VCCD	33	VCCD
49	VSSD		
50	VDDD	34	VDDD
51	P5.0		
52	P5.1		
53	P5.2		
54	P5.3		
55	P5.5		
56	VDDA	35	VDDA
57	VSSA	36	VSSA
58	P1.0	37	P1.0
59	P1.1	38	P1.1
60	P1.2	39	P1.2
61	P1.3	40	P1.3
62	P1.4	41	P1.4
63	P1.5	42	P1.5
64	P1.6	43	P1.6
1	P1.7	44	P1.7
		1	VSSD
2	P2.0	2	P2.0
3	P2.1	3	P2.1
4	P2.2	4	P2.2
5	P2.3	5	P2.3
6	P2.4	6	P2.4
7	P2.5	7	P2.5
8	P2.6	8	P2.6
9	P2.7	9	P2.7
10	VSSD	10	P6.0
11	No Connect (NC)		
12	P6.0		
13	P6.1		

Port/Pin	Analog	Smart I/O	ACT #0	ACT #1	ACT #3	DS #2	DS #3
P2.4	sarmux[4]	Smartlo[0].io[4]	tcpwm.line[0]:1	scb[3].uart_rx:1			scb[1].spi_select1:1
P2.5	sarmux[5]	Smartlo[0].io[5]	tcpwm.line_compl[0]:1	scb[3].uart_tx:1			scb[1].spi_select2:1
P2.6	sarmux[6]	Smartlo[0].io[6]	tcpwm.line[1]:1	scb[3].uart_cts:1			scb[1].spi_select3:1
P2.7	sarmux[7]	Smartlo[0].io[7]	tcpwm.line_compl[1]:1	scb[3].uart_rts:1		lpcomp.comp[0]:0	scb[2].spi_mosi:1
P6.0			tcpwm.line[4]:1	scb[3].uart_rx:0	can.can_tx_enb_n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:0
P6.1			tcpwm.line_compl[4]:1	scb[3].uart_tx:0	can.can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:0
P6.2			tcpwm.line[5]:0	scb[3].uart_cts:0	can.can_tx:0		scb[3].spi_clk:0
P6.3			tcpwm.line_compl[5]:0	scb[3].uart_rts:0			scb[3].spi_select0:0
P6.4			tcpwm.line[6]:0			scb[4].i2c_scl	scb[3].spi_select1:0
P6.5			tcpwm.line_compl[6]:0			scb[4].i2c_sda	scb[3].spi_select2:0
P3.0		Smartlo[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		Smartlo[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		Smartlo[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		Smartlo[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		Smartlo[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5		Smartlo[1].io[5]	tcpwm.line_compl[2]:0				scb[1].spi_select2:0
P3.6		Smartlo[1].io[6]	tcpwm.line[3]:0			scb[4].spi_select3	scb[1].spi_select3:0
P3.7		Smartlo[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso:1
P4.0	csd.vref_ext			scb[0].uart_rx:0	can.can_rx:1	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshield			scb[0].uart_tx:0	can.can_tx:1	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmod			scb[0].uart_cts:0	can.can_tx_enb_n:1	lpcomp.comp[0]:1	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:2	scb[0].spi_select0:0
P4.4				scb[4].uart_rx		scb[4].spi_mosi	scb[0].spi_select1:2
P4.5				scb[4].uart_tx		scb[4].spi_miso	scb[0].spi_select2:2
P4.6				scb[4].uart_cts		scb[4].spi_clk	scb[0].spi_select3:2
P4.7				scb[4].uart_rts		scb[4].spi_select0	
P5.6			tcpwm.line[7]:0			scb[4].spi_select1	scb[2].spi_select3:0
P5.7			tcpwm.line_compl[7]:0			scb[4].spi_select2	
P7.0			tcpwm.line[0]:2	scb[3].uart_rx:2		scb[3].i2c_scl:2	scb[3].spi_mosi:1
P7.1			tcpwm.line_compl[0]:2	scb[3].uart_tx:2		scb[3].i2c_sda:2	scb[3].spi_miso:1
P7.2			tcpwm.line[1]:2	scb[3].uart_cts:2			scb[3].spi_clk:1

Electrical Specifications

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings^[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID1	V _{DDD_ABS}	Digital supply relative to V _{SS}	−0.5	—	6	V	—
SID2	V _{CCD_ABS}	Direct digital core voltage input relative to V _{SS}	−0.5	—	1.95		—
SID3	V _{GPIO_ABS}	GPIO voltage	−0.5	—	V _{DD} +0.5		—
SID4	I _{GPIO_ABS}	Maximum current per GPIO	−25	—	25	mA	—
SID5	I _{GPIO_injection}	GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS}	−0.5	—	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	—	—	V	—
BID45	ESD_CDM	Electrostatic discharge charged device model	500	—	—		—
BID46	LU	Pin current for latch-up	−140	—	140	mA	—

Device Level Specifications

All specifications are valid for −40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 2. DC Specifications

Typical values measured at V_{DD} = 3.3 V and 25 °C.

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID53	V _{DD}	Power supply input voltage	1.8	—	5.5	V	Internally regulated supply
SID255	V _{DD}	Power supply input voltage (V _{CCD} = V _{DDD} = V _{DDA})	1.71	—	1.89		Internally unregulated supply
SID54	V _{CCD}	Output voltage (for core logic)	—	1.8	—		—
SID55	C _{EFC}	External regulator voltage bypass	—	0.1	—	μF	X5R ceramic or better
SID56	C _{EXC}	Power supply bypass capacitor	—	1	—		X5R ceramic or better

Active Mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25 °C.

SID10	I _{DD5}	Execute from flash; CPU at 6 MHz	—	1.8	2.4	mA	Max is at 85 °C and 5.5 V
SID16	I _{DD8}	Execute from flash; CPU at 24 MHz	—	3.0	4.6		Max is at 85 °C and 5.5 V
SID19	I _{DD11}	Execute from flash; CPU at 48 MHz	—	5.4	7.1		Max is at 85 °C and 5.5 V

Note

- Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO
Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[3]}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$		CMOS Input
SID241	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	–	–		–
SID242	V_{IL}	LVTTL input, $V_{DD} < 2.7$ V	–	–	$0.3 \times V_{DD}$		–
SID243	$V_{IH}^{[3]}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, $V_{DD} \geq 2.7$ V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	$V_{DD} - 0.6$	–	–		$I_{OH} = 4$ mA at 3 V V_{DD}
SID60	V_{OH}	Output voltage high level	$V_{DD} - 0.5$	–	–		$I_{OH} = 1$ mA at 1.8 V V_{DD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 4$ mA at 1.8 V V_{DD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		$I_{OL} = 10$ mA at 3 V V_{DD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		$I_{OL} = 3$ mA at 3 V V_{DD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DD} = 3.0$ V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67 ^[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DD} \geq 2.7$ V
SID68 ^[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–		$V_{DD} < 4.5$ V
SID68A ^[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		$V_{DD} > 4.5$ V
SID69 ^[4]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	–
SID69A ^[4]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 5. GPIO AC Specifications
 (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DD} , Load = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DD} , Load = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DD} , Load = 25 pF

Notes

3. V_{IH} must not exceed $V_{DD} + 0.2$ V.
4. Guaranteed by characterization.

Table 8. CTBm Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID300	TPD1	Response time; power=hi	–	150	–	ns	Input is 0.2 V to $V_{DDA}-0.2$ V
SID301	TPD2	Response time; power=med	–	500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID302	TPD3	Response time; power=lo	–	2500	–		Input is 0.2 V to $V_{DDA}-0.2$ V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					
SID_DS_1	I _{DD_HI_M1}	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	I _{DD_MED_M1}	Mode 1, Medium current	–	700	–		25 °C
SID_DS_3	I _{DD_LOW_M1}	Mode 1, Low current	–	200	–		25 °C
SID_DS_4	I _{DD_HI_M2}	Mode 2, High current	–	120	–		25 °C
SID_DS_5	I _{DD_MED_M2}	Mode 2, Medium current	–	60	–		25 °C
SID_DS_6	I _{DD_LOW_M2}	Mode 2, Low current	–	15	–		25 °C
SID_DS_7	G _{BW_HI_M1}	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_8	G _{BW_MED_M1}	Mode 1, Medium current	–	2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_9	G _{BW_LOW_M1}	Mode 1, Low current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_10	G _{BW_HI_M2}	Mode 2, High current	–	0.5	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_11	G _{BW_MED_M2}	Mode 2, Medium current	–	0.2	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_12	G _{BW_Low_M2}	Mode 2, Low current	–	0.1	–		20-pF load, no DC load 0.2 V to $V_{DDA}-0.2$ V
SID_DS_13	V _{OS_HI_M1}	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_14	V _{OS_MED_M1}	Mode 1, Medium current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_15	V _{OS_LOW_M2}	Mode 1, Low current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_16	V _{OS_HI_M2}	Mode 2, High current	–	5	–		With trim 25 °C, 0.2V to $V_{DDA}-0.2$ V
SID_DS_17	V _{OS_MED_M2}	Mode 2, Medium current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V
SID_DS_18	V _{OS_LOW_M2}	Mode 2, Low current	–	5	–		With trim 25 °C, 0.2 V to $V_{DDA}-0.2$ V

Table 14. 10-bit CapSense ADC Specifications (continued)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksp	–	–	2	LSB	V _{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksp	–	–	1	LSB	

Digital Peripherals

Timer Counter Pulse-Width Modulator (TCPWM)

Table 15. TCPWM Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	TCPWM _{FREQ}	Operating frequency	–	–	F _c	MHz	F _c max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	TPWM _{ENEXT}	Input trigger pulse width	2/F _c	–	–	ns	For all trigger events ^[7]
SID.TCPWM.5	TPWM _{EXT}	Output trigger pulse widths	2/F _c	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC _{RES}	Resolution of counter	1/F _c	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM _{RES}	PWM resolution	1/F _c	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q _{RES}	Quadrature inputs resolution	1/F _c	–	–		Minimum pulse width between Quadrature phase inputs

²C

Table 16. Fixed I²C DC Specifications^[7]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID149	I _{I2C1}	Block current consumption at 100 kHz	–	–	50	μA	–
SID150	I _{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I _{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I _{I2C4}	I ² C enabled in Deep Sleep mode	–	1	–		

Table 17. Fixed I²C AC Specifications^[7]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID153	F _{I2C1}	Bit rate	–	–	1	Msp	–

Note

7. Guaranteed by characterization.

Memory

Table 24. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V _{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 25. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	T _{ROWWRITE} ^[10]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	T _{ROWERASE} ^[10]	Row erase time	–	–	16		–
SID176	T _{ROWPROGRAM} ^[10]	Row program time after erase	–	–	4		–
SID178	T _{BULKERASE} ^[10]	Bulk erase time (64 KB)	–	–	35		–
SID180 ^[11]	T _{DEVPROG} ^[10]	Total device program time	–	–	7	Seconds	–
SID181 ^[11]	F _{END}	Flash endurance	100 K	–	–	Cycles	–
SID182 ^[11]	F _{RET}	Flash retention. T _A ≤ 55 °C, 100 K P/E cycles	20	–	–	Years	–
SID182A ^[11]	–	Flash retention. T _A ≤ 85 °C, 10 K P/E cycles	10	–	–		–
SID256	TWS48	Number of Wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of Wait states at 24 MHz	1	–	–		CPU execution from Flash

System Resources

Power-on Reset (POR)

Table 26. Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.CLK#6	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185 ^[11]	V _{RISEIPOR}	Rising trip voltage	0.80	–	1.5	V	–
SID186 ^[11]	V _{FALLIPOR}	Falling trip voltage	0.70	–	1.4		–

Table 27. Brown-out Detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID190 ^[11]	V _{FALLPPOR}	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192 ^[11]	V _{FALLDPSLP}	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Notes

10. It can take as much as 20 milliseconds to write to Flash. During this time the device should not be Reset, or Flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

11. Guaranteed by characterization.

SWD Interface

Table 28. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCCLK1	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCCLK2	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7		SWDCCLK ≤ 1/3 CPU clock frequency
SID215 ^[12]	T_SWDI_SETUP	$T = 1/f_{\text{SWDCCLK}}$	$0.25 \cdot T$	–	–	ns	–
SID216 ^[12]	T_SWDI_HOLD	$T = 1/f_{\text{SWDCCLK}}$	$0.25 \cdot T$	–	–		–
SID217 ^[12]	T_SWDO_VALID	$T = 1/f_{\text{SWDCCLK}}$	–	–	$0.5 \cdot T$		–
SID217A ^[12]	T_SWDO_HOLD	$T = 1/f_{\text{SWDCCLK}}$	1	–	–		–

Internal Main Oscillator

Table 29. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	250	μA	–
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	180	μA	–

Table 30. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	
SID226	T _{STARTIMO}	IMO startup time	–	–	7	μs	–
SID228	T _{JITRMSIMO2}	RMS jitter at 24 MHz	–	145	–	ps	–

Internal Low-Speed Oscillator

Table 31. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I _{ILO1}	ILO operating current	–	0.3	1.05	μA	–

Table 32. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234 ^[12]	T _{STARTILO1}	ILO startup time	–	–	2	ms	–
SID236 ^[12]	T _{ILODUTY}	ILO duty cycle	40	50	60	%	–
SID237	F _{ILOTRIM1}	ILO frequency range	20	40	80	kHz	–

Note

12. Guaranteed by design.

Smart I/O

Table 38. Smart I/O Pass-through Time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	

CAN

Table 39. CAN Specifications

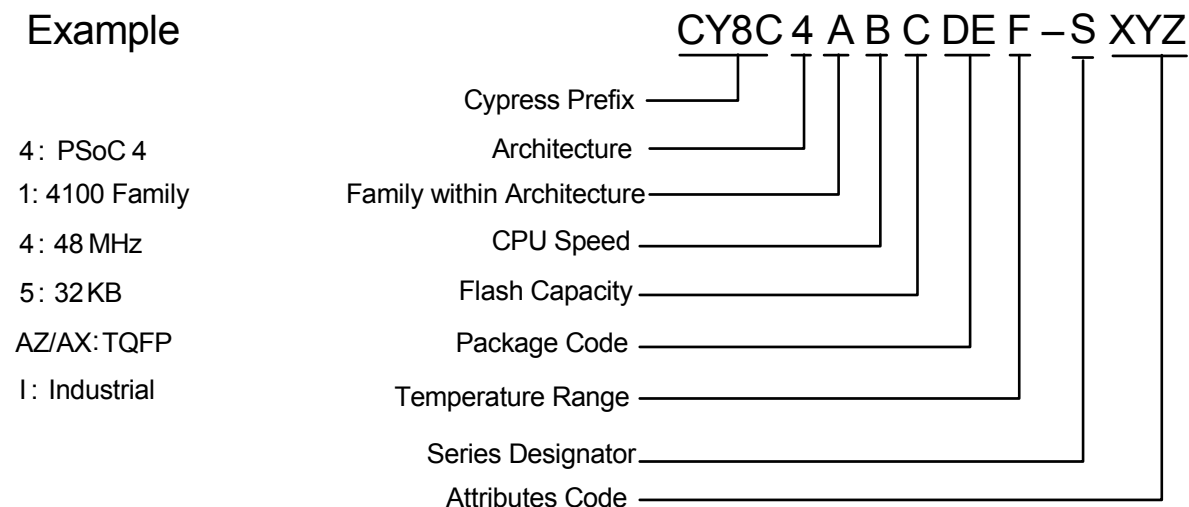
Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID420	IDD_CAN	Block current consumption	–	–	200	μA	
SID421	CAN_bits	CAN Bit rate	–	–	1	Mbps	Min 8-MHZ clock

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	1	4100 Family
B	CPU Speed	2	24 MHz
		4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX	TQFP (0.8-mm pitch)
		AZ	TQFP (0.5-mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature Range	I	Industrial
S	Series Designator	S	PSoC 4 S-Series
		M	PSoC 4 M-Series
		L	PSoC 4 L-Series
		BL	PSoC 4 BLE-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

The following is an example of a part number:

Example



Packaging

The PSoC 4100S Plus will be offered in 44 TQFP, 64 TQFP Normal pitch, and 64 TQFP Fine Pitch packages.

Package dimensions and Cypress drawing numbers are in the following table.

Table 40. Package List

Spec ID#	Package	Description	Package Dwg
BID20	64-pin TQFP	14 × 14 × 1.4-mm height with 0.8-mm pitch	51-85046
BID27	64-pin TQFP	10 × 10 × 1.6-mm height with 0.5-mm pitch	51-85051
BID34A	44-pin TQFP	10 × 10 × 1.4-mm height with 0.8-mm pitch	51-85064

Table 41. Package Thermal Characteristics

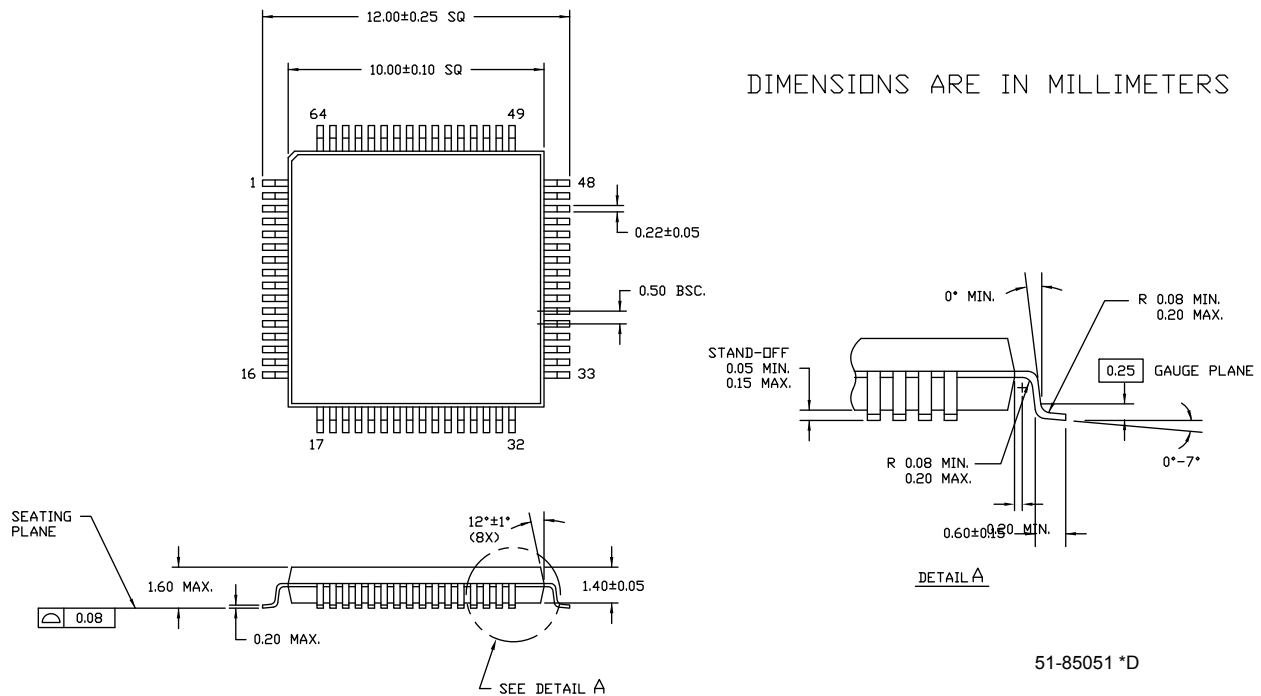
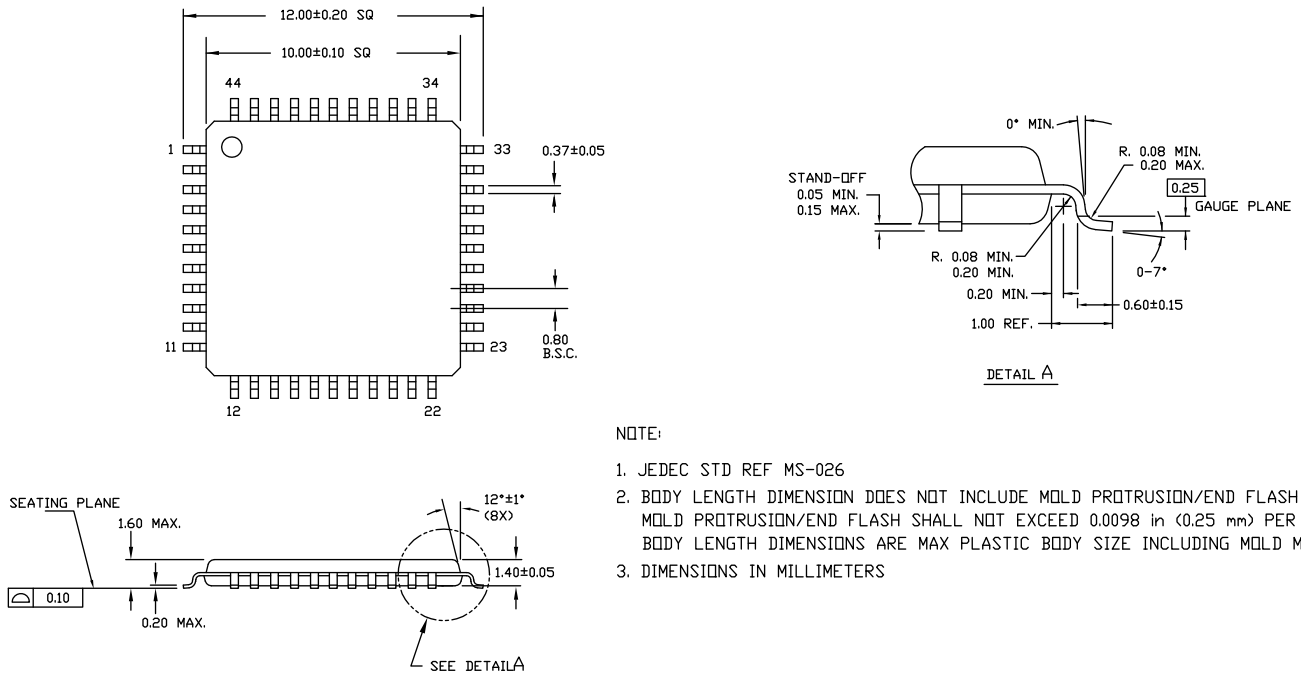
Parameter	Description	Package	Min	Typ	Max	Units
T _A	Operating ambient temperature		−40	25	85	°C
T _J	Operating junction temperature		−40	—	100	°C
T _{JA}	Package θ _{JA}	44-pin TQFP	—	55.6	—	°C/Watt
T _{JC}	Package θ _{JC}	44-pin TQFP	—	14.4	—	°C/Watt
T _{JA}	Package θ _{JA}	64-pin TQFP (0.5-mm pitch)	—	46	—	°C/Watt
T _{JC}	Package θ _{JC}	64-pin TQFP (0.5-mm pitch)	—	10	—	°C/Watt
T _{JA}	Package θ _{JA}	64-pin TQFP (0.8-mm pitch)	—	36.8	—	°C/Watt
T _{JC}	Package θ _{JC}	64-pin TQFP (0.8-mm pitch)	—	9.4	—	°C/Watt

Table 42. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 43. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

Figure 8. 64-pin TQFP Package (0.5-mm Pitch) Outline

Figure 9. 44-Pin TQFP Package Outline

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

Acronyms

Table 44. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 44. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I ² C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

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