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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Audio Processor
Interface	Host Interface, I²C, SAI, SPI
Clock Rate	120MHz
Non-Volatile Memory	ROM (126kB)
On-Chip RAM	42kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dspb56362ag120r2

2.10 Digital Audio Interface (DAX)

Table 2-12 Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI	Input	Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively).
PD0	Input, Output, or Disconnected		**Port D 0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
ADO	Output	Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/EBU, CP340 and IEC958 data in a biphase mark format.
PD1	Input, Output, or Disconnected		**Port D 1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.11 Timer

Table 2-13 Timer Signal

Signal Name	Type	State During Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected it to Vcc through a pull-up resistor in order to ensure a stable logic level at the input. This input is 5 V tolerant.

Table 3-5 Clock Operation (continued) 100 and 120 MHz Values

No.	Characteristics	Symbol	100 MHz		120 MHz	
			Min	Max	Min	Max
6	CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1, PDF = 1, Ef > 15 MHz)[4, 5] CLKOUT falling edge from EXTAL rising edge with PLL enabled (MF = 2 or 4, PDF = 1, Ef > 15 MHz)[4, 5] CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[4, 5]		0.0 ns 0.0 ns 0.0 ns	1.8 ns 1.8 ns 1.8 ns		
7	Instruction cycle time = I_{CYC} = T_C[6] See Table 3-5 (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	 0.00 ns 0.00 ns	 ∞ 8.53 µs		 8.53 µs

1 Measured at 50% of the input transition.

2 The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.

3 The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

4 Periodically sampled and not 100% tested.

5 The skew is not guaranteed for any other MF value.

6 The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.

3.8 Phase Lock Loop (PLL) Characteristics

Table 3-6 PLL Characteristics

Characteristics	100 MHz		Unit
	Min	Max	
V_{CO} frequency when PLL enabled (MF × E_f × 2/PDF)	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP})[1] • @ MF ≤ 4 • @ MF > 4	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	 pF pF
Note:			

1 C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(680 × MF) – 120, for MF ≤ 4, or
1100 × MF, for MF > 4

3.10 External Memory Expansion Port (Port A)

3.10.1 SRAM Timing

Table 3-8 SRAM Read and Write Accesses 100 and 120 MHz[1]

No.	Characteristics	Symbol	Expression[2]	100 MHz		120 MHz		Unit
				Min	Max	Min	Max	
100	Address valid and AA assertion pulse width[3]	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ $[1 \le WS \le 3]$	16.0	—	12.0	—	ns
			$(WS + 2) \times T_C - 4.0$ $[4 \le WS \le 7]$	56.0	—	46.0	—	ns
			$(WS + 3) \times T_C - 4.0$ $[WS \ge 8]$	106.0	—	87.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	**100 MHz:** $0.25 \times T_C - 2.0$ $[WS = 1]$	0.5	—	0.1	—	ns
			$1.25 \times T_C - 2.0$ $[WS \ge 4]$	10.5	—	8.4	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	**100 MHz:** $1.5 \times T_C - 4.0$ $[WS = 1]$	11.0	—	8.5	—	ns
			All frequencies: $WS \times T_C - 4.0$ $[2 \le WS \le 3]$	16.0	—	12.7	—	ns
			$(WS - 0.5) \times T_C - 4.0$ $[WS \ge 4]$	31.0	---	25.2	—	
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	**100 MHz:** $0.25 \times T_C - 2.0$ $[1 \le WS \le 3]$	0.5	—	0.1	—	ns
			$1.25 \times T_C - 2.0$ $[4 \le WS \le 7]$	10.5	—	8.4	—	
			$2.25 \times T_C - 2.0$ $[WS \ge 8]$	20.5	—	16.7	—	
			All frequencies: $1.25 \times T_C - 4.0$ $[4 \le WS \le 7]$	8.5	—	6.4	—	
			$2.25 \times T_C - 4.0$ $[WS \ge 8]$	18.5	—	14.7	—	

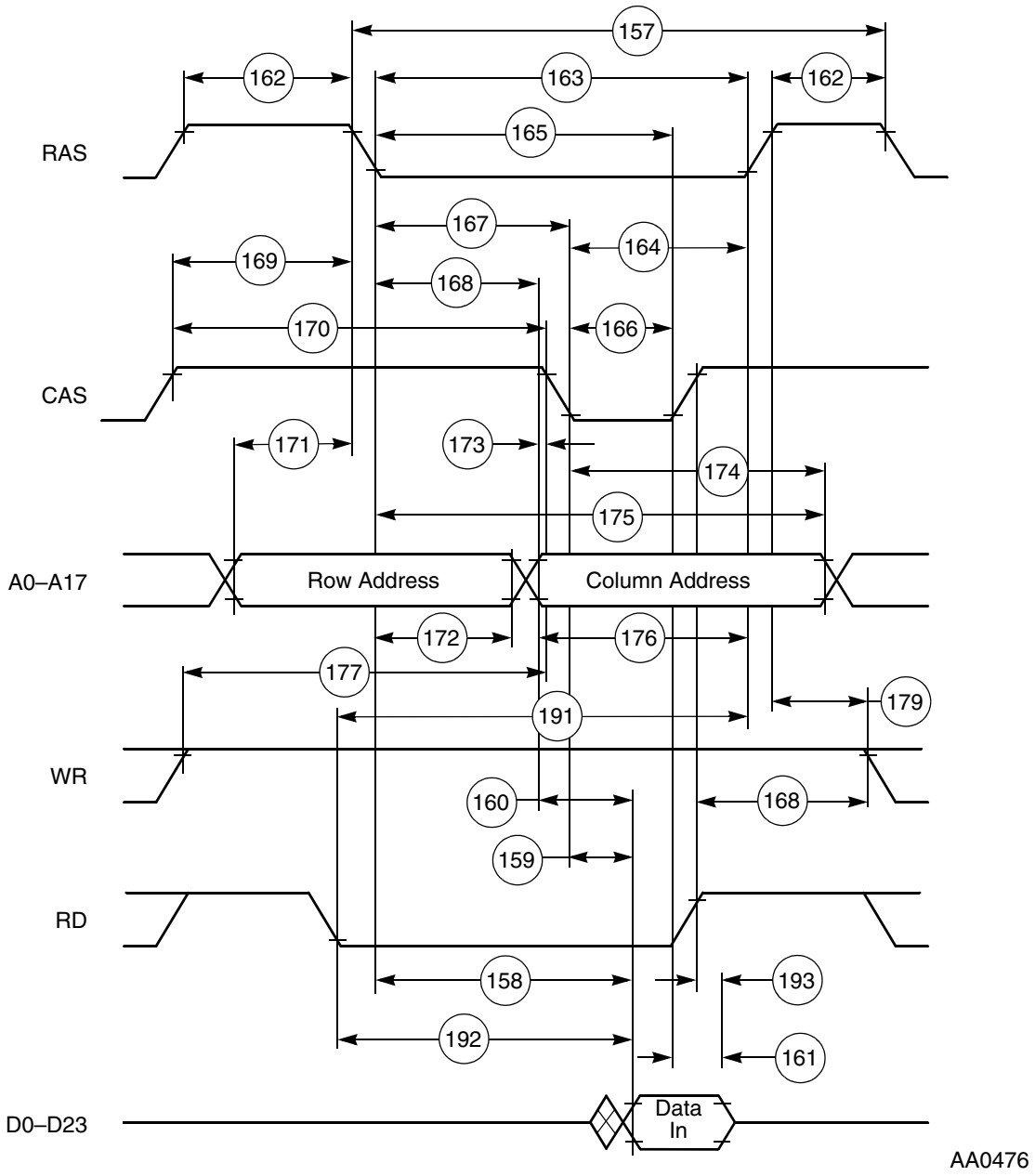

Figure 3-17 DRAM Out-of-Page Read Access

Table 3-17 External Bus Synchronous Timings (SRAM Access)[1] (continued)

No.	Characteristics	Expression[2, 3]	100 MHz		Unit
			Min	Max	
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	4.0	ns
210	CLKOUT high to $\overline{WR}$ assertion[5]	$0.5 \times T_C + 4.3$ [WS = 1 or WS ≥ 4]	6.3	9.3	ns
		All frequencies: [2 ≤ WS ≤ 3]	1.3	4.3	
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	3.8	ns

1 External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.

2 WS is the number of wait states specified in the BCR.

3 The asynchronous delays specified in the expressions are valid for DSP56362.

4 T198 and T199 are valid for Address Trace mode if the ATE bit in the OMR is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A0–A23 is internal or external, when this mode is enabled

5 If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.

3.11 Parallel Host Interface (HDI08) Timing

Table 3-20 Host Interface (HDI08) Timing[1, 2]

No.	Characteristics[3]	Expression	100 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[4] $\overline{\text{HACK}}$ read assertion width	$T_C + 9.9$	19.9	—	ns
318	Read data strobe deassertion width[4] $\overline{\text{HACK}}$ read deassertion width	—	9.9	—	ns
319	Read data strobe deassertion width[4] after “Last Data Register” reads[5, 6], or between two consecutive CVR, ICR, or ISR reads[7] $\overline{\text{HACK}}$ deassertion width after “Last Data Register” reads[5, 6]	$2.5 \times T_C + 6.6$	31.6	—	ns
320	Write data strobe assertion width[8]$\overline{\text{HACK}}$ write assertion width	—	13.2	—	ns
321	Write data strobe deassertion width[8] $\overline{\text{HACK}}$ write deassertion width after ICR, CVR and “Last Data Register” writes[5]	$2.5 \times T_C + 6.6$	31.6	—	ns
	after IVR writes, or after TXH:TXM writes (with HBE=0), or after TXL:TXM writes (with HBE=1)		16.5	—	
322	$\overline{\text{HAS}}$ assertion width	—	9.9	—	ns
323	$\overline{\text{HAS}}$ deassertion to data strobe assertion[9]	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[8] Host data input setup time before $\overline{\text{HACK}}$ write deassertion	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[8] Host data input hold time after $\overline{\text{HACK}}$ write deassertion	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[4] $\overline{\text{HACK}}$ read assertion to output data active from high impedance	—	3.3	—	ns
327	Read data strobe assertion to output data valid[4] $\overline{\text{HACK}}$ read assertion to output data valid	—	—	24.2	ns
328	Read data strobe deassertion to output data high impedance[4] $\overline{\text{HACK}}$ read deassertion to output data high impedance	—	—	9.9	ns
329	Output data hold time after read data strobe deassertion[4] Output data hold time after $\overline{\text{HACK}}$ read deassertion	—	3.3	—	ns
330	$\overline{\text{HCS}}$ assertion to read data strobe deassertion[4]	$T_C + 9.9$	19.9	—	ns
331	$\overline{\text{HCS}}$ assertion to write data strobe deassertion[8]	—	9.9	—	ns
332	$\overline{\text{HCS}}$ assertion to output data valid	—	—	19.1	ns

Table 3-20 Host Interface (HDI08) Timing[1, 2] (continued)

No.	Characteristics[3]	Expression	100 MHz		Unit
			Min	Max	
333	$\overline{HCS}$ hold time after data strobe deassertion[9]	—	0.0	—	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	—	4.7	—	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	—	3.3	—	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[9] • Read • Write	—	 0 4.7	 — —	ns
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[9]	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[4, 5, 10]	T_C	10	—	ns
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[5, 8, 10]	$2 \times T_C$	20	—	ns
340	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[5, 9, 10]	—	—	19.1	ns
341	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request)[5, 9, 10, 11]	—	—	300.0	ns
342	Delay from DMA $\overline{HACK}$ deassertion to HOREQ assertion • For “Last Data Register” read[5] • For “Last Data Register” write[5] • For other cases	 $2 \times T_C + 19.1$ $1.5 \times T_C + 19.1$	 39.1 34.1 0.0	 — — —	ns
343	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion • HROD = 0[5]	—	 —	 20.2	ns
344	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request[5, 11]	—	 —	 300.0	ns

1 See **Host Port Usage Considerations** in the DSP56362 User Design Manual.

2 In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.

3 V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +100°C, C_L = 50 pF

4 The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.

5 The “last data register” is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the little endian mode (HBE = 0), or RXH/TXH in the big endian mode (HBE = 1).

6 This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.

7 This timing is applicable only if two consecutive reads from one of these registers are executed.

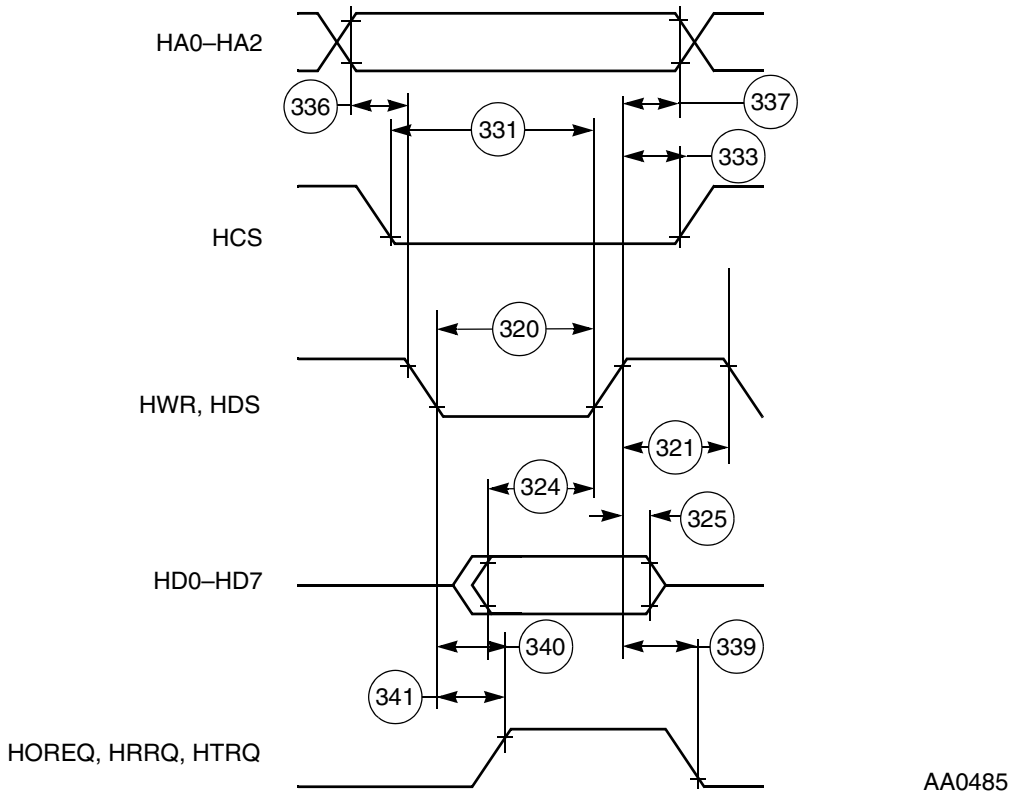

Figure 3-29 Write Timing Diagram, Non-Multiplexed Bus

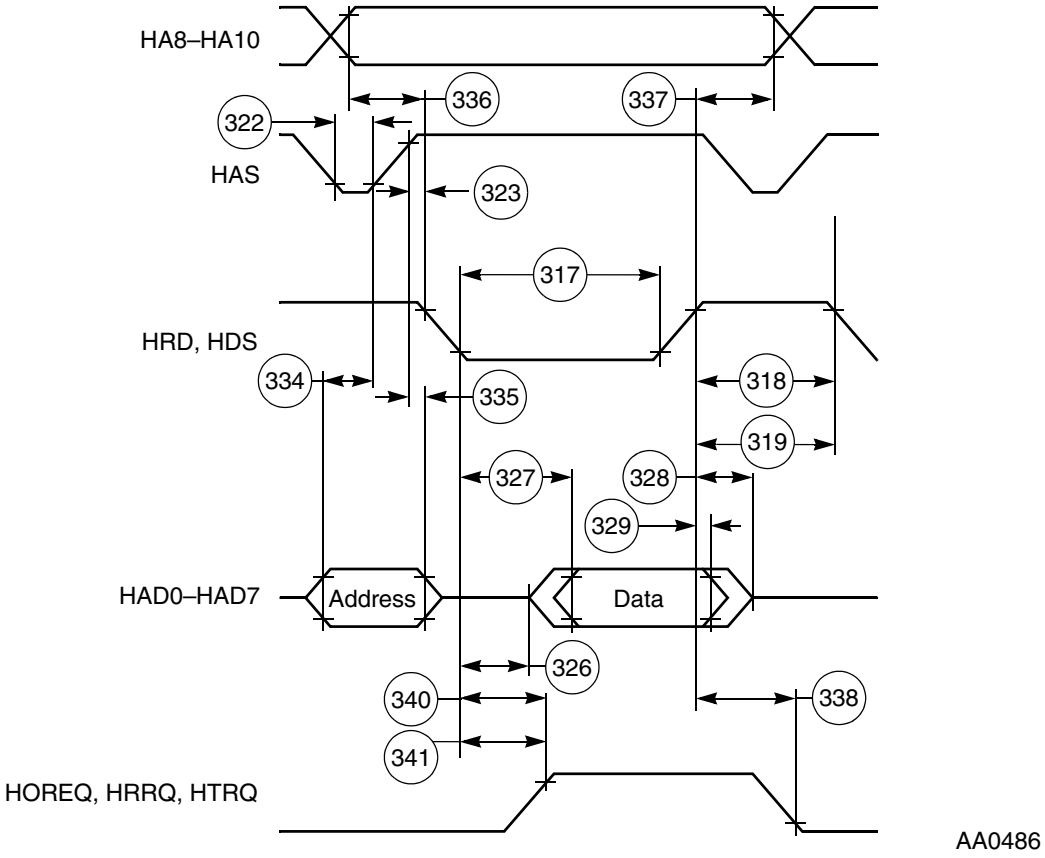

Figure 3-30 Read Timing Diagram, Multiplexed Bus

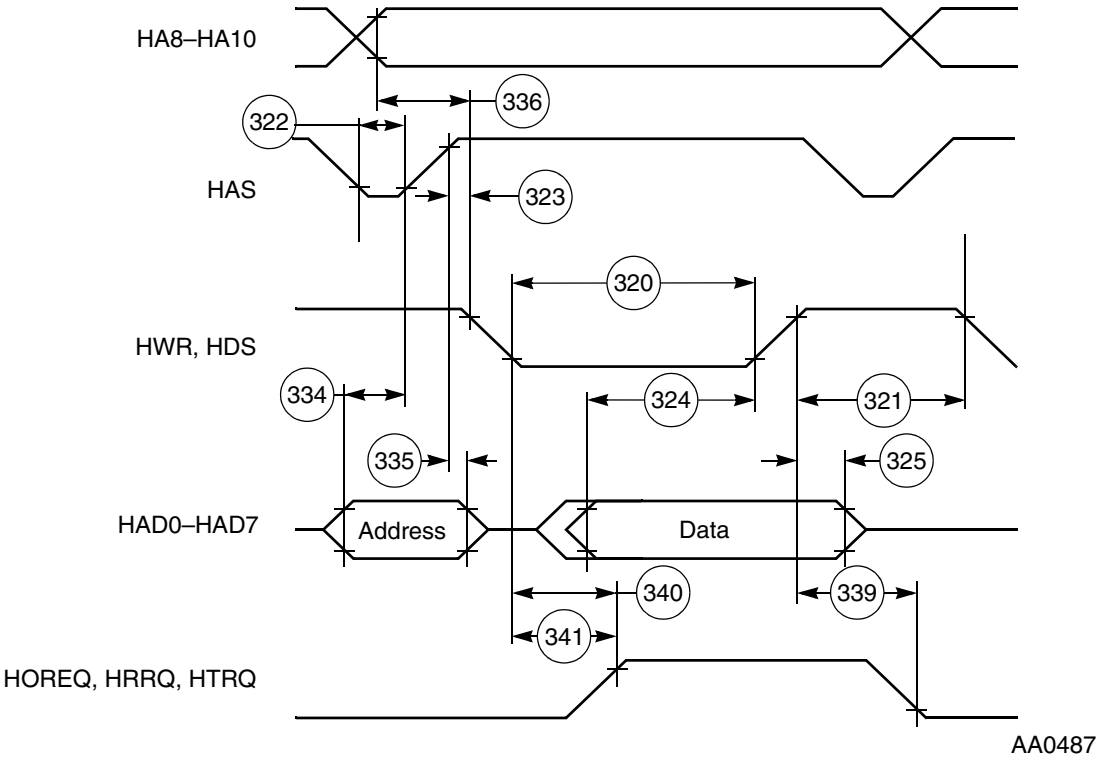

Figure 3-31 Write Timing Diagram, Multiplexed Bus

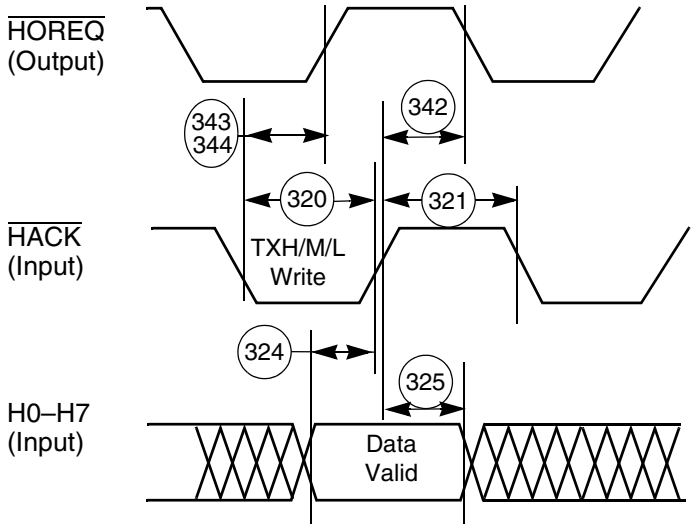

Figure 3-32 Host DMA Write Timing Diagram

3.13 Serial Host Interface (SHI) I2C Protocol Timing

Table 3-22 SHI I2C Protocol Timing

Standard I2C*							
No.	Characteristics	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
	Tolerable spike width on SCL or SDA Filters bypassed Narrow filters enabled Wide filters enabled	—	 — — —	 0 50 100	 — — —	 0 50 100	ns
171	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
172	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	—	0.6	—	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
175	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
176	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
177	SCL and SDA rise time	T_R	—	1000	$20 + 0.1 \times C_b$	300	ns
178	SCL and SDA fall time	T_F	—	300	$20 + 0.1 \times C_b$	300	ns
179	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
180	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
181	Stop condition set-up time	$T_{SU;STO}$	4.0	—	0.6	—	µs
182	Capacitive load for each line	C_b	—	400	—	400	pF
183	DSP clock frequency Filters bypassed Narrow filters enabled Wide filters enabled	F_{DSP}	 10.6 11.8 13.1	 — — —	 28.5 39.7 61.0	 — — —	MHz
184	$\overline{HREQ}$ in deassertion to last SCL edge ($\overline{HREQ}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
186	First SCL sampling edge to $\overline{HREQ}$ output deassertion Filters bypassed Narrow filters enabled Wide filters enabled	$T_{NG;RQO}$ $2 \times T_C + 30$ $2 \times T_C + 120$ $2 \times T_C + 208$	 — — —	 50 140 228	 — — —	 50 140 228	ns

Table 3-23 SCL Serial Clock Cycle generated as Master

Filters bypassed	$T_{I^2CCP} + 2.5 \times T_C + 45ns + T_R$
Narrow filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 135ns + T_R$
Wide filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 223ns + T_R$

EXAMPLE:

For DSP clock frequency of 100 MHz (i.e. $T_C = 10ns$), operating in a standard-mode I^2C environment ($F_{SCL} = 100$ KHz (i.e. $T_{SCL} = 10\mu s$), $T_R = 1000ns$), with filters bypassed

$$T_{I^2CCP} = 10\mu s - 2.5 \times 10ns - 45ns - 1000ns = 8930ns$$

Choosing HRS = 0 gives

$$HDM[7:0] = 8930ns/(2 \times 10ns \times 8) - 1 = 55.8$$

Thus the HDM[7:0] value should be programmed to $38 (=56).

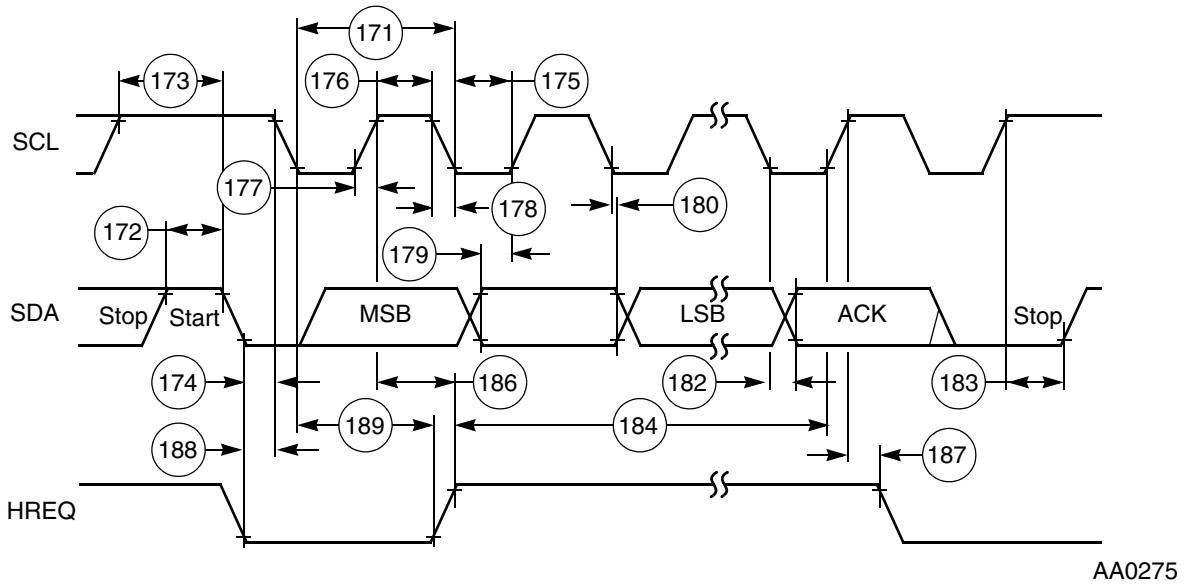

Figure 3-39 I2C Timing

Table 3-24 Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	100 MHz		Condition[4]	Unit
				Min	Max		
458	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns
459	FST input (wl) to transmitter drive enable assertion	—	—	—	31.0	—	ns
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge	—	—	— —	32.0 18.0	x ck i ck	ns
463	HCKR/HCKT clock cycle	—	—	40.0	—		ns
464	HCKT input rising edge to TXC output	—	—	—	27.5		ns
465	HCKR input rising edge to RXC output	—	—	—	27.5		ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = 0°C to +100°C, C_L = 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode (asynchronous implies that TXC and RXC are two different clocks)
i ck s = internal clock, synchronous mode (synchronous implies that TXC and RXC are the same clock)

3 bl = bit length
wl = word length
wr = word length relative

4 TXC(SCKT pin) = transmit clock
RXC(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the clock cycle at the pin is defined by Icyc and the ESAI control registers.

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.

7 Periodically sampled and not 100% tested.

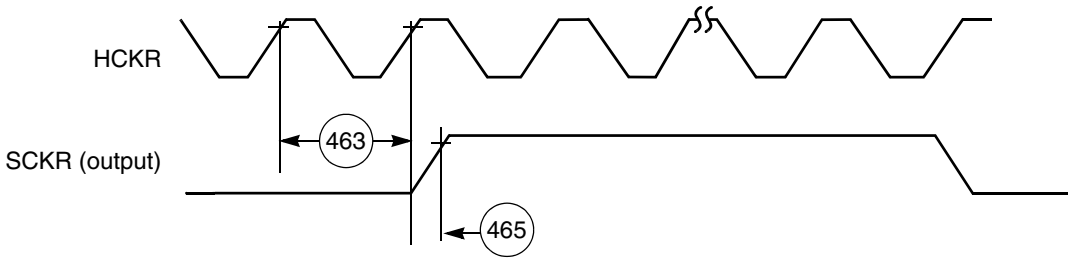

Figure 3-43 ESAI HCKR Timing

3.15 Digital Audio Transmitter Timing

Table 3-25 Digital Audio Transmitter Timing

No.	Characteristic	Expression	100 MHz		Unit
			Min	Max	
	ACI frequency[1]	—	—	50	MHz
220	ACI period	$2 \times T_C$	20	—	ns
221	ACI high duration	$0.5 \times T_C$	5	—	ns
222	ACI low duration	$0.5 \times T_C$	5	—	ns
223	ACI rising edge to ADO valid	$1.5 \times T_C$	—	15	ns

1 In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of the DSP56362 internal clock frequency. For example, if the DSP56362 is running at 100 MHz internally, the ACI frequency should be less than 50 MHz.

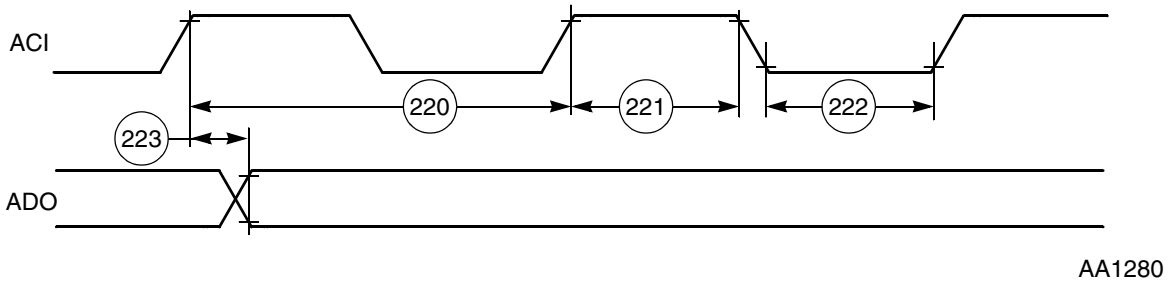

Figure 3-44 Digital Audio Transmitter Timing

Table 4-1 DSP56362 LQFP Signal Identification by Pin Number

Pin No.	Signal Name[1]	Pin No.	Signal Name[1]	Pin No.	Signal Name[1]
1	SCK/SCL	26	GND_S	51	AA2/$\overline{RAS2}$
2	$\overline{SS}$/HA2	27	ADO or PD1	52	$\overline{CAS}$
3	$\overline{HREQ}$	28	ACI or PD0	53	$\overline{DE}$
4	SDO0 or PC11	29	TIO0	54	GND_Q
5	$\overline{SDO1}$ or $\overline{PC10}$	30	$\overline{HCS}$/HCS, HA10, or PB13	55	EXTAL
6	SDO2/SDI3 or PC9	31	HA2, HA9, or PB10	56	V_{CCQL}
7	SDO3/SDI2 or PC8	32	HA1, HA8, or PB9	57	V_{CCC}
8	V_{CCS}	33	HA0, $\overline{HAS}$/HAS, or PB8	58	GND_C
9	GND_S	34	H7, HAD7, or PB7	59	CLKOUT
10	SDO4/SDI1 or PC7	35	H6, HAD6, or PB6	60	NC (not connected)
11	SDO5/SDI0 or PC6	36	H5, HAD5, or PB5	61	$\overline{PINIT}$/$\overline{NMI}$
12	FST or PC4	37	H4, HAD4, or PB4	62	$\overline{TA}$
13	FSR or PC1	38	V_{CCH}	63	$\overline{BR}$
14	SCKT or PC3	39	GND_H	64	$\overline{BB}$
15	SCKR or PC0	40	H3, HAD3, or PB3	65	V_{CCC}
16	HCKT or PC5	41	H2, HAD2, or PB2	66	GND_C
17	HCKR or PC2	42	H1, HAD1, or PB1	67	$\overline{WR}$
18	V_{CCQL}	43	H0, HAD0, or PB0	68	$\overline{RD}$
19	GND_Q	44	$\overline{RESET}$	69	AA1/$\overline{RAS1}$
20	V_{CCQH}	45	V_{CCP}	70	AA0/$\overline{RAS0}$
21	$\overline{HDS}$/HDS, $\overline{HWR}$/HWR, or PB12	46	PCAP	71	$\overline{BG}$
22	HRW, $\overline{HRD}$/HRD, or PB11	47	GND_P	72	A0
23	$\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, or PB15	48	GND_{P1}	73	A1
24	$\overline{HOREQ}$/HOREQ, $\overline{HTRQ}$/HTRQ, or PB14	49	V_{CCQH}	74	V_{CCA}
25	V_{CCS}	50	AA3/$\overline{RAS3}$	75	GND_A

Table 4-2 DSP56362 LQFP Signal Identification by Name (continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
$\overline{\text{NMI}}$	61	$\overline{\text{RAS2}}$	52	V_{CCD}	129
PB0	43	$\overline{\text{RAS3}}$	51	V_{CCH}	38
PB1	42	$\overline{\text{RD}}$	68	V_{CCP}	45
PB10	31	RESET	44	V_{CCQH}	20
PB11	22	SCK	1	V_{CCQH}	49
PB12	21	SCKR	15	V_{CCQH}	95
PB13	30	SCKT	14	V_{CCQL}	18
PB14	24	SCL	1	V_{CCQL}	56
PB15	23	SDA	144	V_{CCQL}	91
PB2	41	SDI0	11	V_{CCQL}	126
PB3	40	SDI1	10	V_{CCS}	8
PB4	37	SDI2	7	V_{CCS}	25
PB5	36	SDI3	6	$\overline{\text{WR}}$	67
PB6	35	SDO0	4		
PB7	34	SDO1	5		
PB8	33	SDO2	6		

5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A = ambient temperature °C

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W

$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W

$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

```
          do        #(XDAT_END-XDAT_START),XLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
          move      #INT_YDAT,r0
          move      #YDAT_START,r1
          do        #(YDAT_END-YDAT_START),YLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,y:(r0)+
YLOAD_LOOP
;

          jmp       INT_PROG

PROG_START
          move      #$0,r0
          move      #$0,r4
          move      #$3f,m0
          move      #$3f,m4
;
          clr       a
          clr       b
          move      #$0,x0
          move      #$0,x1
          move      #$0,y0
          move      #$0,y1
          bset      #4,omr              ; ebd
;
sbr       dor       #60,_end
          mac       x0,y0,a   x:(r0)+,x1          y:(r4)+,y1
          mac       x1,y1,a   x:(r0)+,x0          y:(r4)+,y0
          add       a,b
          mac       x0,y0,a   x:(r0)+,x1
          mac       x1,y1,a                       y:(r4)+,y0
          move      b1,x:$ff
_end
          bra       sbr
          nop
          nop
          nop
          nop
PROG_END
          nop
          nop


XDAT_START
;         org       x:0
          dc        $262EB9
          dc        $86F2FE
          dc        $E56A5F
          dc        $616CAC
```

```
dc        $8FFD75
dc        $9210A
dc        $A06D7B
dc        $CEA798
dc        $8DFBF1
dc        $A063D6
dc        $6C6657
dc        $C2A544
dc        $A3662D
dc        $A4E762
dc        $84F0F3
dc        $E6F1B0
dc        $B3829
dc        $8BF7AE
dc        $63A94F
dc        $EF78DC
dc        $242DE5
dc        $A3E0BA
dc        $EBAB6B
dc        $8726C8
dc        $CA361
dc        $2F6E86
dc        $A57347
dc        $4BE774
dc        $8F349D
dc        $A1ED12
dc        $4BFCE3
dc        $EA26E0
dc        $CD7D99
dc        $4BA85E
dc        $27A43F
dc        $A8B10C
dc        $D3A55
dc        $25EC6A
dc        $2A255B
dc        $A5F1F8
dc        $2426D1
dc        $AE6536
dc        $CBBC37
dc        $6235A4
dc        $37F0D
dc        $63BEC2
dc        $A5E4D3
dc        $8CE810
dc        $3FF09
dc        $60E50E
dc        $CFFB2F
dc        $40753C
dc        $8262C5
dc        $CA641A
dc        $EB3B4B
dc        $2DA928
dc        $AB6641
dc        $28A7E6
dc        $4E2127
```

```
144 sda                ip5b_io
|
[Model]         ip5b_i
Model_type         Input
Polarity         Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp         5.00pF         5.00pF         5.00pF
|
|
[Voltage Range]       3.3v       3v       3.6v
[GND_clamp]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00    -5.21e+02    -3.65e+02    -5.18e+02
-3.10e+00    -4.69e+02    -3.30e+02    -4.67e+02
-2.90e+00    -4.18e+02    -2.94e+02    -4.16e+02
-2.70e+00    -3.67e+02    -2.59e+02    -3.65e+02
-2.50e+00    -3.16e+02    -2.23e+02    -3.14e+02
-2.30e+00    -2.65e+02    -1.88e+02    -2.63e+02
-2.10e+00    -2.14e+02    -1.52e+02    -2.12e+02
-1.90e+00    -1.63e+02    -1.17e+02    -1.61e+02
-1.70e+00    -1.13e+02    -9.25e+01    -1.10e+02
-1.50e+00    -7.83e+01    -6.88e+01    -7.58e+01
-1.30e+00    -4.43e+01    -4.52e+01    -4.17e+01
-1.10e+00    -1.02e+01    -2.15e+01    -7.67e+00
-9.00e-01    -9.69e-03    -1.18e+00    -7.81e-03
-7.00e-01    -2.83e-04    -5.70e-03    -8.42e-04
-5.00e-01    -1.35e-06    -4.53e-05    -1.00e-05
-3.00e-01    -1.31e-09    -3.74e-07    -8.58e-09
-1.00e-01    -2.92e-11    -3.00e-09    -3.64e-11
0.000e+00    -2.44e-11    -5.14e-10    -2.79e-11
|
|
[Model]         ip5b_io
Model_type         I/O
Polarity         Non-Inverting
Vinl= 0.8000v
Vinh= 2.000v
C_comp         5.00pF         5.00pF         5.00pF
|
|
[Voltage Range]       3.3v       3v       3.6v
[Pulldown]
|voltage         I(typ)         I(min)         I(max)
|
-3.30e+00    -5.21e+02    -3.65e+02    -5.18e+02
-3.10e+00    -4.69e+02    -3.30e+02    -4.67e+02
-2.90e+00    -4.18e+02    -2.94e+02    -4.16e+02
-2.70e+00    -3.67e+02    -2.59e+02    -3.65e+02
-2.50e+00    -3.16e+02    -2.23e+02    -3.14e+02
-2.30e+00    -2.65e+02    -1.88e+02    -2.63e+02
-2.10e+00    -2.14e+02    -1.52e+02    -2.12e+02
-1.90e+00    -1.63e+02    -1.17e+02    -1.61e+02
-1.70e+00    -1.13e+02    -9.25e+01    -1.10e+02
```