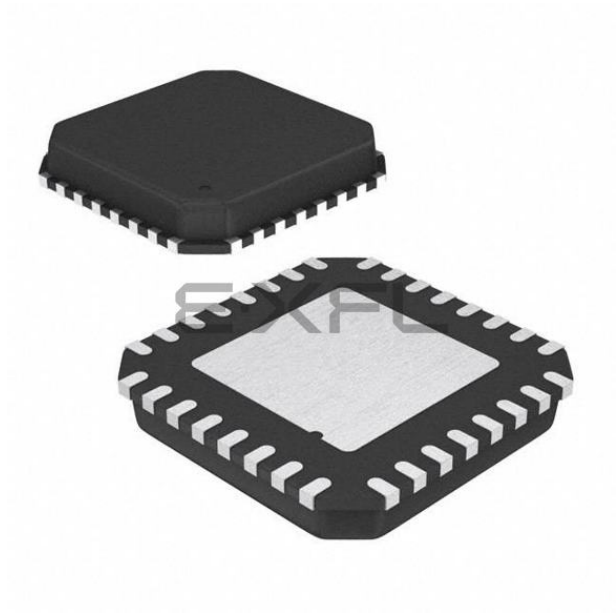

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny861a-mu

old value and program the new value) or to split the Erase and Write operations in two different operations. The Programming times for the different modes are shown in Table 5-1.

Table 5-1. EEPROM Mode Bits

EEPM1	EEPM0	Programming Time	Operation
0	0	3.4 ms	Erase and Write in one operation (Atomic Operation)
0	1	1.8 ms	Erase Only
1	0	1.8 ms	Write Only
1	1	–	Reserved for future use

When EEPE is set, any write to EEPMn will be ignored. During reset, the EEPMn bits will be reset to 0b00 unless the EEPROM is busy programming.

- **Bit 3 – EERIE: EEPROM Ready Interrupt Enable**

Writing EERIE to one enables the EEPROM Ready Interrupt if the I-bit in SREG is set. Writing EERIE to zero disables the interrupt. The EEPROM Ready Interrupt generates a constant interrupt when Non-volatile memory is ready for programming.

- **Bit 2 – EEMPE: EEPROM Master Program Enable**

The EEMPE bit determines whether writing EEPE to one will have effect or not.

When EEMPE is set, setting EEPE within four clock cycles will program the EEPROM at the selected address. If EEMPE is zero, setting EEPE will have no effect. When EEMPE has been written to one by software, hardware clears the bit to zero after four clock cycles.

- **Bit 1 – EEPE: EEPROM Program Enable**

The EEPROM Program Enable Signal EEPE is the programming enable signal to the EEPROM. When EEPE is written, the EEPROM will be programmed according to the EEPMn bits setting. The EEMPE bit must be written to one before a logical one is written to EEPE, otherwise no EEPROM write takes place. When the write access time has elapsed, the EEPE bit is cleared by hardware. When EEPE has been set, the CPU is halted for two cycles before the next instruction is executed.

- **Bit 0 – EERE: EEPROM Read Enable**

The EEPROM Read Enable Signal – EERE – is the read strobe to the EEPROM. When the correct address is set up in the EEAR Register, the EERE bit must be written to one to trigger the EEPROM read. The EEPROM read access takes one instruction, and the requested data is available immediately. When the EEPROM is read, the CPU is halted for four cycles before the next instruction is executed. The user should poll the EEPE bit before starting the read operation. If a write operation is in progress, it is neither possible to read the EEPROM, nor to change the EEAR Register.

6.1.3 Flash Clock – clk_{FLASH}

The Flash clock controls operation of the Flash interface. The Flash clock is usually active simultaneously with the CPU clock.

6.1.4 ADC Clock – clk_{ADC}

The ADC is provided with a dedicated clock domain. This allows halting the CPU and I/O clocks in order to reduce noise generated by digital circuitry. This gives more accurate ADC conversion results.

6.1.5 Fast Peripheral Clock – clk_{PCK}

Selected peripherals can be clocked at a frequency higher than the CPU core. The fast peripheral clock is generated by an on-chip PLL circuit.

6.1.6 PLL System Clock – clk_{ADC}

The PLL can also be used to generate a system clock. The clock signal can be prescaled to avoid overclocking the CPU.

6.2 Clock Sources

The device has the following clock source options, selectable by Flash Fuse bits as shown below. The clock from the selected source is input to the AVR clock generator, and routed to the appropriate modules.

Table 6-1. Device Clocking Options Select[1] vs. PB4 and PB5 Functionality

Device Clocking Option	CKSEL[3:0]	PB4	PB5
External Clock (see page 26)	0000	XTAL1	I/O
High-Frequency PLL Clock (see page 26)	0001	I/O	I/O
Calibrated Internal 8 MHz Oscillator (see page 28)	0010	I/O	I/O
Internal 128 kHz Oscillator (see page 29)	0011	I/O	I/O
Low-Frequency Crystal Oscillator (see page 29)	01xx	XTAL1	XTAL2
Crystal Oscillator / Ceramic Resonator 0.4...0.9 MHz (see page 30)	1000 1001	XTAL1	XTAL2
Crystal Oscillator / Ceramic Resonator 0.9...3.0 MHz (see page 30)	1010 1011	XTAL1	XTAL2
Crystal Oscillator / Ceramic Resonator 3...8 MHz (see page 30)	1100 1101	XTAL1	XTAL2
Crystal Oscillator / Ceramic Resonator 8...20 MHz (see page 30)	1110 1111	XTAL1	XTAL2

Note: 1. For all fuses “1” means unprogrammed and “0” means programmed.

The various choices for each clocking option is given in the following sections. When the CPU wakes up from Power-down or Power-save, the selected clock source is used to time the start-up, ensuring stable oscillator operation before instruction execution starts. When the CPU starts from reset, there is an additional delay allowing the power to reach a stable level before com-

Table 6-13. Clock Prescaler Select (Continued)

CLKPS3	CLKPS2	CLKPS1	CLKPS0	Clock Division Factor
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

10.2.2 Alternate Functions of Port B

The Port B pins with alternate function are shown in Table 10-6.

Table 10-6. Port B Pins Alternate Functions

Port Pin	Alternate Function
PB7	$\overline{\text{RESET}}$: Reset pin dW: debugWire I/O ADC10: ADC Input Channel 10 PCINT15: Pin Change Interrupt 0, Source 15
PB6	ADC9: ADC Input Channel 9 T0: Timer/Counter0 Clock Source INT0: External Interrupt 0 Input PCINT14: Pin Change Interrupt 0, Source 14
PB5	XTAL2: Crystal Oscillator Output CLKO: System Clock Output OC1D: Timer/Counter1 Compare Match D Output ADC8: ADC Input Channel 8 PCINT13: Pin Change Interrupt 0, Source 13
PB4	XTAL1: Crystal Oscillator Input CLKI: External Clock Input $\overline{\text{OC1D}}$: Inverted Timer/Counter1 Compare Match D Output ADC7: ADC Input Channel 7 PCINT12: Pin Change Interrupt 0, Source 12
PB3	OC1B: Timer/Counter1 Compare Match B Output PCINT11: Pin Change Interrupt 0, Source 11
PB2	USCK: USI Clock (Three Wire Mode) SCL : USI Clock (Two Wire Mode) $\overline{\text{OC1B}}$: Inverted Timer/Counter1 Compare Match B Output PCINT10: Pin Change Interrupt 0, Source 10
PB1	DO: USI Data Output (Three Wire Mode) OC1A: Timer/Counter1 Compare Match A Output PCINT9: Pin Change Interrupt 1, Source 9
PB0	DI: USI Data Input (Three Wire Mode) SDA: USI Data Input (Two Wire Mode) $\overline{\text{OC1A}}$: Inverted Timer/Counter1 Compare Match A Output PCINT8: Pin Change Interrupt 1, Source 8

- **Port B, Bit 7 – $\overline{\text{RESET}}$/dW/ADC10/PCINT15**
  - RESET, Reset pin: When the RSTDISBL Fuse is programmed, this pin functions as a normal I/O pin, and the part will have to rely on Power-on Reset and Brown-out Reset as its reset sources. When the RSTDISBL Fuse is unprogrammed, the reset circuitry is connected to the pin, and the pin can not be used as an I/O pin.
  - If PB7 is used as a reset pin, DDB7, PORTB7 and PINB7 will all read 0.
  - dW: When the debugWIRE Enable (DWEN) Fuse is programmed and Lock bits are unprogrammed, the RESET port pin is configured as a wire-AND (open-drain) bi-directional I/O pin with pull-up enabled and becomes the communication gateway between target and emulator.

- ADC10: ADC input Channel 10. Note that ADC input channel 10 uses analog power.
- PCINT15: Pin Change Interrupt source 15.

- **Port B, Bit 6 – ADC9/T0/INT0/PCINT14**
  - ADC9: ADC input Channel 9. Note that ADC input channel 9 uses analog power.
  - T0: Timer/Counter0 counter source.
  - INT0: The PB6 pin can serve as an External Interrupt source 0.
  - PCINT14: Pin Change Interrupt source 14.

- **Port B, Bit 5 – XTAL2/CLKO/ADC8/PCINT13**
  - XTAL2: Chip clock Oscillator pin 2. Used as clock pin for crystal Oscillator or Low-frequency crystal Oscillator. When used as a clock pin, the pin can not be used as an I/O pin.
  - CLKO: The divided system clock can be output on the PB5 pin, if the CKOUT Fuse is programmed, regardless of the PORTB5 and DDB5 settings. It will also be output during reset.
  - OC1D Output Compare Match output: The PB5 pin can serve as an external output for the Timer/Counter1 Compare Match D when configured as an output (DDA1 set). The OC1D pin is also the output pin for the PWM mode timer function.
  - ADC8: ADC input Channel 8. Note that ADC input channel 8 uses analog power.
  - PCINT13: Pin Change Interrupt source 13.

- **Port B, Bit 4 – XTAL1/CLKI/OC1B/ADC7/PCINT12**
  - XTAL1/CLKI: Chip clock Oscillator pin 1. Used for all chip clock sources except internal calibrated oscillator. When used as a clock pin, the pin can not be used as an I/O pin.
  - $\overline{\text{OC1D}}$: Inverted Output Compare Match output: The PB4 pin can serve as an external output for the Timer/Counter1 Compare Match D when configured as an output (DDA0 set). The $\overline{\text{OC1D}}$ pin is also the inverted output pin for the PWM mode timer function.
  - ADC7: ADC input Channel 7. Note that ADC input channel 7 uses analog power.
  - PCINT12: Pin Change Interrupt source 12.

- **Port B, Bit 3 – OC1B/PCINT11**
  - OC1B, Output Compare Match output: The PB3 pin can serve as an external output for the Timer/Counter1 Compare Match B. The PB3 pin has to be configured as an output (DDB3 set (one)) to serve this function. The OC1B pin is also the output pin for the PWM mode timer function.
  - PCINT11: Pin Change Interrupt source 11.

- **Port B, Bit 2 – SCK/USCK/SCL/$\overline{\text{OC1B}}$/PCINT10**
  - USCK: Three-wire mode Universal Serial Interface Clock.
  - SCL: Two-wire mode Serial Clock for USI Two-wire mode.
  - $\overline{\text{OC1B}}$: Inverted Output Compare Match output: The PB2 pin can serve as an external output for the Timer/Counter1 Compare Match B when configured as an output (DDB2 set). The $\overline{\text{OC1B}}$ pin is also the inverted output pin for the PWM mode timer function.
  - PCINT10: Pin Change Interrupt source 10.

Table 10-8. Overriding Signals for Alternate Functions in PB[3:0]

Signal Name	PB3/OC1B/ PCINT11	PB2/SCK/USCK/SCL/$\overline{OC1B}$/PCINT10	PB1/MISO/DO/OC1A/ PCINT9	PB0/MOSI/DI/SDA/ $\overline{OC1A}$/PCINT8
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	USI_TWO_WIRE • $\overline{USIPOS}$	0	USI_TWO_WIRE • $\overline{USIPOS}$
DDOV	0	(USI_SCL_HOLD + $\overline{PORTB2}$) • DDB2 • $\overline{USIPOS}$	0	($\overline{SDA}$ + $\overline{PORTB0}$) • DDB0 • $\overline{USIPOS}$
PVOE	OC1B Enable	$\overline{OC1B\ Enable}$ + $\overline{USIPOS}$ • USI_TWO_WIRE • DDB2	$\overline{OC1A\ Enable}$ + $\overline{USIPOS}$ • USI_THREE_WIRE	$\overline{OC1A\ Enable}$ + (USI_TWO_WIRE • DDB0 • $\overline{USIPOS}$)
PVOV	OC1B	OC1B	$\overline{OC1A}$ + (DO • $\overline{USIPOS}$)	OC1A
PTOE	0	USITC • $\overline{USIPOS}$	0	0
DIEOE	PCINT11 • PCIE	PCINT10 • PCIE + USISIE • $\overline{USIPOS}$	PCINT9 • PCIE	PCINT8 • PCIE + (USISIE • $\overline{USIPOS}$)
DIEOV	0	0	0	0
DI	PCINT11	USCK/SCL/PCINT10	PCINT9	DI/SDA/PCINT8
AIO				

Note: 1. INTRC means that one of the internal oscillators is selected (by the CKSEL fuses), EXTCK means that external clock is selected (by the CKSEL fuses).

10.3 Register Description

10.3.1 MCUCR – MCU Control Register

Bit	7	6	5	4	3	2	1	0	
0x35 (0x55)	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	MCUCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 6 – PUD: Pull-up Disable**

When this bit is written to one, the pull-ups in the I/O ports are disabled even if the DDxn and PORTxn Registers are configured to enable the pull-ups ({DDxn, PORTxn} = 0b01). See “Configuring the Pin” on page 55 for more details about this feature.

10.3.2 PORTA – Port A Data Register

Bit	7	6	5	4	3	2	1	0	
0x1B (0x3B)	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	PORTA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

10.3.3 DDRA – Port A Data Direction Register

Bit	7	6	5	4	3	2	1	0	
0x1A (0x3A)	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

For actual placement of the I/O pins, refer to “Pinout ATtiny261A/461A/861A” on page 2. The device-specific I/O register and bit locations are listed in the “Register Description” on page 111.

12.2.1 Speed

The maximum speed of the Timer/Counter1 is 64 MHz. However, if a supply voltage below 2.7 volts is used, it is recommended to use the Low Speed Mode (LSM), because the Timer/Counter1 is not running fast enough on low voltage levels. In the Low Speed Mode the fast peripheral clock is scaled down to 32 MHz. For more details about the Low Speed Mode, see “PLLCSR – PLL Control and Status Register” on page 119.

12.2.2 Accuracy

The Timer/Counter1 is a 10-bit Timer/Counter module that can alternatively be used as an 8-bit Timer/Counter. The Timer/Counter1 registers are basically 8-bit registers, but on top of that there is a 2-bit High Byte Register (TC1H) that can be used as a common temporary buffer to access the two MSBs of the 10-bit Timer/Counter1 registers by the AVR CPU via the 8-bit data bus, if the 10-bit accuracy is used. Whereas, if the two MSBs of the 10-bit registers are written to zero the Timer/Counter1 is working as an 8-bit Timer/Counter. When reading the low byte of any 8-bit register the two MSBs are written to the TC1H register, and when writing the low byte of any 8-bit register the two MSBs are written from the TC1H register. Special procedures must be followed when accessing the 10-bit Timer/Counter1 values via the 8-bit data bus. These procedures are described in the section “Accessing 10-Bit Registers” on page 107.

12.2.3 Registers

The Timer/Counter (TCNT1) and Output Compare Registers (OCR1A, OCR1B, OCR1C and OCR1D) are 8-bit registers that are used as a data source to be compared with the TCNT1 contents. The OCR1A, OCR1B and OCR1D registers determine the action on the OC1A, OC1B and OC1D pins and they can also generate the compare match interrupts. The OCR1C holds the Timer/Counter TOP value, i.e. the clear on compare match value. The Timer/Counter1 High Byte Register (TC1H) is a 2-bit register that is used as a common temporary buffer to access the MSB bits of the Timer/Counter1 registers, if the 10-bit accuracy is used.

Interrupt request (overflow TOV1, and compare matches OCF1A, OCF1B, OCF1D and fault protection FPF1) signals are visible in the Timer Interrupt Flag Register (TIFR) and Timer/Counter1 Control Register D (TCCR1D). The interrupts are individually masked with the Timer Interrupt Mask Register (TIMSK) and the FPIE1 bit in the Timer/Counter1 Control Register D (TCCR1D).

Control signals are found in the Timer/Counter Control Registers TCCR1A, TCCR1B, TCCR1C, TCCR1D and TCCR1E.

12.2.4 Synchronization

In asynchronous clocking mode the Timer/Counter1 and the prescaler allow running the CPU from any clock source while the prescaler is operating on the fast peripheral clock (PCK) having frequency of 64 MHz (or 32 MHz in Low Speed Mode). This is possible because there is a synchronization boundary between the CPU clock domain and the fast peripheral clock domain. Figure 12-2 shows Timer/Counter 1 synchronization register block diagram and describes synchronization delays in between registers. Note that all clock gating details are not shown in the figure.

The Timer/Counter1 register values go through the internal synchronization registers, which cause the input synchronization delay, before affecting the counter operation. The registers TCCR1A, TCCR1B, TCCR1C, TCCR1D, OCR1A, OCR1B, OCR1C and OCR1D can be read

Figure 12-17. Timer/Counter Timing Diagram, Setting of OCF1x, with Prescaler ($f_{clkT1}/8$)

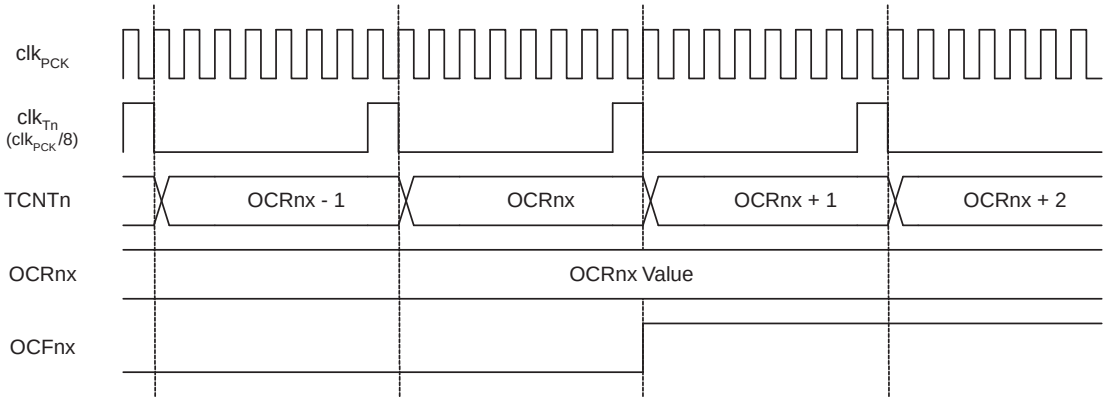
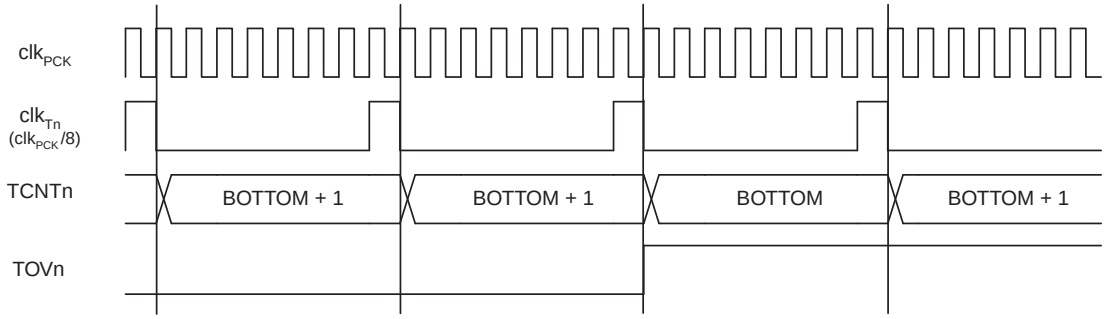


Figure 12-18 shows the setting of TOV1 in Phase and Frequency Correct PWM Mode.

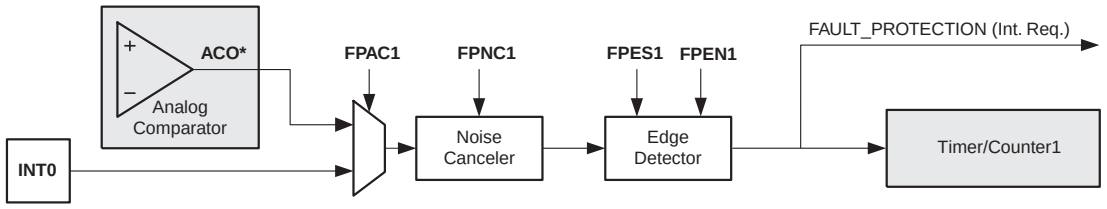
Figure 12-18. Timer/Counter Timing Diagram, with Prescaler ($f_{clkT1}/8$)



12.10 Fault Protection Unit

The Timer/Counter1 incorporates a Fault Protection unit, which can be set to disable the PWM output pins when an external event is triggered. The external signal indicating an event can be applied via the external interrupt INT0 pin or, alternatively, via the analog-comparator unit. The Fault Protection unit is illustrated in Figure 12-19. The elements of the block diagram that are not directly a part of the Fault Protection unit are gray shaded.

Figure 12-19. Fault Protection Unit Block Diagram



Fault Protection mode is enabled by setting the Fault Protection Enable (FPEN1) bit and triggered by a change in logic level at external interrupt pin (INT0). Alternatively, fault protection mode can be triggered by the Analog Comparator Output (ACO).

When Fault Protection is triggered, the COM1x bits are cleared, Output Comparators are disconnected from the PWM output pins and PORTB register bits are connected to the PWM output

applied to the AREF pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

14.2.4 DIDR1 – Digital Input Disable Register 1

Bit	7	6	5	4	3	2	1	0	
0x02 (0x22)	ADC10D	ADC9D	ADC8D	ADC7D	–	–	–	–	DIDR1
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:4 – ADC10D:ADC7D: ADC[10:7] Digital Input Disable**

When this bit is written logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[10:7] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot 512}{V_{REF}} \cdot GAIN$$

where V_{POS} is the voltage on the positive input pin, V_{NEG} the voltage on the negative input pin, and V_{REF} the selected voltage reference. The result is presented in two's complement form, from 0x200 (-512d) through 0x000 (+0d) to 0x1FF (+511d). The GAIN is either 1x, 8x, 20x or 32x.

However, if the signal is not bipolar by nature (9 bits + sign as the 10th bit), this scheme loses one bit of the converter dynamic range. Then, if the user wants to perform the conversion with the maximum dynamic range, the user can perform a quick polarity check of the result and use the unipolar differential conversion with selectable differential input pair. When the polarity check is performed, it is sufficient to read the MSB of the result (ADC9 in ADCH). If the bit is one, the result is negative, and if this bit is zero, the result is positive.

15.12 Temperature Measurement

The temperature measurement is based on an on-chip temperature sensor that is coupled to a single ended ADC11 channel. Selecting the ADC11 channel by writing the MUX[5:0] bits in ADMUX register to "111111" enables the temperature sensor. The internal 1.1V voltage reference must also be selected for the ADC voltage reference source in the temperature sensor measurement. When the temperature sensor is enabled, the ADC converter can be used in single conversion mode to measure the voltage over the temperature sensor.

The measured voltage has a linear relationship to the temperature as described in Table 15-2 The sensitivity is approximately 1 LSB / °C and the accuracy depends on the method of user calibration. Typically, the measurement accuracy after a single temperature calibration is ±10°C, assuming calibration at room temperature. Better accuracies are achieved by using two temperature points for calibration.

Table 15-2. Temperature vs. Sensor Output Voltage (Typical Case)

Temperature	**-40 °C**	**+25 °C**	**+85 °C**
ADC	230 LSB	300 LSB	370 LSB

The values described in Table 15-2 are typical values. However, due to process variation the temperature sensor output voltage varies from one chip to another. To be capable of achieving more accurate results the temperature measurement can be calibrated in the application software. The sofware calibration can be done using the formula:

$$T = k * [(ADCH << 8) \mid ADCL] + T_{OS}$$

where ADCH and ADCL are the ADC data registers, k is the fixed slope coefficient and T_{OS} is the temperature sensor offset. Typically, k is very close to 1.0 and in single-point calibration the coefficient may be omitted. Where higher accuracy is required the slope coefficient should be evaluated based on measurements at two temperatures.

trigger signal. If ADEN in ADCSRA is set, this will start a conversion. Switching to Free Running mode (ADTS[2:0]=0) will not cause a trigger event, even if the ADC Interrupt Flag is set.

Table 15-6. ADC Auto Trigger Source Selections

ADTS2	ADTS1	ADTS0	Trigger Source
0	0	0	Free Running mode
0	0	1	Analog Comparator
0	1	0	External Interrupt Request 0
0	1	1	Timer/Counter0 Compare Match A
1	0	0	Timer/Counter0 Overflow
1	0	1	Timer/Counter0 Compare Match B
1	1	0	Timer/Counter1 Overflow
1	1	1	Watchdog Interrupt Request

15.13.5 DIDR0 – Digital Input Disable Register 0

Bit	7	6	5	4	3	2	1	0	
0x01 (0x21)	ADC6D	ADC5D	ADC4D	ADC3D	AREFD	ADC2D	ADC1D	ADC0D	DIDR0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:4, 2:0 – ADC6D:ADC0D: ADC[6:0] Digital Input Disable**

When this bit is written logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[6:0] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

- **Bit 3 – AREFD: AREF Digital Input Disable**

When this bit is written logic one, the digital input buffer on the AREF pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the AREF pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

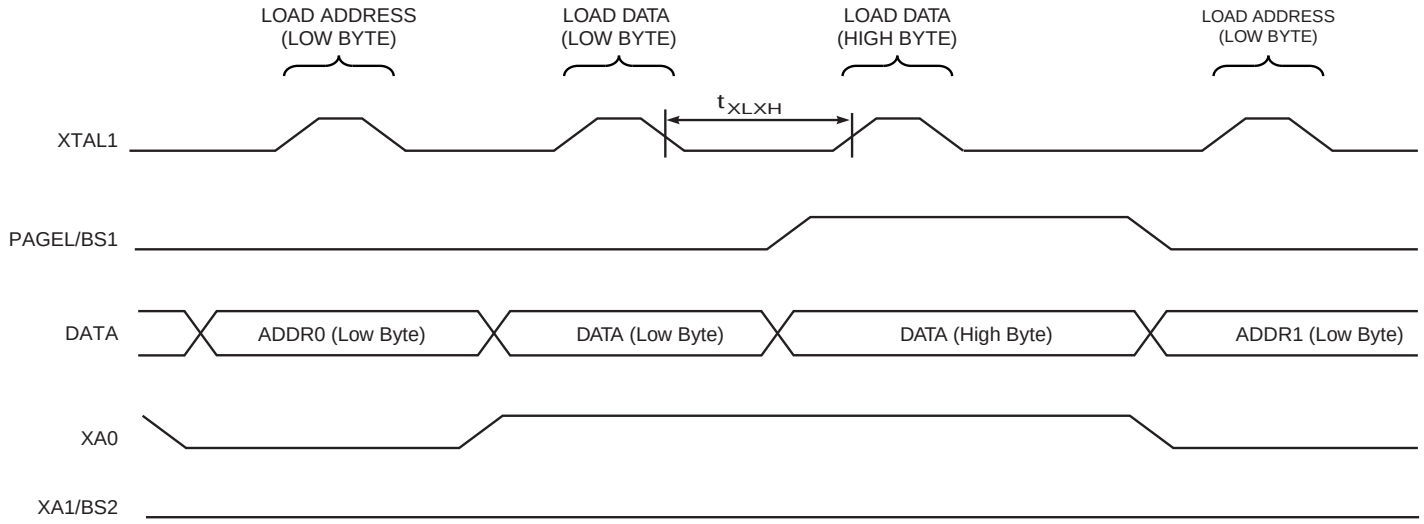
15.13.6 DIDR1 – Digital Input Disable Register 1

Bit	7	6	5	4	3	2	1	0	
0x02 (0x22)	ADC10D	ADC9D	ADC8D	ADC7D	–	–	–	–	DIDR1
Read/Write	R/W	R/W	R/W	R/W	R	R	R	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bits 7:4 – ADC10D:ADC7D: ADC[10:7] Digital Input Disable**

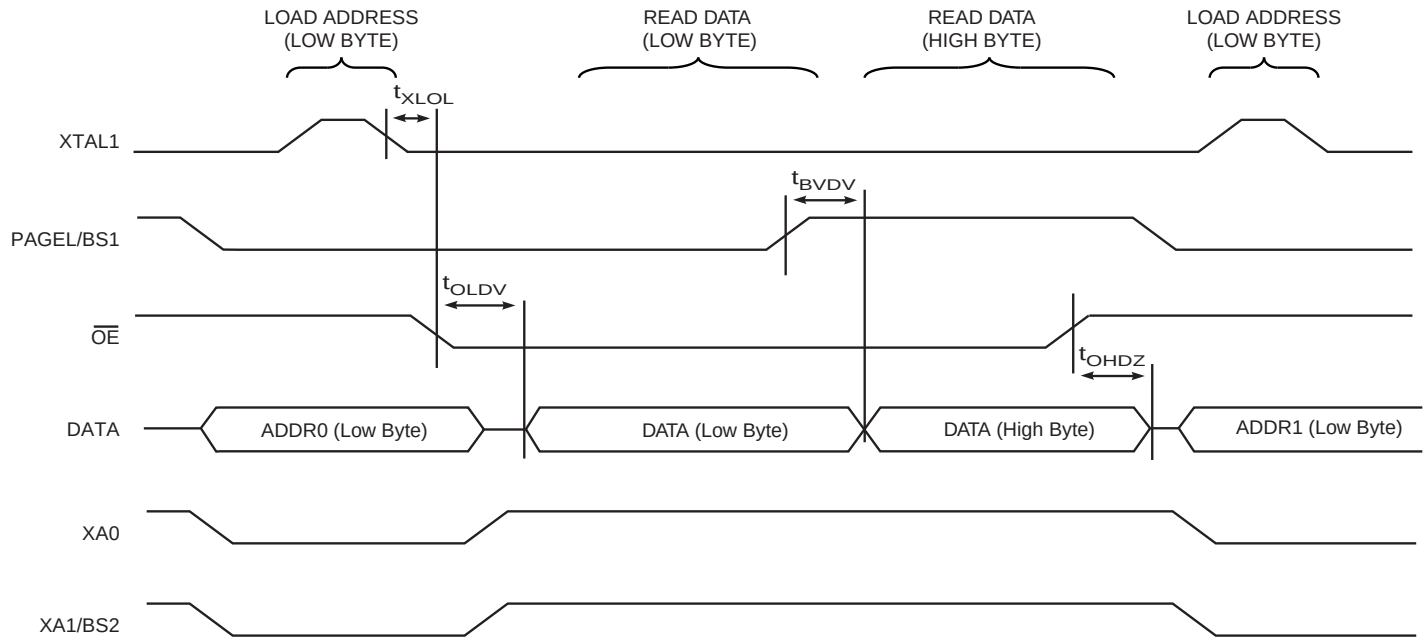
When this bit is written logic one, the digital input buffer on the corresponding ADC pin is disabled. The corresponding PIN register bit will always read as zero when this bit is set. When an analog signal is applied to the ADC[10:7] pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

Figure 19-6. Parallel Programming Timing, Loading Sequence with Timing Requirements



Note: The timing requirements shown in Figure 19-5 (i.e., t_{DVXH}, t_{XHXL}, and t_{XLDX}) also apply to loading operation.

Figure 19-7. Parallel Programming Timing, Reading Sequence (within the Same Page) with Timing Requirements



Note: The timing requirements shown in Figure 19-5 (i.e., t_{DVXH}, t_{XHXL}, and t_{XLDX}) also apply to reading operation.

Table 19-12. Parallel Programming Characteristics, V_{CC} = 5V ± 10%

Symbol	Parameter	Min	Typ	Max	Units
V_{PP}	Programming Enable Voltage	11.5		12.5	V
I_{PP}	Programming Enable Current			250	µA
t_{DVXH}	Data and Control Valid before XTAL1 High	67			ns

20.2 ATtiny261A

20.2.1 Current Consumption in Active Mode

Figure 20-1. Active Supply Current vs. Low Frequency (0.1 - 1.0 MHz)

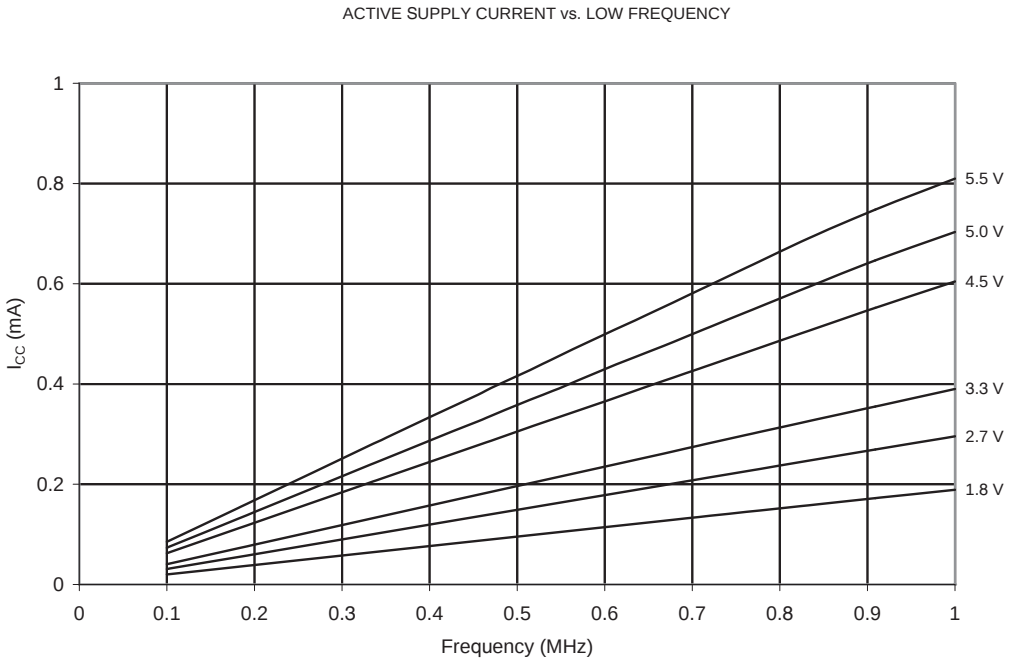


Figure 20-2. Active Supply Current vs. Frequency (1 - 20 MHz)

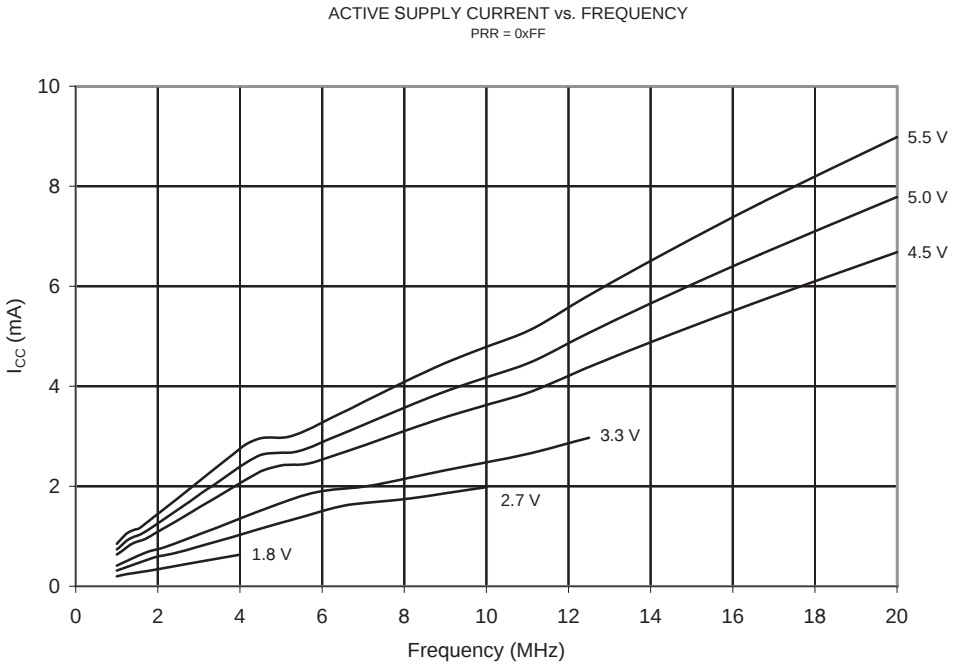


Figure 20-58. Idle Supply Current vs. Frequency (1 - 20 MHz)

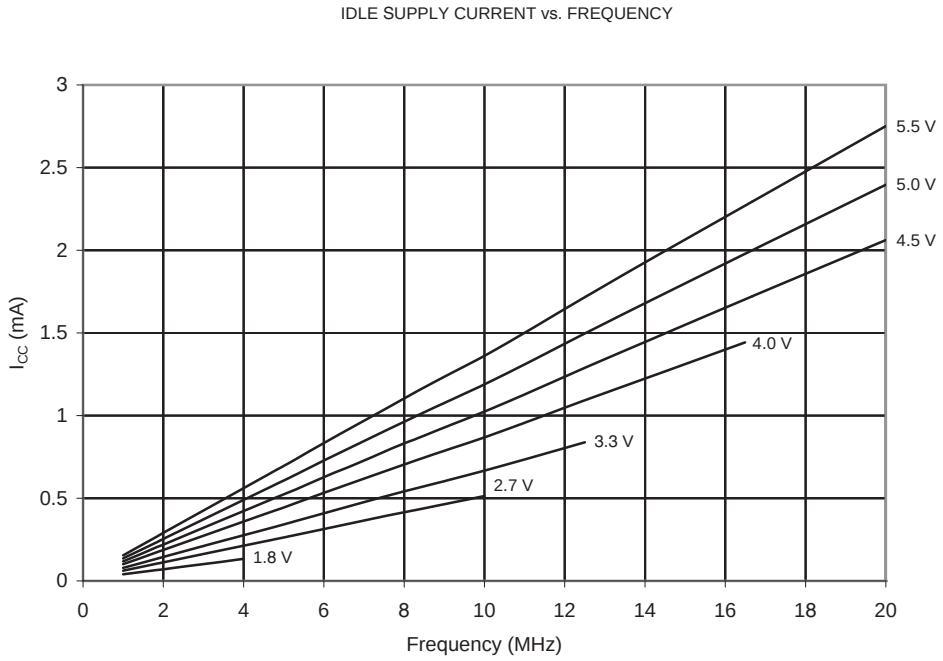


Figure 20-59. Idle Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 8 MHz)

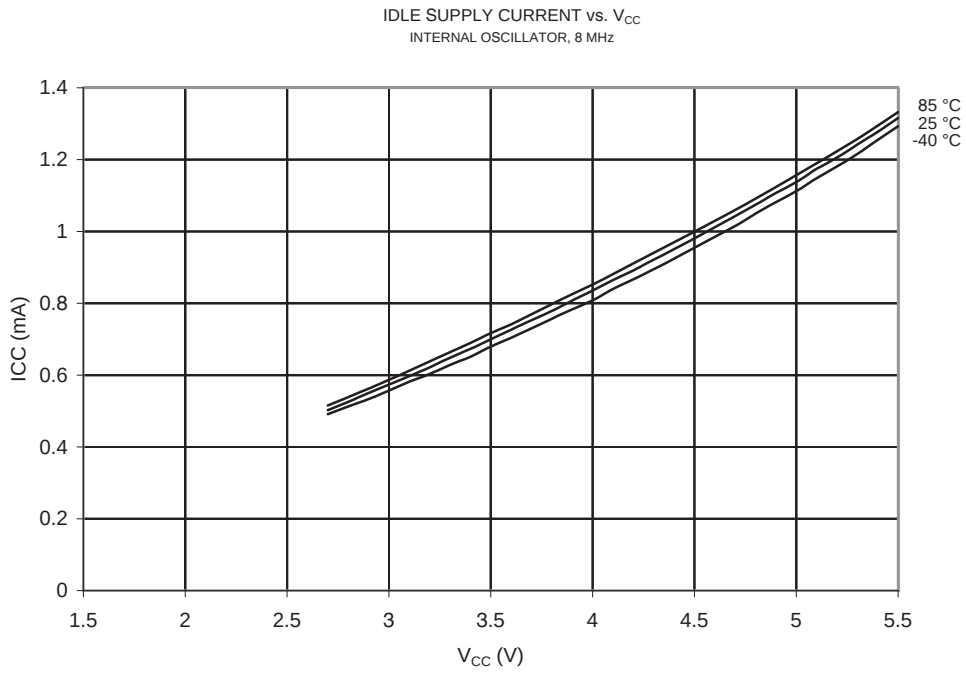


Figure 20-72. Pull-Up Resistor Current vs. Input Voltage (I/O Pin, V_{CC} = 3V)

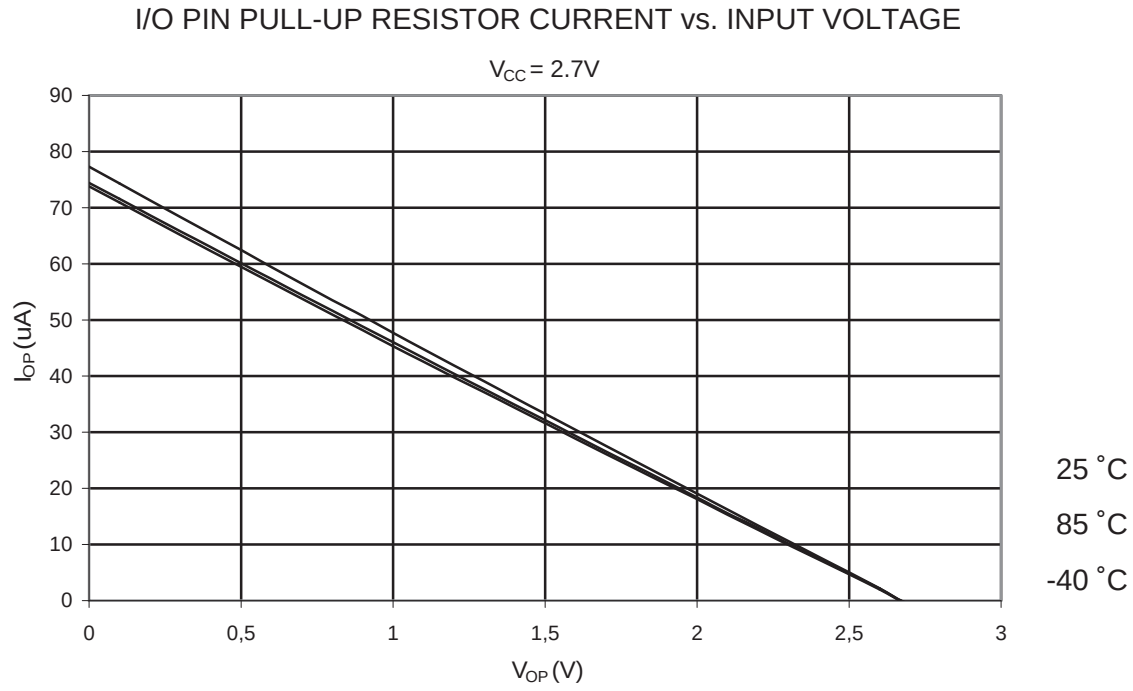


Figure 20-73. Pull-Up Resistor Current vs. Input Voltage (I/O Pin, V_{CC} = 5V)

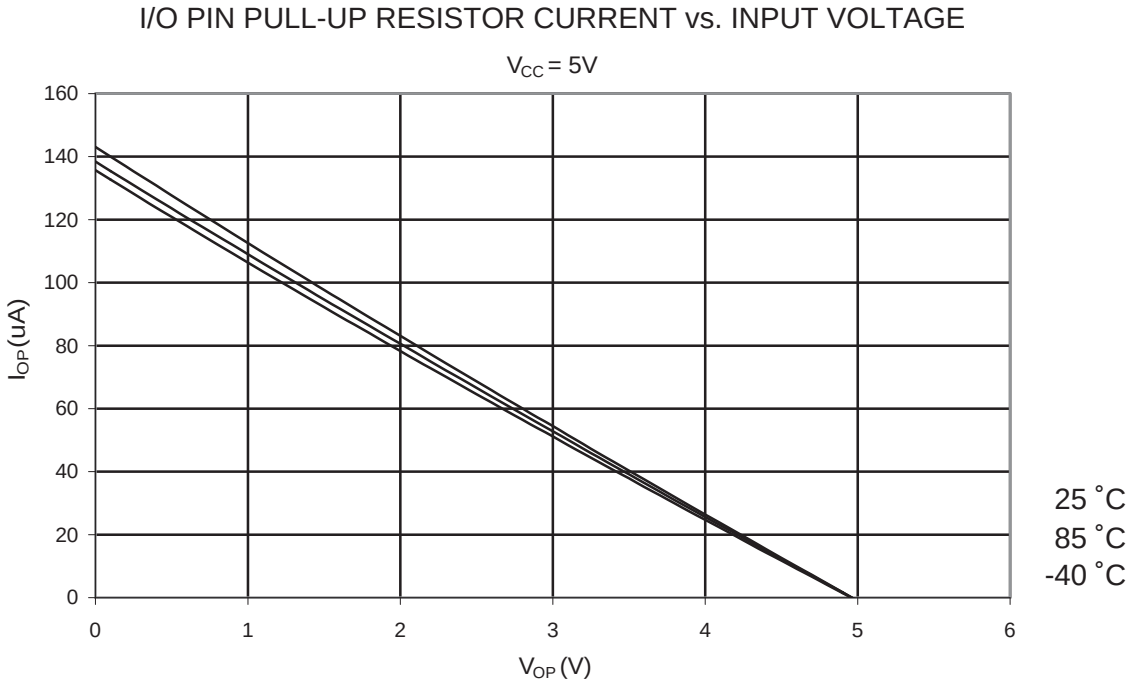
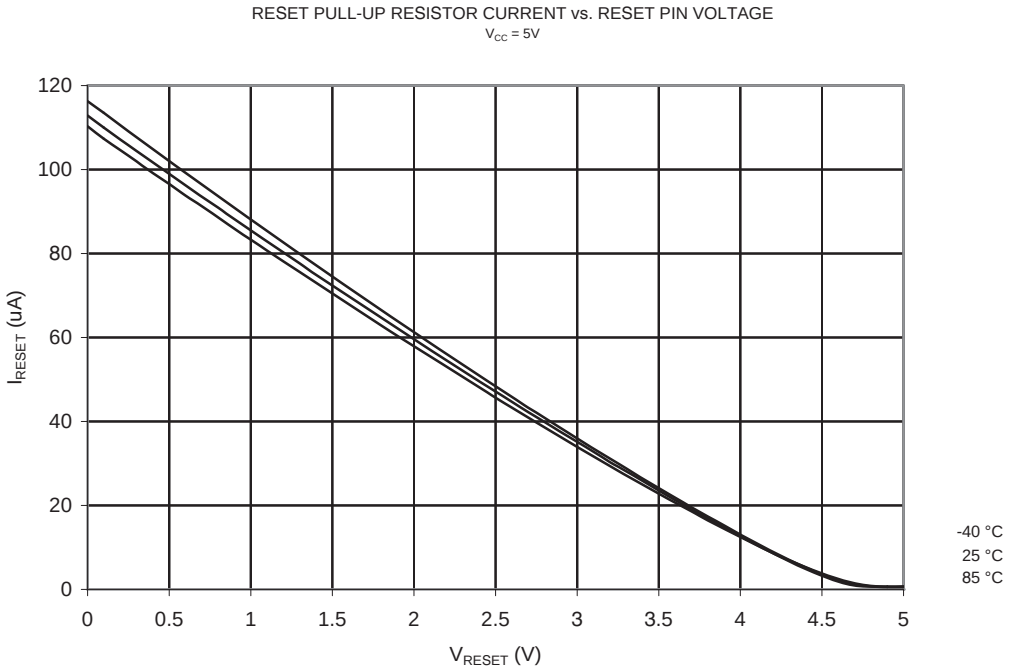


Figure 20-76. Pull-Up Resistor Current vs. Input Voltage (Reset Pin, V_{CC} = 5V)



20.3.7 Output Driver Strength

Figure 20-77. V_{OL}: Output Voltage vs. Sink Current (I/O Pin, V_{CC} = 1.8V)

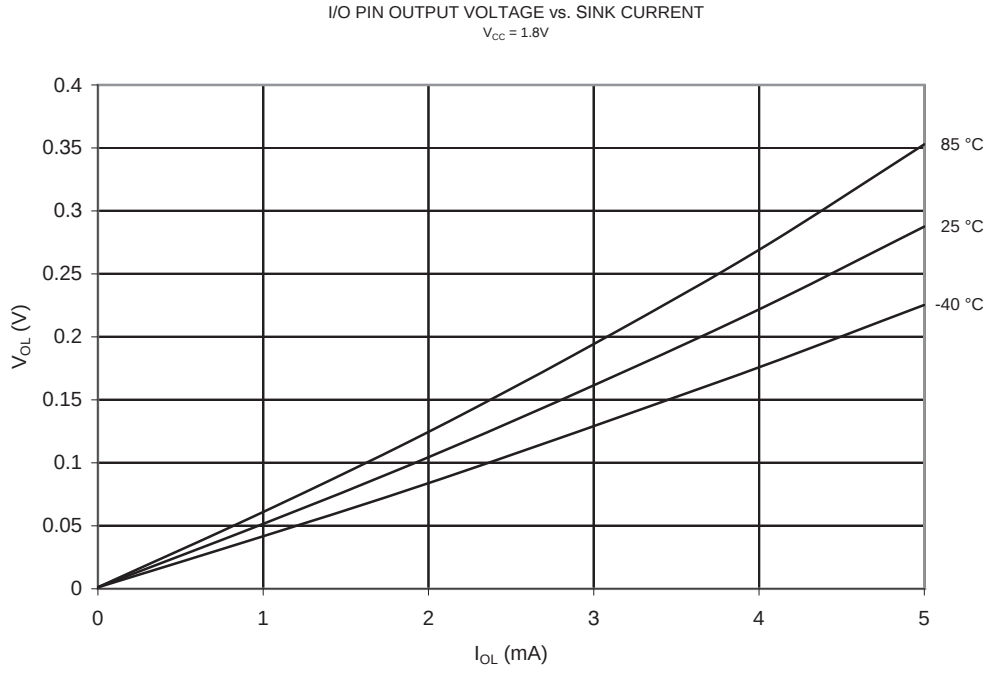
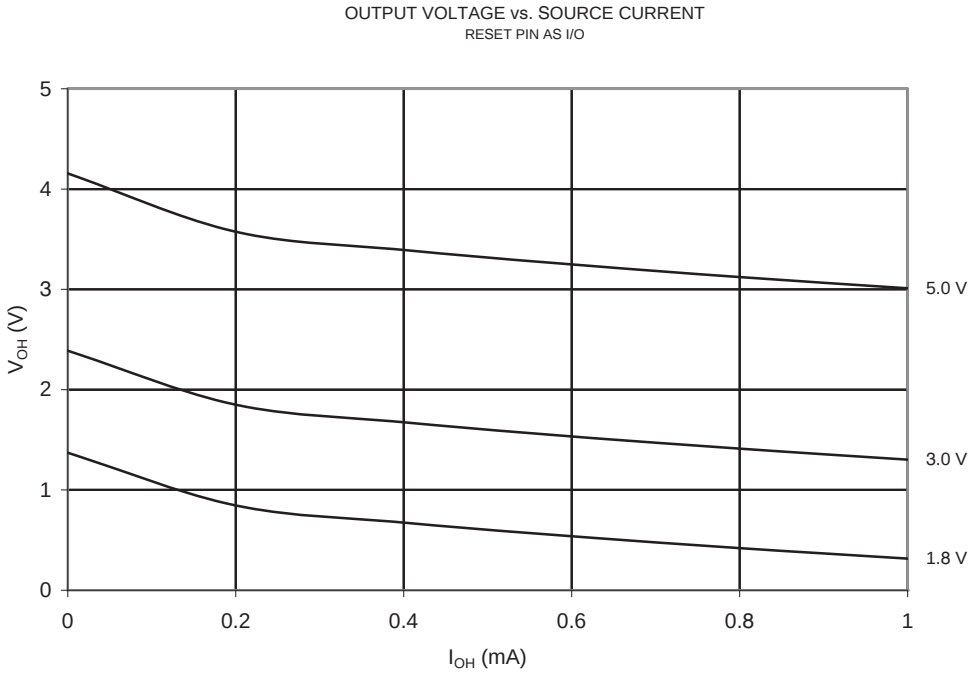


Figure 20-86. V_{OH}: Output Voltage vs. Source Current (Reset Pin as I/O, T = 25°C)



20.3.8 Input Thresholds and Hysteresis

Figure 20-87. V_{IH}: Input Threshold Voltage vs. V_{CC} (I/O Pin, Read as '1')

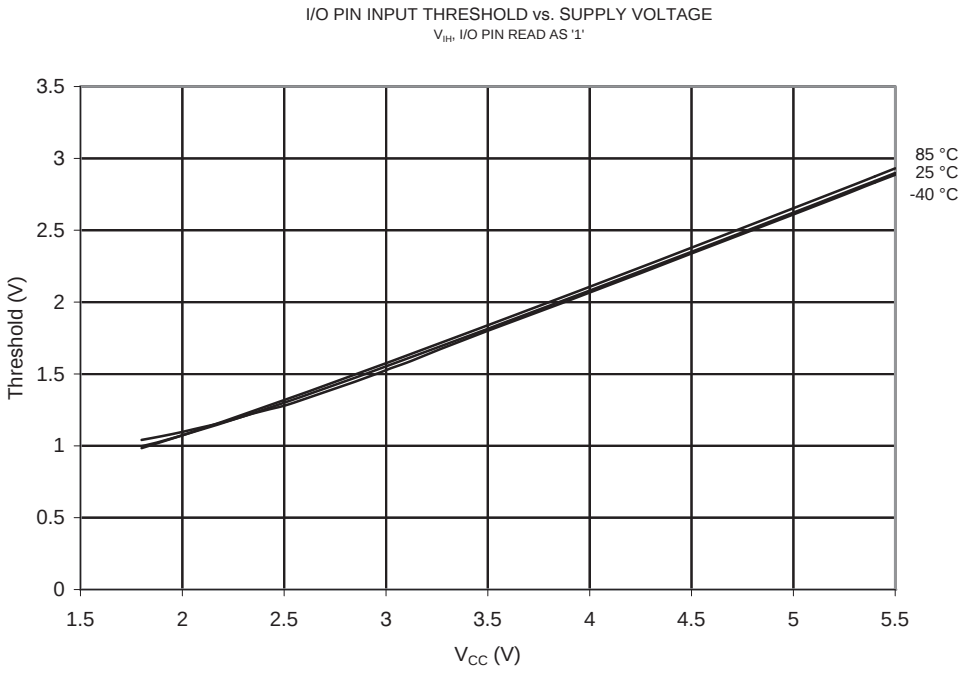
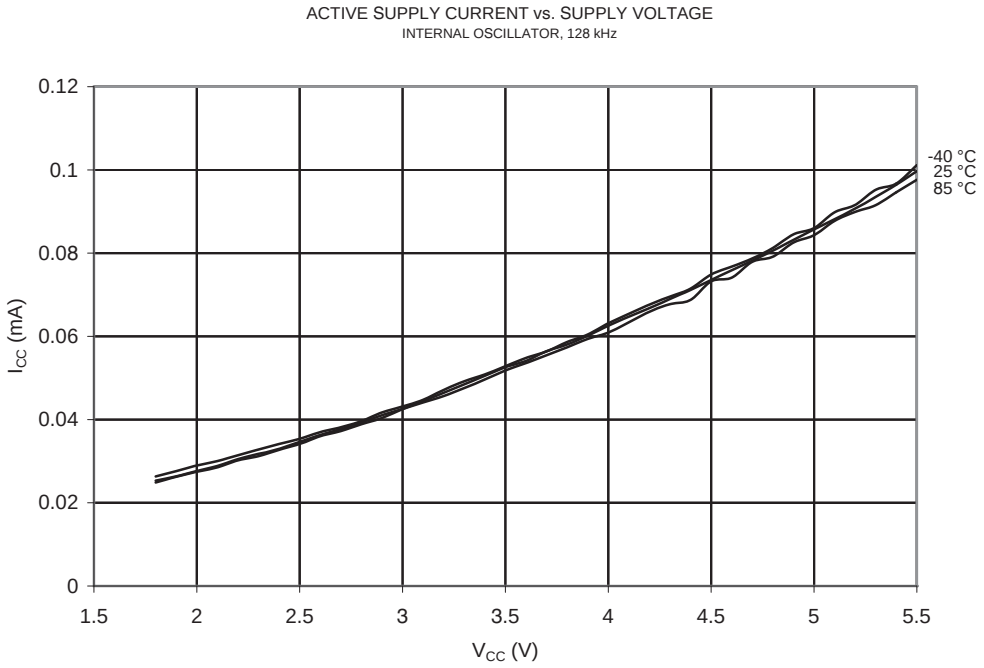
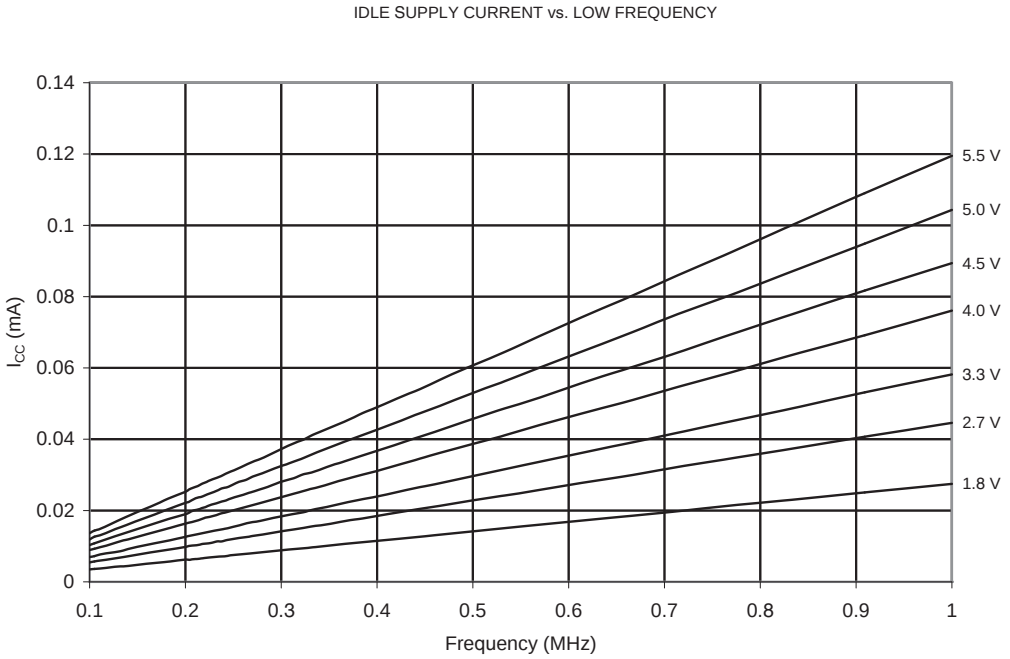


Figure 20-107. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 128 kHz)



20.4.2 Current Consumption in Idle Mode

Figure 20-108. Idle Supply Current vs. Low Frequency (0.1 - 1.0 MHz)



Mnemonics	Operands	Description	Operation	Flags	#Clocks
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(z) ← R1:R0	None	
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

23.3 ATtiny861A

Speed (MHz)	Power Supply	Ordering Code [1]	Package [2]	Operational Range
20	1.8 – 5.5V	ATtiny861A-MU ATtiny861A-MUR ATtiny861A-PU ATtiny861A-SU ATtiny861A-SUR ATtiny861A-XU ATtiny861A-XUR	32M1-A 32M1-A 20P3 20S2 20S2 20X 20X	Industrial (-40°C to +85°C) [3]

Notes: 1. Code indicators:

- U: matte tin
- R: tape & reel

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
3. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

Package Type	
32M1-A	32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S2	20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline Package (TSSOP)