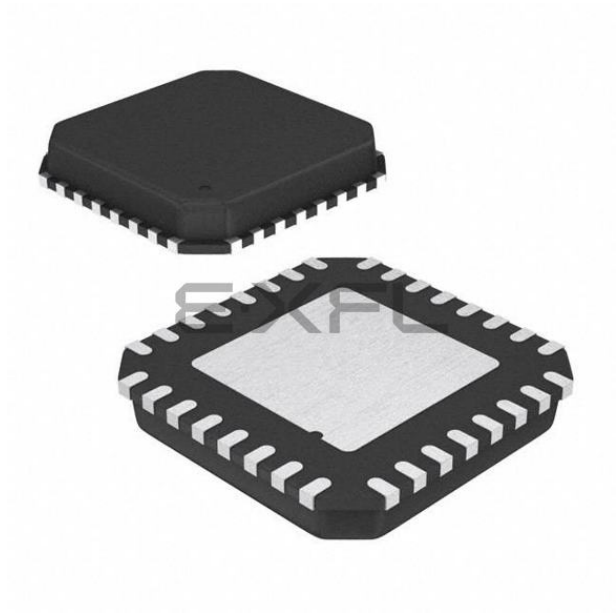

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	USI
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	16
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny861a-mur

4.3.1 SREG – AVR Status Register

Bit	7	6	5	4	3	2	1	0	
0x3F (0x5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – I: Global Interrupt Enable**

The Global Interrupt Enable bit must be set for the interrupts to be enabled. The individual interrupt enable control is then performed in separate control registers. If the Global Interrupt Enable Register is cleared, none of the interrupts are enabled independent of the individual interrupt enable settings. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts. The I-bit can also be set and cleared by the application with the SEI and CLI instructions, as described in the instruction set reference.

- **Bit 6 – T: Bit Copy Storage**

The Bit Copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T-bit as source or destination for the operated bit. A bit from a register in the Register File can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the Register File by the BLD instruction.

- **Bit 5 – H: Half Carry Flag**

The Half Carry Flag H indicates a Half Carry in some arithmetic operations. Half Carry is useful in BCD arithmetic. See the “Instruction Set Description” for detailed information.

- **Bit 4 – S: Sign Bit, S = N ⊕ V**

The S-bit is always an exclusive or between the Negative Flag N and the Two’s Complement Overflow Flag V. See the “Instruction Set Description” for detailed information.

- **Bit 3 – V: Two’s Complement Overflow Flag**

The Two’s Complement Overflow Flag V supports two’s complement arithmetics. See the “Instruction Set Description” for detailed information.

- **Bit 2 – N: Negative Flag**

The Negative Flag N indicates a negative result in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

- **Bit 1 – Z: Zero Flag**

The Zero Flag Z indicates a zero result in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

- **Bit 0 – C: Carry Flag**

The Carry Flag C indicates a carry in an arithmetic or logic operation. See the “Instruction Set Description” for detailed information.

Table 10-4 and Table 10-5 relate the alternate functions of Port A to the overriding signals shown in Figure 10-5 on page 60.

Table 10-4. Overriding Signals for Alternate Functions in PA[7:4]

Signal Name	PA7/ADC6/AIN0/ PCINT7	PA6/ADC5/AIN1/ PCINT6	PA5/ADC4/AIN2/ PCINT5	PA4/ADC3/ICP0/ PCINT4
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	0	0	0
DDOV	0	0	0	0
PVOE	0	0	0	0
PVOV	0	0	0	0
PTOE	0	0	0	0
DIEOE	PCINT7 • PCIE + ADC6D	PCINT6 • PCIE + ADC5D	PCINT5 • PCIE + ADC4D	PCINT4 • PCIE + ADC3D
DIEOV	$\overline{\text{ADC6D}}$	$\overline{\text{ADC5D}}$	$\overline{\text{ADC4D}}$	$\overline{\text{ADC3D}}$
DI	PCINT7	PCINT6	PCINT5	ICP0/PCINT4
AIO	ADC6, AIN0	ADC5, AIN1	ADC4, AIN2	ADC3

Table 10-5. Overriding Signals for Alternate Functions in PA[3:0]

Signal Name	PA3/AREF/ PCINT3	PA2/ADC2/INT1/ USCK/SCL/PCINT2	PA1/ADC1/DO/ PCINT1	PA0/ADC0/DI/SDA/ PCINT0
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	USI_TWO_WIRE • USIPOS	0	USI_TWO_WIRE • USIPOS
DDOV	0	(USI_SCL_HOLD + $\overline{\text{PORTB2}}$) • DDB2 • USIPOS	0	($\overline{\text{SDA}}$ + $\overline{\text{PORTB0}}$) • DDRB0 • USIPOS
PVOE	0	USI_TWO_WIRE • DDRB2	USI_THREE_WIRE • USIPOS	USI_TWO_WIRE • DDRB0 • USIPOS
PVOV	0	0	DO • USIPOS	0
PTOE	0	USI_PTOE • USIPOS	0	0
DIEOE	PCINT3 • PCIE	PCINT2 • PCIE + INT1 + ADC2D + USISIE • USIPOS	PCINT1 • PCIE + ADC1D	PCINT0 • PCIE + ADC0D + USISIE • USIPOS
DIEOV	0	$\overline{\text{ADC2D}}$	ADC1D	ADC0D
DI	PCINT3	USCK/SCL/INT1/ PCINT2	PCINT1	DI/SDA/PCINT0
AIO	AREF	ADC2	ADC1	ADC0

- **Port B, Bit 1 – MISO/DO/OC1A/PCINT9**
  - DO: Three-wire mode Universal Serial Interface Data output. Three-wire mode Data output overrides PORTB1 value and it is driven to the port when data direction bit DDB1 is set (one). PORTB1 still enables the pull-up, if the direction is input and PORTB1 is set (one).
  - OC1A: Output Compare Match output: The PB1 pin can serve as an external output for the Timer/Counter1 Compare Match B when configured as an output (DDB1 set). The OC1A pin is also the output pin for the PWM mode timer function.
  - PCINT9: Pin Change Interrupt source 9.

- **Port B, Bit 0 – MOSI/DI/SDA/$\overline{\text{OC1A}}$/PCINT8**
  - DI: Data Input in USI Three-wire mode. USI Three-wire mode does not override normal port functions, so pin must be configure as an input for DI function.
  - SDA: Two-wire mode Serial Interface Data.
  - $\overline{\text{OC1A}}$: Inverted Output Compare Match output: The PB0 pin can serve as an external output for the Timer/Counter1 Compare Match B when configured as an output (DDB0 set). The $\overline{\text{OC1A}}$ pin is also the inverted output pin for the PWM mode timer function.
  - PCINT8: Pin Change Interrupt source 8.

Table 10-7 and Table 10-8 relate the alternate functions of Port B to the overriding signals shown in Figure 10-5 on page 60.

Table 10-7. Overriding Signals for Alternate Functions in PB[7:4]

Signal Name	PB7/RESET/ dW/ADC10/ PCINT15	PB6/ADC9/T0/ INT0/PCINT14	PB5/XTAL2/CLKO/ OC1D/ADC8/ PCINT13(1)	PB4/XTAL1/ $\overline{\text{OC1D}}$/ADC7/ PCINT12(1)
PUOE	$\overline{\text{RSTDISBL}}$(1) • DWEN(1)	0	$\overline{\text{INTRC}}$ • $\overline{\text{EXTCLK}}$	INTRC
PUOV	1	0	0	0
DDOE	RSTDISBL(1) • DWEN(1)	0	$\overline{\text{INTRC}}$ • $\overline{\text{EXTCLK}}$	INTRC
DDOV	debugWire Transmit	0	0	0
PVOE	0	0	OC1D Enable	OC1D Enable
PVOV	0	0	OC1D	OC1D
PTOE	0	0	0	0
DIEOE	0	$\overline{\text{RSTDISBL}}$ + (PCINT14 • PCIE + ADC9D)	INTRC • EXTCLK + PCINT13 • PCIE + ADC8D	$\overline{\text{INTRC}}$ + PCINT12 • PCIE + ADC7D
DIEOV	ADC10D	ADC9D	(INTRC • EXTCLK) + ADC8D	INTRC • ADC7D
DI	PCINT15	T0/INT0/PCINT14	PCINT13	PCINT12
AIO	RESET / ADC10	ADC9	XTAL2, ADC8	XTAL1, ADC7

Note: 1. “1” when the Fuse is “0” (Programmed).

Figure 11-9. Timer/Counter Timing Diagram, Setting of OCF0x, with Prescaler ($f_{clk\_I/O}/8$)

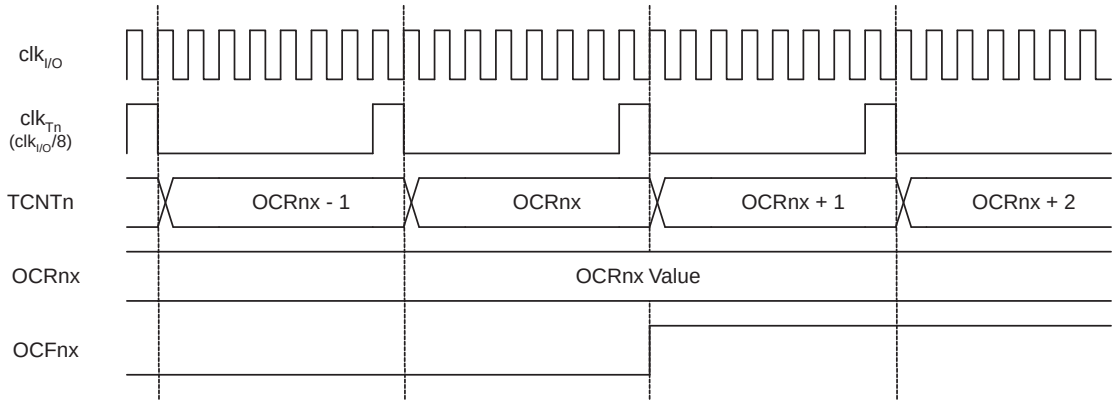
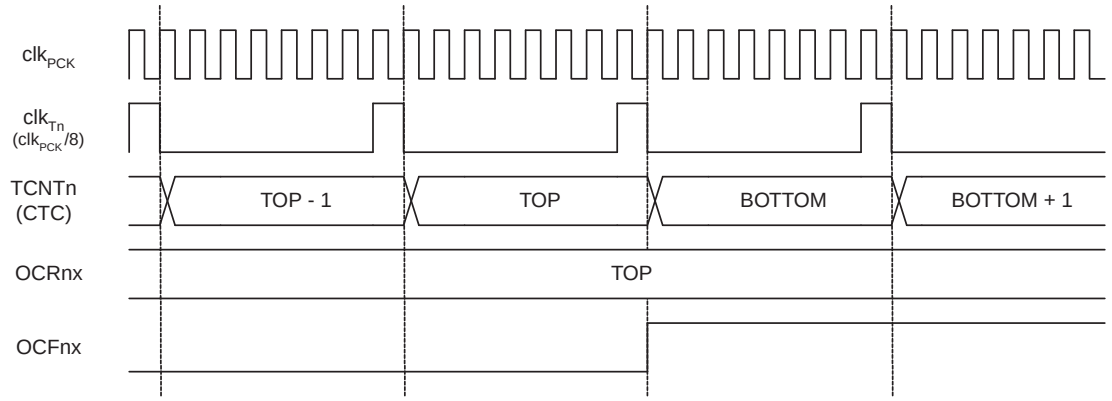


Figure 11-10 shows the setting of OCF0A and the clearing of TCNT0 in CTC mode.

Figure 11-10. Timer/Counter Timing Diagram, CTC mode, with Prescaler ($f_{clk\_I/O}/8$)



11.9 Accessing Registers in 16-bit Mode

In 16-bit mode (the TCW0 bit is set to one) the TCNT0H/L and OCR0A/B or TCNT0L/H and OCR0B/A are 16-bit registers that can be accessed by the AVR CPU via the 8-bit data bus. The 16-bit register must be byte accessed using two read or write operations. The 16-bit Timer/Counter has a single 8-bit register for temporary storing of the high byte of the 16-bit access. The same temporary register is shared between all 16-bit registers. Accessing the low byte triggers the 16-bit read or write operation. When the low byte of a 16-bit register is written by the CPU, the high byte stored in the temporary register, and the low byte written are both copied into the 16-bit register in the same clock cycle. When the low byte of a 16-bit register is read by the CPU, the high byte of the 16-bit register is copied into the temporary register in the same clock cycle as the low byte is read.

There is one exception in the temporary register usage. In the Output Compare mode the 16-bit Output Compare Register OCR0A/B is read without the temporary register, because the Output Compare Register contains a fixed value that is only changed by CPU access. However, in 16-bit Input Capture mode the ICR0 register formed by the OCR0A and OCR0B registers must be accessed with the temporary register.

To do a 16-bit write, the high byte must be written before the low byte. For a 16-bit read, the low byte must be read before the high byte.

The following code examples show how to do an atomic read of the TCNT0 register contents. Reading any of the OCR0 register can be done by using the same principle.

Assembly Code Example

```
TIM0_ReadTCNT0:
  ; Save global interrupt flag
  in  r18,SREG
  ; Disable interrupts
  cli
  ; Read TCNT0 into r17:r16
  in  r16,TCNT0L
  in  r17,TCNT0H
  ; Restore global interrupt flag
  out SREG,r18
  ret
```

C Code Example

```
unsigned int TIM0_ReadTCNT0( void )
{
  unsigned char sreg;
  unsigned int i;
  /* Save global interrupt flag */
  sreg = SREG;
  /* Disable interrupts */
  _CLI();
  /* Read TCNT0 into i */
  i = TCNT0L;
  i |= ((unsigned int)TCNT0H << 8);
  /* Restore global interrupt flag */
  SREG = sreg;
  return i;
}
```

Note: See “Code Examples” on page 6.

The assembly code example returns the TCNT0H/L value in the r17:r16 register pair.

pins. The Fault Protection Enable (FPEN1) is automatically cleared at the same system clock as the COM1nx bits are cleared.

If the Fault Protection Interrupt Enable bit (FPIE1) is set, a Fault Protection interrupt is generated and the FPEN1 bit is cleared. Alternatively the FPEN1 bit can be polled by software to figure out when the Timer/Counter has entered to Fault Protection mode.

12.10.1 Fault Protection Trigger Source

The main trigger source for the Fault Protection unit is the external interrupt pin (INT0). Alternatively the Analog Comparator output can be used as trigger source for the Fault Protection unit. The Analog Comparator is selected as trigger source by setting the Fault Protection Analog Comparator (FPAC1) bit in the Timer/Counter1 Control Register (TCCR1D). Be aware that changing trigger source can trigger a Fault Protection mode. Therefore it is recommended to clear the FPF1 flag after changing trigger source, setting edge detector or enabling the Fault Protection.

Both the external interrupt pin (INT0) and the Analog Comparator output (ACO) inputs are sampled using the same technique as with the T0 pin (see Figure 11-3 on page 73). The edge detectors are also identical but when the noise canceler is enabled additional logic is activated before the edge detector, increasing the propagation delay with four system clock cycles.

An Input Capture can also be triggered by software by controlling the port of the INT0 pin.

12.10.2 Noise Canceler

The noise canceler uses a simple digital filtering technique to improve noise immunity. Consecutive samples are monitored in a pipeline four units deep. The signal going to the edge detecter is allowed to change only when all four samples are equal.

The noise canceler is enabled by setting the Fault Protection Noise Canceler (FPNC1) bit in Timer/Counter1 Control Register D (TCCR1D). When enabled, the noise canceler introduces an additional delay of four system clock cycles to a change applied to the input.

The noise canceler uses the system clock directly and is therefore not affected by the prescaler.

12.11 Accessing 10-Bit Registers

If 10-bit values are written to the TCNT1 and OCR1A/B/C/D registers, the 10-bit registers can be byte accessed by the AVR CPU via the 8-bit data bus using two read or write operations. The 10-bit registers have a common 2-bit Timer/Counter1 High Byte Register (TC1H) that is used for temporary storing of the two MSBs of the 10-bit access. The same TC1H register is shared between all 10-bit registers. Accessing the low byte triggers the 10-bit read or write operation. When the low byte of a 10-bit register is written by the CPU, the high byte stored in the TC1H register, and the low byte written are both copied into the 10-bit register in the same clock cycle. When the low byte of a 10-bit register is read by the CPU, the high byte of the 10-bit register is copied into the TC1H register in the same clock cycle as the low byte is read.

To do a 10-bit write, the high byte must be written to the TC1H register before the low byte is written. For a 10-bit read, the low byte must be read before the high byte.

12.11.1 Reusing the temporary high byte register

If writing to more than one 10-bit register where the high byte is the same for all registers written, then the high byte only needs to be written once. However, note that the same rule of atomic operation described previously also applies in this case.

12.12.7 TCNT1 – Timer/Counter1

Bit	7	6	5	4	3	2	1	0	
0x2E (0x4E)	MSB							LSB	TCNT1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

This 8-bit register contains the value of Timer/Counter1.

The Timer/Counter1 is realized as a 10-bit up/down counter with read and write access. Due to synchronization of the CPU, Timer/Counter1 data written into Timer/Counter1 is delayed by one and half CPU clock cycles in synchronous mode and at most one CPU clock cycles for asynchronous mode. When a 10-bit accuracy is preferred, special procedures must be followed for accessing the 10-bit TCNT1 register via the 8-bit AVR data bus. These procedures are described in section “Accessing 10-Bit Registers” on page 107. Alternatively the Timer/Counter1 can be used as an 8-bit Timer/Counter. Note that the Timer/Counter1 always starts counting up after writing the TCNT1 register.

12.12.8 TC1H – Timer/Counter1 High Byte

Bit	7	6	5	4	3	2	1	0	
0x25 (0x45)	–	–	–	–	–	–	TC19	TC18	TC1H
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The temporary Timer/Counter1 register is an 2-bit read/write register.

- **Bits 7:2 – Res: Reserved Bits**

These bits are reserved and always reads zero.

- **Bits 1:0 – TC19, TC18: Two MSB bits of the 10-bit accesses**

If 10-bit accuracy is used, the Timer/Counter1 High Byte Register (TC1H) is used for temporary storing the MSB bits (TC19, TC18) of the 10-bit acceses. The same TC1H register is shared between all 10-bit registers within the Timer/Counter1. Note that special procedures must be followed when accessing the 10-bit TCNT1 register via the 8-bit AVR data bus. These procedures are described in section “Accessing 10-Bit Registers” on page 107.

12.12.9 OCR1A – Timer/Counter1 Output Compare Register A

Bit	7	6	5	4	3	2	1	0	
0x2D (0x4D)	MSB							LSB	OCR1A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The output compare register A is an 8-bit read/write register.

The Timer/Counter Output Compare Register A contains data to be continuously compared with Timer/Counter1. Actions on compare matches are specified in TCCR1A. A compare match does only occur if Timer/Counter1 counts to the OCR1A value. A software write that sets TCNT1 and OCR1A to the same value does not generate a compare match.

A compare match will set the compare interrupt flag OCF1A after a synchronization delay following the compare event.

Note that, if 10-bit accuracy is used special procedures must be followed when accessing the internal 10-bit Ouput Compare Registers via the 8-bit AVR data bus. These procedures are described in section “Accessing 10-Bit Registers” on page 107.

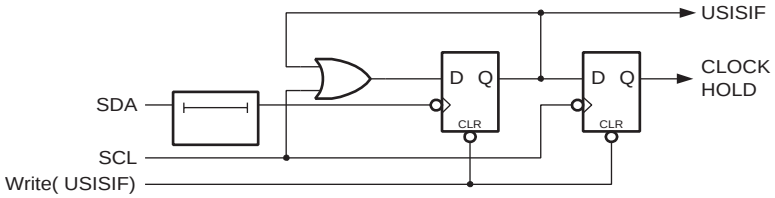
3. The master set the first bit to be transferred and releases the SCL line (C). The slave samples the data and shifts it into the USI Data Register at the positive edge of the SCL clock.
4. After eight bits containing slave address and data direction (read or write) have been transferred, the slave counter overflows and the SCL line is forced low (D). If the slave is not the one the master has addressed, it releases the SCL line and waits for a new start condition.
5. When the slave is addressed, it holds the SDA line low during the acknowledgment cycle before holding the SCL line low again (i.e., the USI Counter Register must be set to 14 before releasing SCL at (D)). Depending on the R/W bit the master or slave enables its output. If the bit is set, a master read operation is in progress (i.e., the slave drives the SDA line) The slave can hold the SCL line low after the acknowledge (E).
6. Multiple bytes can now be transmitted, all in same direction, until a stop condition is given by the master (F), or a new start condition is given.

If the slave is not able to receive more data it does not acknowledge the data byte it has last received. When the master does a read operation it must terminate the operation by forcing the acknowledge bit low after the last byte transmitted.

13.3.5 Start Condition Detector

The start condition detector is shown in Figure 13-6. The SDA line is delayed (in the range of 50 to 300 ns) to ensure valid sampling of the SCL line. The start condition detector is only enabled in Two-wire mode.

Figure 13-6. Start Condition Detector, Logic Diagram



The start condition detector works asynchronously and can therefore wake up the processor from power-down sleep mode. However, the protocol used might have restrictions on the SCL hold time. Therefore, when using this feature in this case the Oscillator start-up time set by the CKSEL Fuses (see “Clock System” on page 24) must also be taken into the consideration. Refer to the USISIF bit description on page Page 132 for further details.

13.3.6 Clock speed considerations

Maximum frequency for SCL and SCK is f_{CK} / 2. This is also the maximum data transmit and receive rate in both two- and three-wire mode. In two-wire slave mode the Two-wire Clock Control Unit will hold the SCL low until the slave is ready to receive more data. This may reduce the actual data rate in two-wire mode.

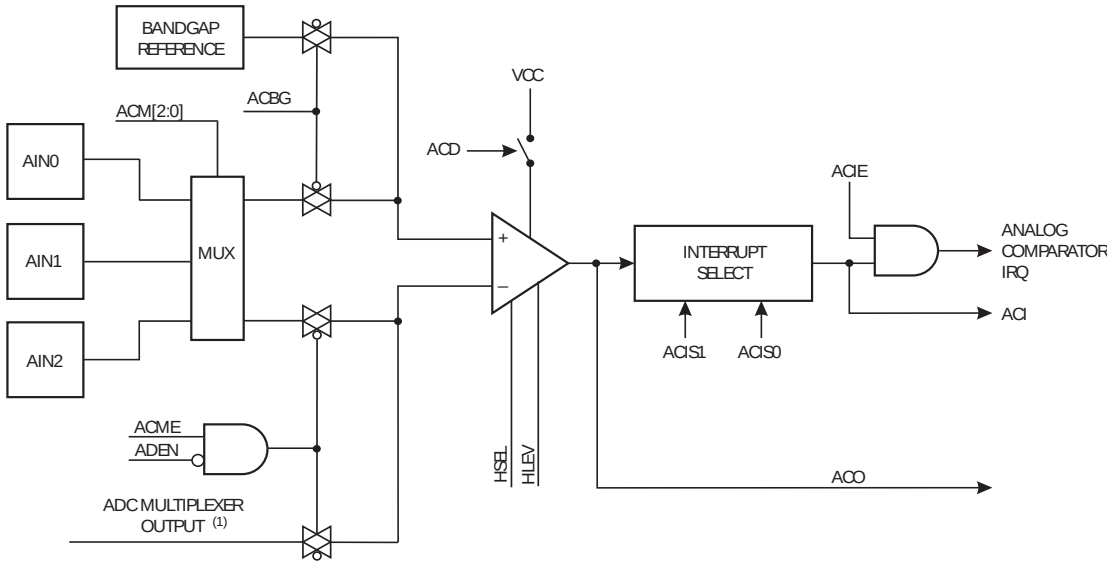
13.4 Alternative USI Usage

The flexible design of the USI allows it to be used for other tasks when serial communication is not needed. Below are some examples.

14. AC – Analog Comparator

The analog comparator compares the input values on the selectable positive pin (AIN0, AIN1 or AIN2) and selectable negative pin (AIN0, AIN1 or AIN2). When the voltage on the positive pin is higher than the voltage on the negative pin, the Analog Comparator Output, ACO, is set. The comparator can trigger a separate interrupt, exclusive to the analog comparator. The user can select Interrupt triggering on comparator output rise, fall or toggle. A block diagram of the comparator and its surrounding logic is shown in Figure 14-1.

Figure 14-1. Analog Comparator Block Diagram



Notes: 1. See Table 14-1 on page 136.

See Figure 1-1 on page 2 and Table 10-3 on page 62 for Analog Comparator pin placement.

14.1 Analog Comparator Multiplexed Input

When the Analog to Digital Converter (ADC) is configurated as single ended input channel, it is possible to select any of the ADC[10:0] pins to replace the negative input to the analog comparator. The ADC multiplexer is used to select this input, and consequently, the ADC must be switched off to utilize this feature. If the Analog Comparator Multiplexer Enable bit (ACME in ADCSRB) is set and the ADC is switched off (ADEN in ADCSRA is zero), MUX[5:0] in ADMUX select the input pin to replace the negative input to the analog comparator, as shown in Table 14-1. If ACME is cleared or ADEN is set, either AIN0, AIN1 or AIN2 is applied to the negative input to the analog comparator.

Table 14-1. Analog Comparator Multiplexed Input

ACME	ADEN	MUX[5:0]	ACM[2:0]	Positive Input	Negative Input
0	x	xxxxxx	000	AIN0	AIN1
0	x	xxxxxx	001	AIN0	AIN2
0	x	xxxxxx	010	AIN1	AIN0
0	x	xxxxxx	011	AIN1	AIN2

15. ADC – Analog to Digital Converter

15.1 Features

- **10-bit Resolution**
- **1.0 LSB Integral Non-linearity**
- **± 2 LSB Absolute Accuracy**
- **13 µs Conversion Time**
- **15 kSPS at Maximum Resolution**
- **11 Multiplexed Single Ended Input Channels**
- **16 Differential input pairs**
- **15 Differential input pairs with selectable gain**
- **Temperature Sensor Input Channel**
- **Optional Left Adjustment for ADC Result Readout**
- **0 - V_{CC} ADC Input Voltage Range**
- **Selectable 1.1V / 2.56V ADC Voltage Reference**
- **Free Running or Single Conversion Mode**
- **ADC Start Conversion by Auto Triggering on Interrupt Sources**
- **Interrupt on ADC Conversion Complete**
- **Sleep Mode Noise Cancele**
- **Unipolar / Bipolar Input Mode**
- **Input Polarity Reversal Mode**

15.2 Overview

A 10-bit, successive approximation, Analog to Digital Converter (ADC) is connected to a 11-channel analog multiplexer, which allows 16 differential voltage input combinations and 11 single-ended voltage inputs constructed from the pins PA[7:0] or PB[7:4]. The differential input is equipped with a programmable gain stage, providing amplification steps of 1x, 8x, 20x or 32x on the differential input voltage before the A/D conversion. The single-ended voltage inputs refer to 0V (GND).

The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion. A block diagram of the ADC is shown in Figure 15-1 on page 142.

Internal reference voltages of nominally 1.1V or 2.56V are provided On-chip. The Internal reference voltage of 2.56V, can optionally be externally decoupled at the AREF (PA3) pin by a capacitor, for better noise performance. Alternatively, V_{CC} can be used as reference voltage for single ended channels. There is also an option to use an external voltage reference and turn-off the internal voltage reference. These options are selected using the REFS[2:0] bits of the ADCSRB and ADMUX registers.

16. debugWIRE On-chip Debug System

16.1 Features

- **Complete Program Flow Control**
- **Emulates All On-chip Functions, Both Digital and Analog , except RESET Pin**
- **Real-time Operation**
- **Symbolic Debugging Support (Both at C and Assembler Source Level, or for Other HLLs)**
- **Unlimited Number of Program Break Points (Using Software Break Points)**
- **Non-intrusive Operation**
- **Electrical Characteristics Identical to Real Device**
- **Automatic Configuration System**
- **High-Speed Operation**
- **Programming of Non-volatile Memories**

16.2 Overview

The debugWIRE On-chip debug system uses a One-wire, bi-directional interface to control the program flow, execute AVR instructions in the CPU and to program the different non-volatile memories.

16.3 Physical Interface

When the debugWIRE Enable (DWEN) Fuse is programmed and Lock bits are unprogrammed, the debugWIRE system within the target device is activated. The RESET port pin is configured as a wire-AND (open-drain) bi-directional I/O pin with pull-up enabled and becomes the communication gateway between target and emulator.

Figure 16-1 shows the schematic of a target MCU, with debugWIRE enabled, and the emulator connector. The system clock is not affected by debugWIRE and will always be the clock source selected by the CKSEL Fuses.

Figure 16-1. The debugWIRE Setup

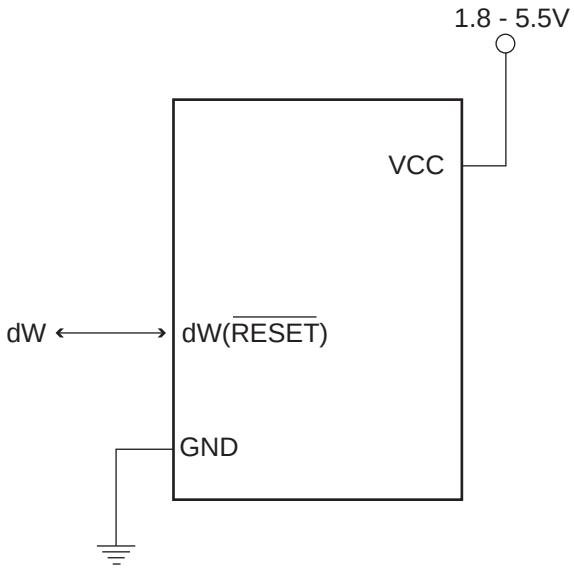


Figure 20-54. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 8 MHz)

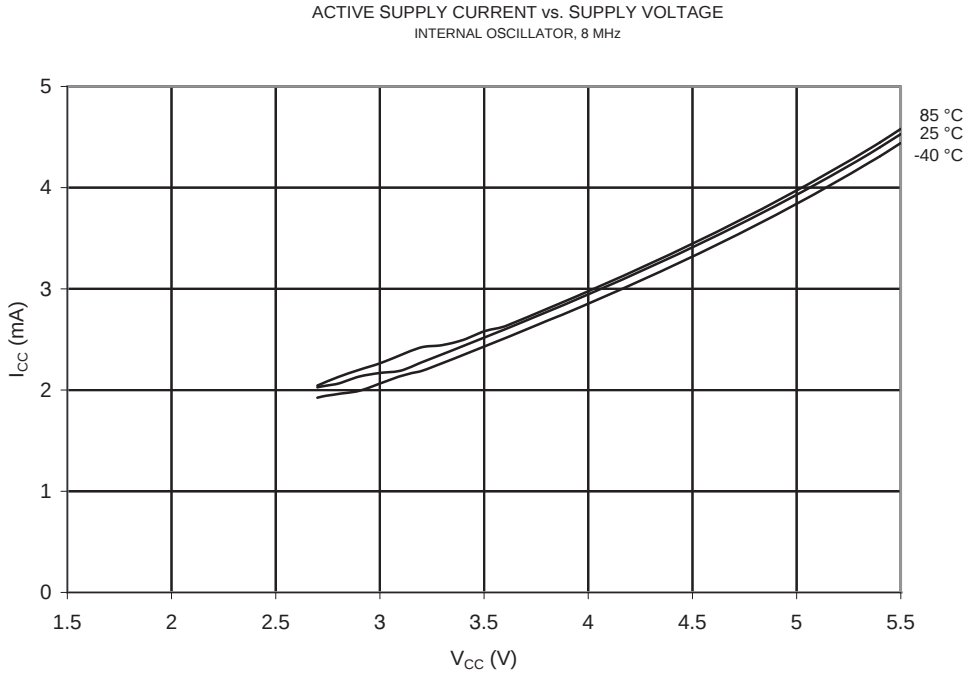


Figure 20-55. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 1 MHz)

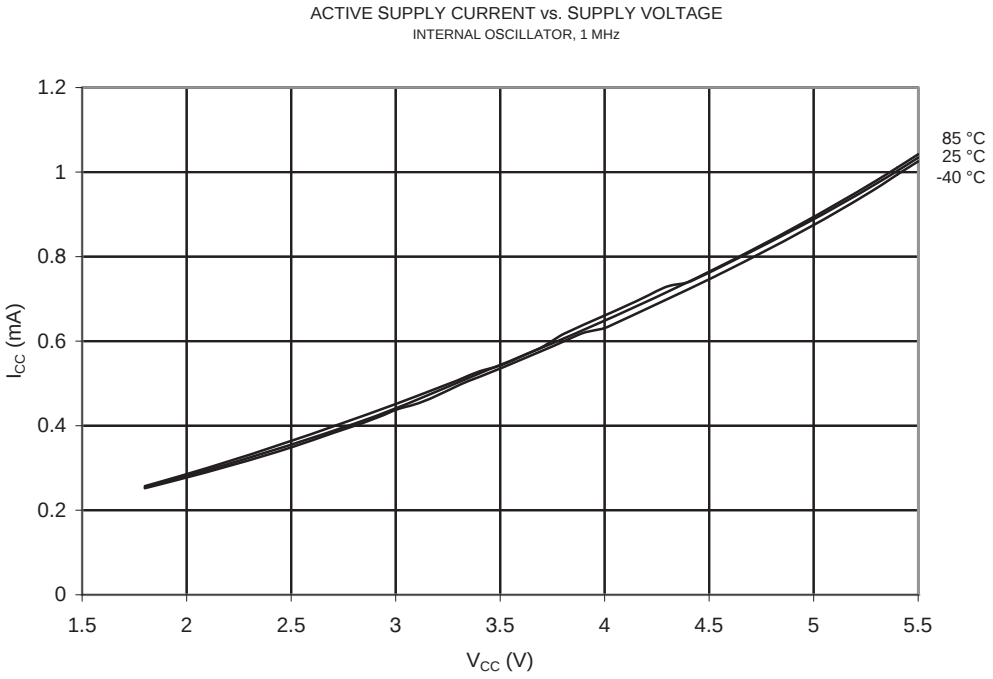


Figure 20-74. Pull-Up Resistor Current vs. Input Voltage (Reset Pin, V_{CC} = 1.8V)

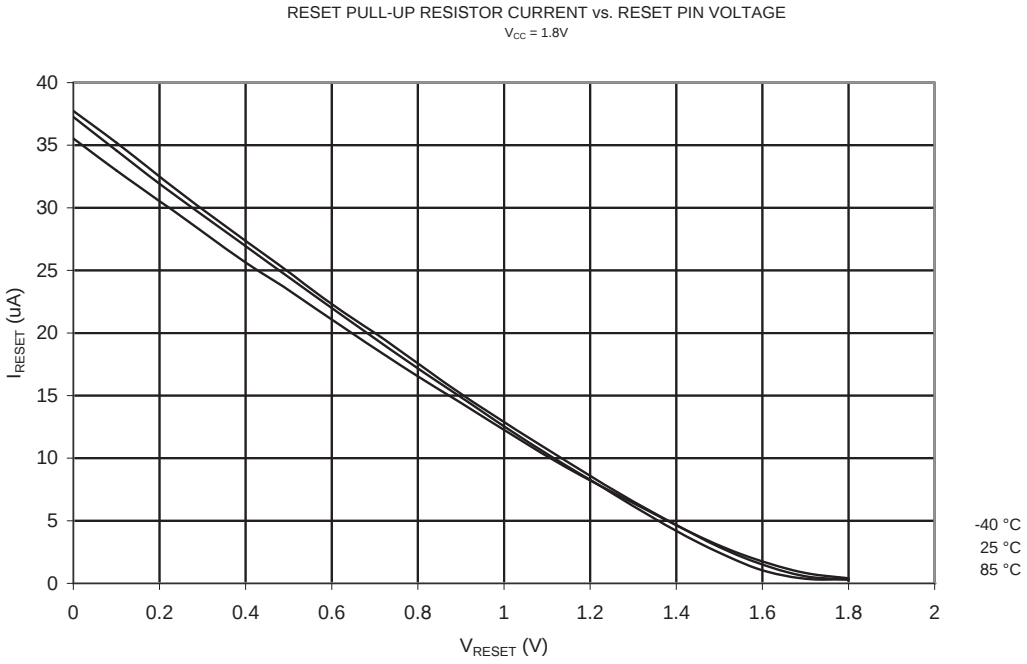


Figure 20-75. Pull-Up Resistor Current vs. Input Voltage (Reset Pin, V_{CC} = 3V)

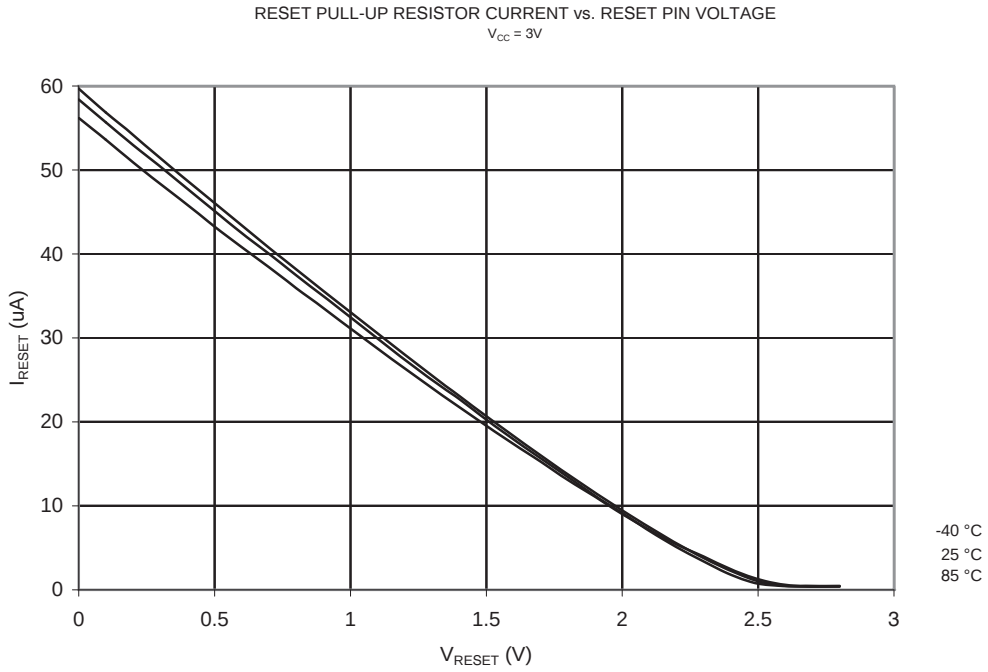


Figure 20-82. V_{OH}: Output Voltage vs. Source Current (I/O Pin, V_{CC} = 5V)

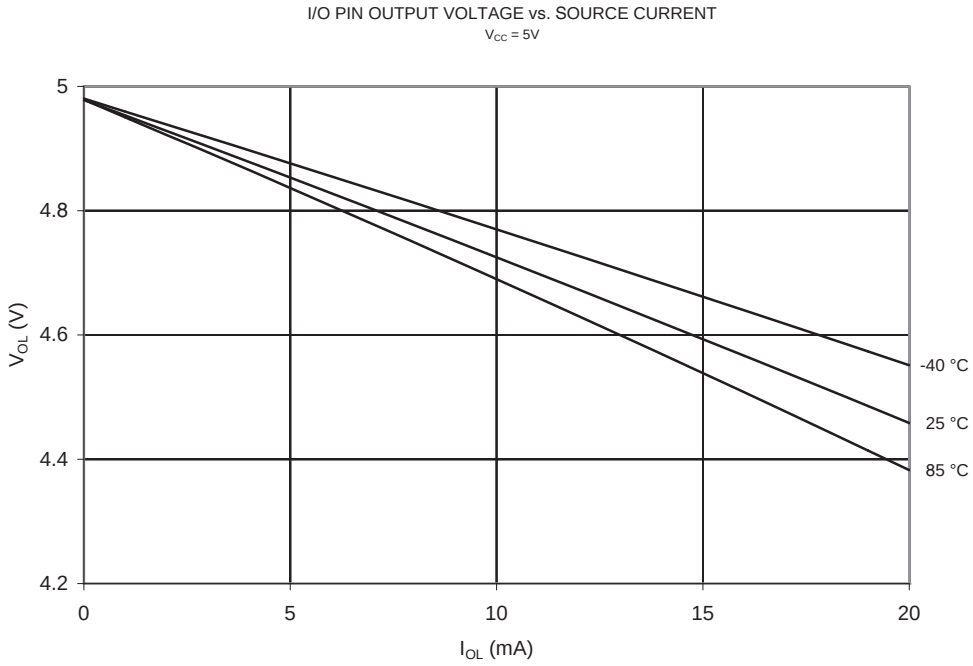


Figure 20-83. V_{OL}: Output Voltage vs. Sink Current (Reset Pin as I/O, V_{CC} = 5V)

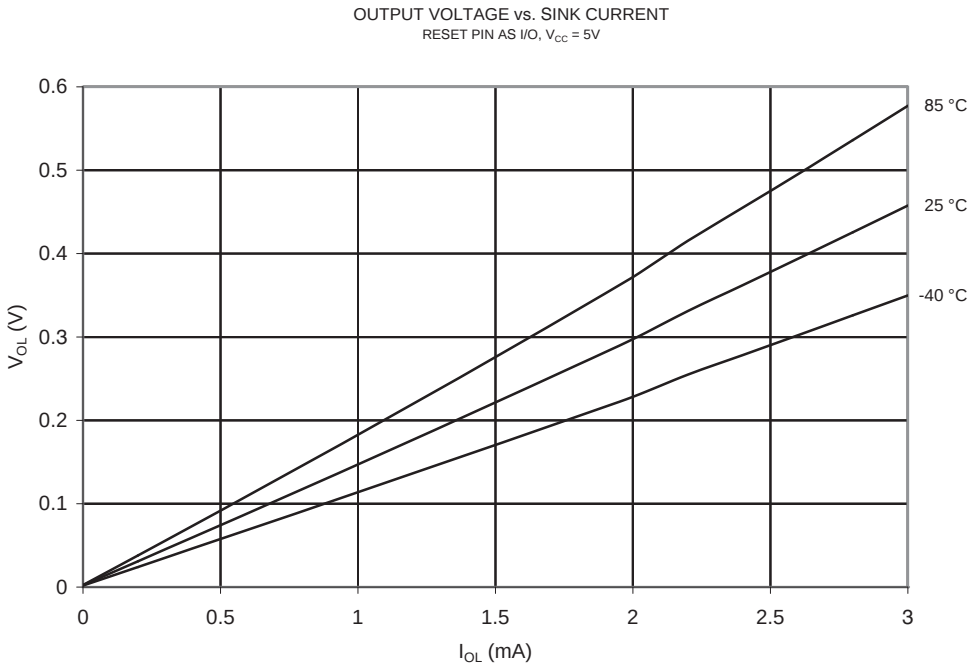


Figure 20-105. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 8 MHz)

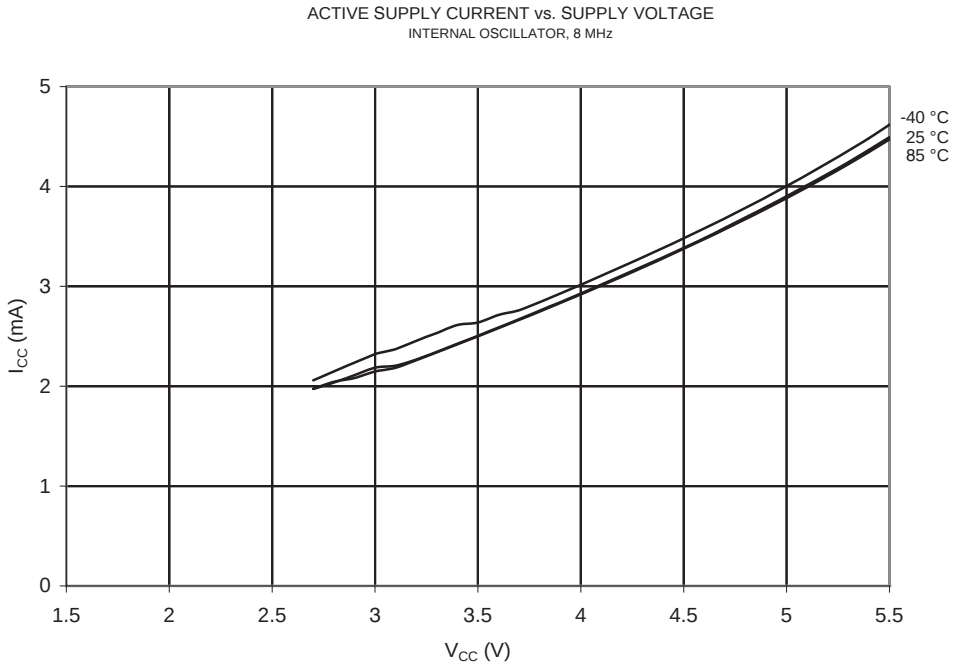
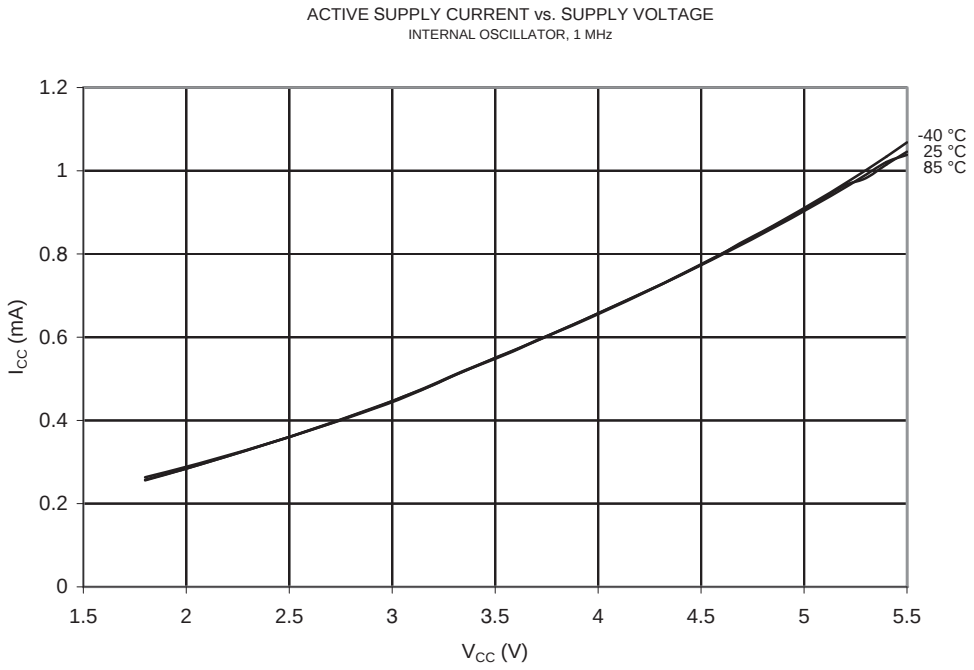


Figure 20-106. Active Supply Current vs. V_{CC} (Internal Calibrated Oscillator, 1 MHz)



20.4.3 Current Consumption in Power-Down Mode

Figure 20-113. Power-down Supply Current vs. V_{CC} (Watchdog Timer Disabled)

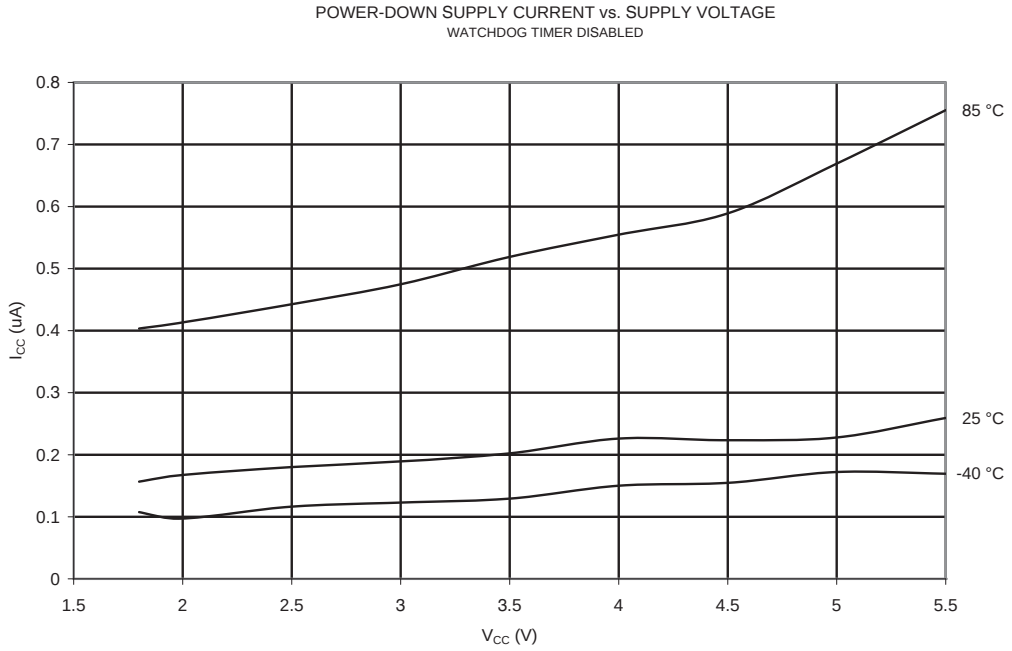


Figure 20-114. Power-down Supply Current vs. V_{CC} (Watchdog Timer Enabled)

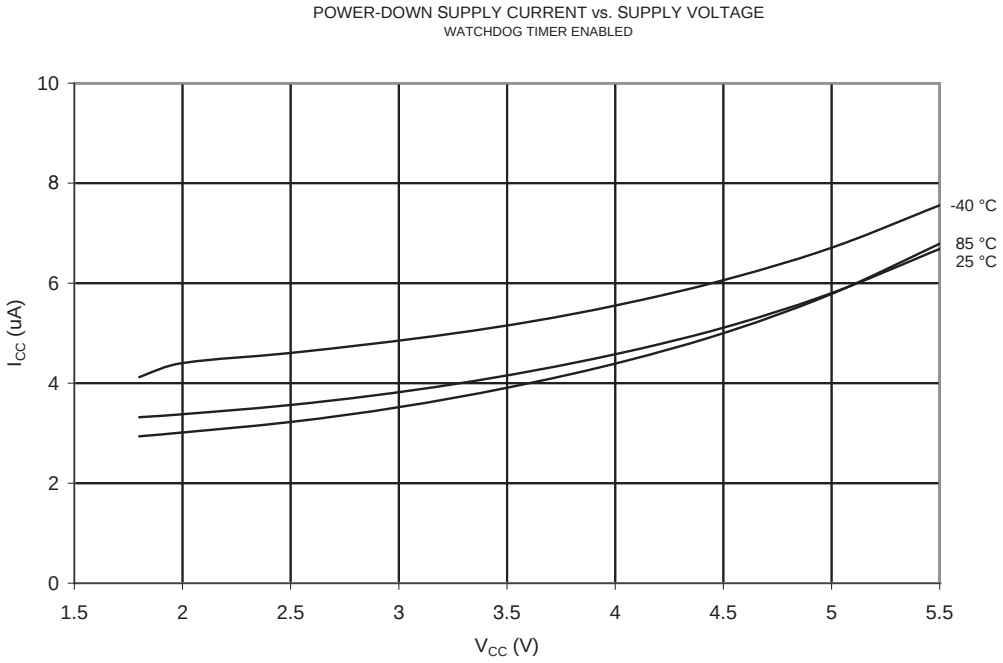


Figure 20-141. V_{IH}: Input Threshold Voltage vs. V_{CC} (Reset Pin, Read as ‘1’)

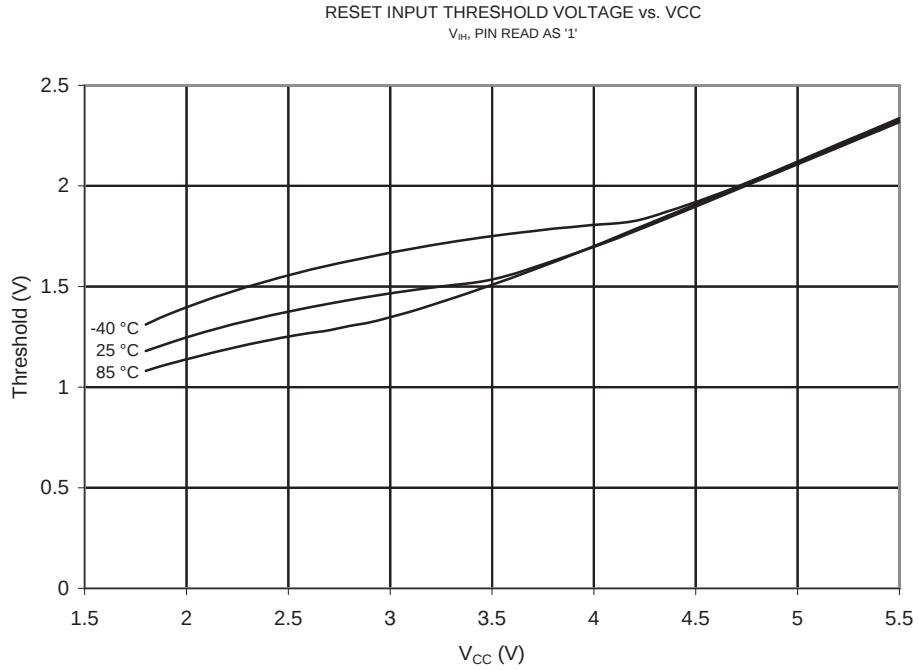
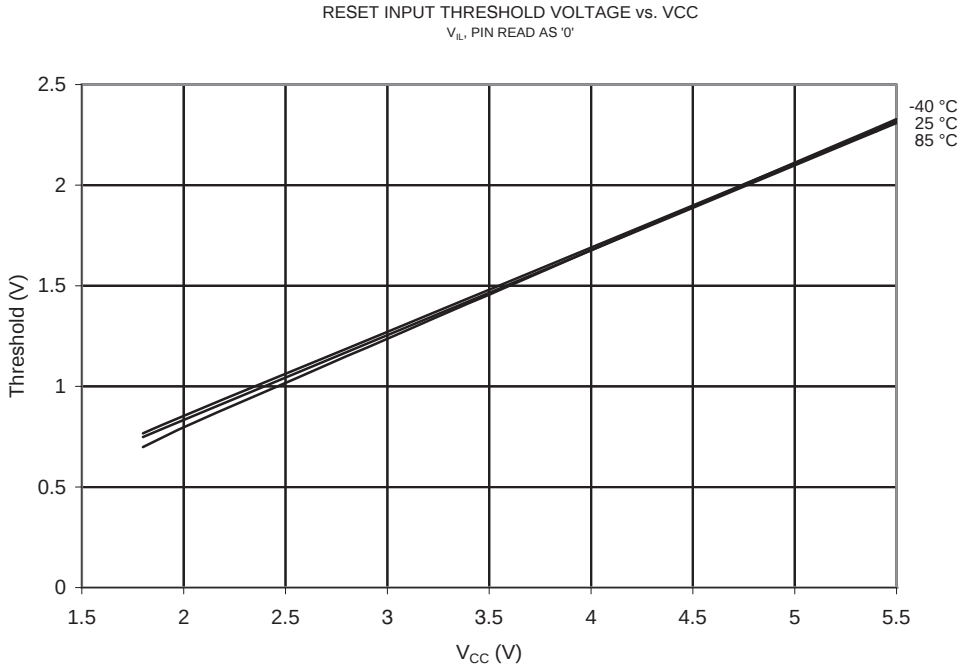
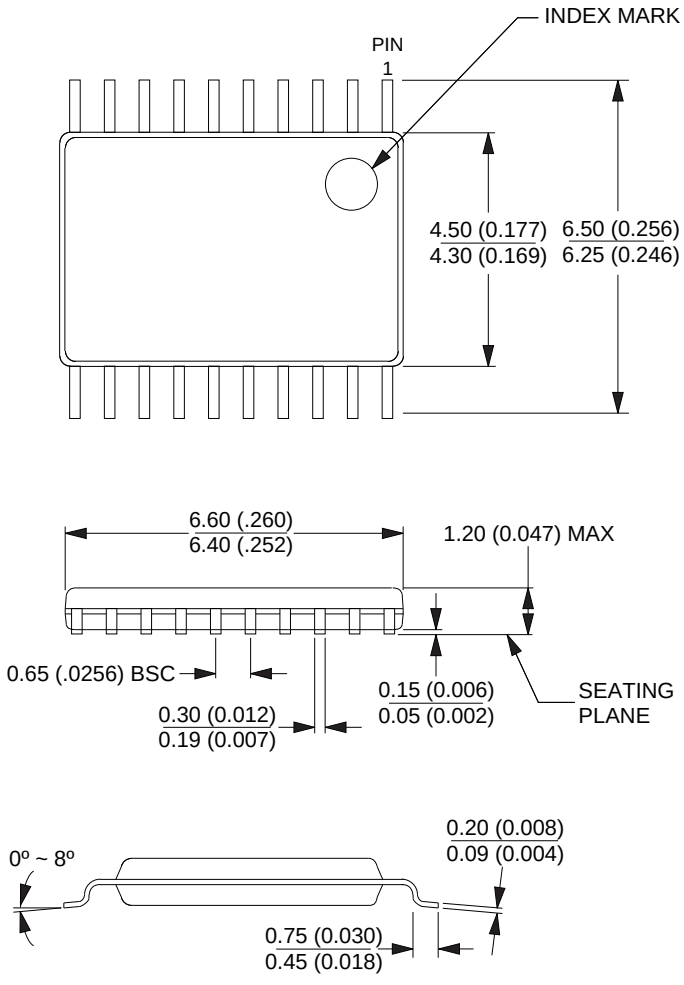


Figure 20-142. V_{IL}: Input Threshold Voltage vs. V_{CC} (Reset Pin, Read as ‘0’)



24.4 20X

Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.
JEDEC Standard MO-153 AC



10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20X**, (Formerly 20T), 20-lead, 4.4 mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	20X	C

26. Datasheet Revision History

26.1 Rev. 8197C – 05/11

1. Added:
   - Section 3.3 “Capacitive Touch Sensing” on page 6
   - Section 4. “CPU Core” on page 7
   - Table 6-10, “Capacitance of Low-Frequency Crystal Oscillator,” on page 29
   - Table 15-5 on page 157
   - Section 19.7 “Analog Comparator Characteristics” on page 193
   - Table 19-8 on page 191
   - Table 19-9 on page 192
   - Tape & reel part numbers in Section 23. “Ordering Information” on page 281
   - Ordering codes for ATtiny261A with extended temperature, on page 281
2. Updated:
   - Section 6.4 “Clock Output Buffer” on page 32 (CLKO)
   - Figure 15-1 on page 142, “Analog to Digital Converter Block Schematic”, changed INTERNAL 1.18V REFERENCE to 1.1V
   - Table 18-8 on page 171, No. of Pages in the EEPROM from 64 to 32 for ATtiny261A
   - Table 19-1 on page 185
   - Section 19.3 “Speed” on page 187
   - Characteristic plots Figure 20-3 on page 200, Figure 20-8 on page 202, Figure 20-54 on page 226, Figure 20-59 on page 228, Figure 20-105 on page 252, and Figure 20-110 on page 254
   - Bit syntax throughout the datasheet, e.g. from CS02:0 to CS0[2:0]
3. Deleted:
   - “Preliminary” status. All devices now final and in production.
   - “Disclaimer” on page 6.

26.2 Rev. 8197B – 01/10

1. Updated 32M1-A drawing in Section 24. “Packaging Information” on page 284.

26.3 Rev. 8197A – 10/09

1. Initial revision created from document 2588C (ATtiny261/461/861)
2. Updated "Ordering Information" on page 281, page 282 and page 283. Pb-plated packages are no longer offered and there are no separate ordering codes for commercial operation range, the only available option now is industrial. Also, added new package options
3. Added sections:
   - “Software BOD Disable” on page 36
   - “ATtiny461A” on page 225
   - “ATtiny861A” on page 251
4. Updated sections:
   - “Stack Pointer” on page 11